ESD8118

ESD Protection Diode

Low Capacitance Array for High Speed Data Lines

The ESD8118 surge protection is specifically designed to protect four high speed data pairs from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines.

Features

- Low Capacitance (0.35 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- HDMI 1.3/1.4/2.0
- Display Port

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

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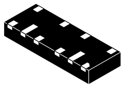
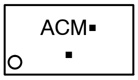
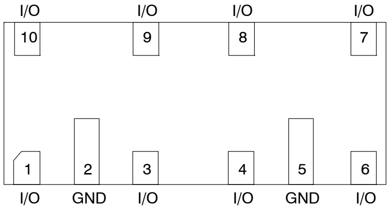


UDFN10
CASE 517CY

MARKING DIAGRAM



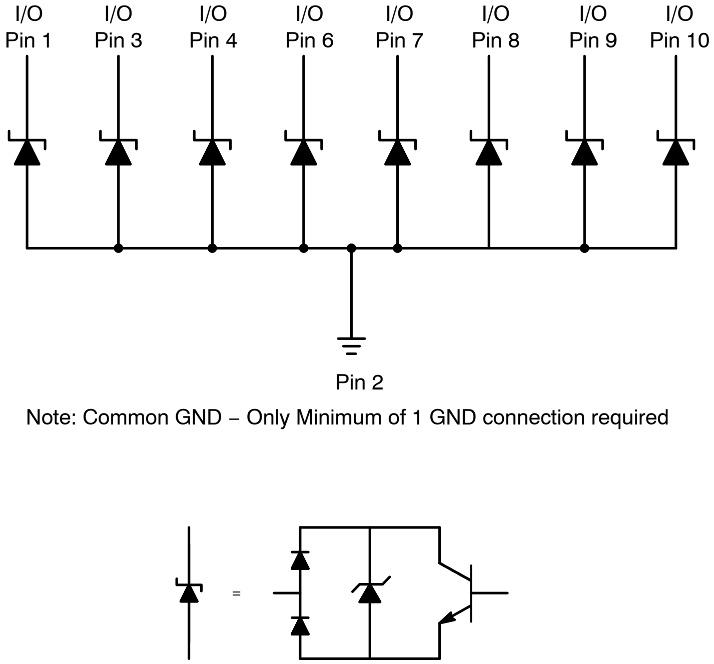
PIN CONFIGURATION



ORDERING INFORMATION

Device	Package	Shipping†
ESD8118MUTAG	UDFN10 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



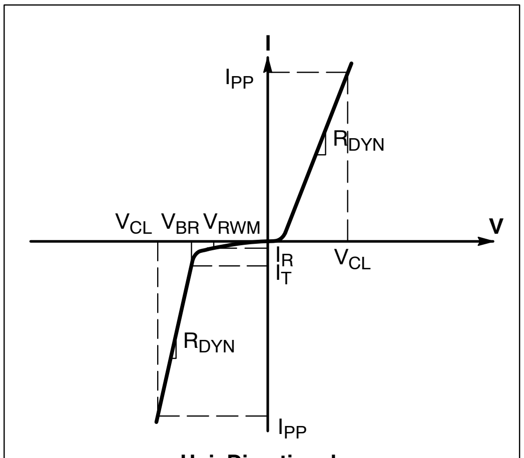
Note: Common GND − Only Minimum of 1 GND connection required

Figure 1. Pin Schematic

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V_{RWM}	Working Peak Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
V_{HOLD}	Holding Reverse Voltage
I_{HOLD}	Holding Reverse Current
R_{DYN}	Dynamic Resistance
I_{PP}	Maximum Peak Pulse Current
V_C	Clamping Voltage @ I_{PP} $V_C = V_{HOLD} + (I_{PP} * R_{DYN})$



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	4.0	5.0		V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V, I/O Pin to GND			1.0	μA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 KV Contact	See Figures 2 and 3			V
Clamping Voltage TLP (Note 2) See Figures 6 through 9	V_C	I_{PP} = 8 A I_{PP} = −8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) I_{PP} = 16 A I_{PP} = −16 A } IEC 61000−4−2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)		8.5 −4.5 11.4 −8.0		V
Dynamic Resistance	R_{DYN}	I/O Pin to GND GND to I/O Pin		0.35 0.44		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins and GND V_R = 0 V, f = 1 MHz, between I/O Pins V_R = 0 V, f = 1 MHz, T_A = 65°C between I/O Pins and GND		0.30 0.15 0.37	0.35 0.20 0.47	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. For test procedure see Figures 4 and 5 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

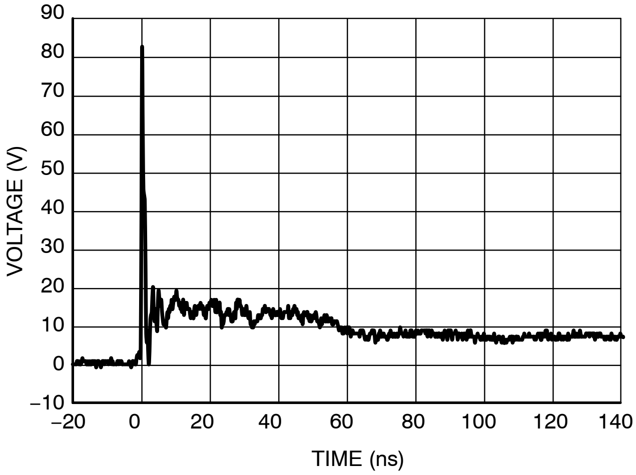


Figure 2. IEC61000−4−2 +8 kV Contact Clamping Voltage

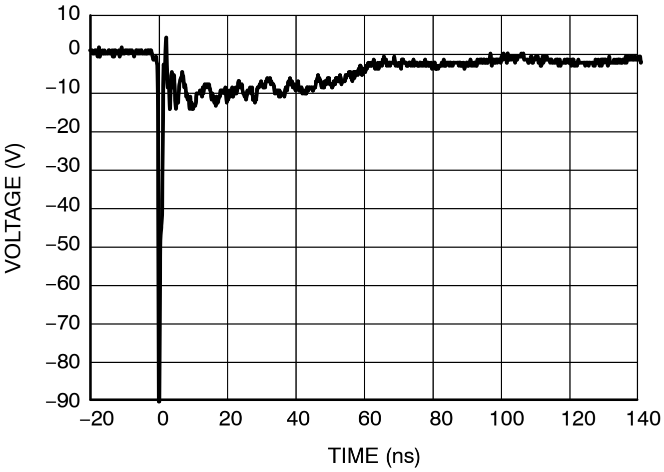


Figure 3. IEC61000−4−2 −8 kV Contact Clamping Voltage

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

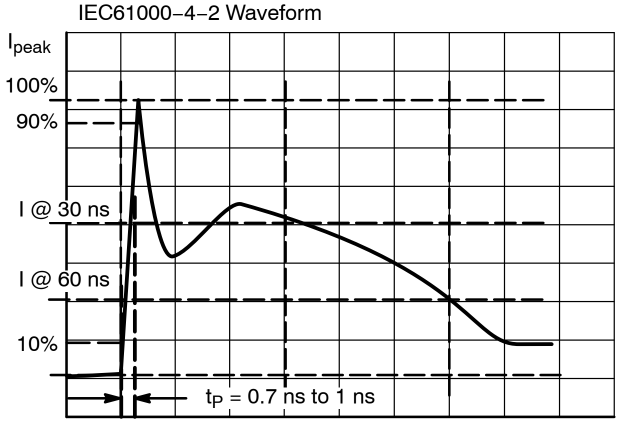


Figure 4. IEC61000−4−2 Spec

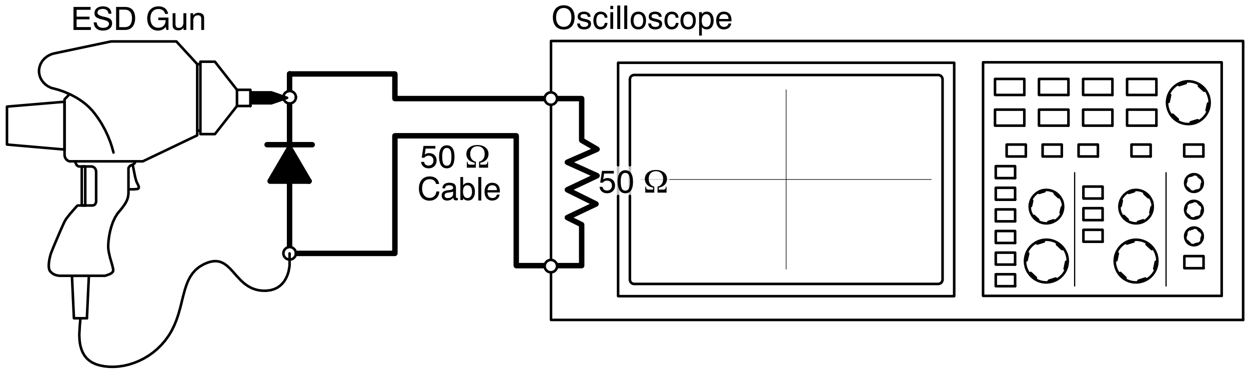


Figure 5. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8307/D – Characterization of ESD Clamping Performance.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D and AND8308/D.

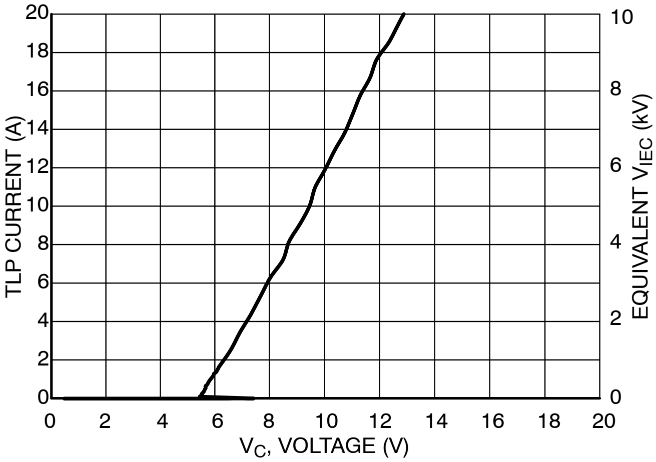


Figure 6. Positive TLP I−V Curve

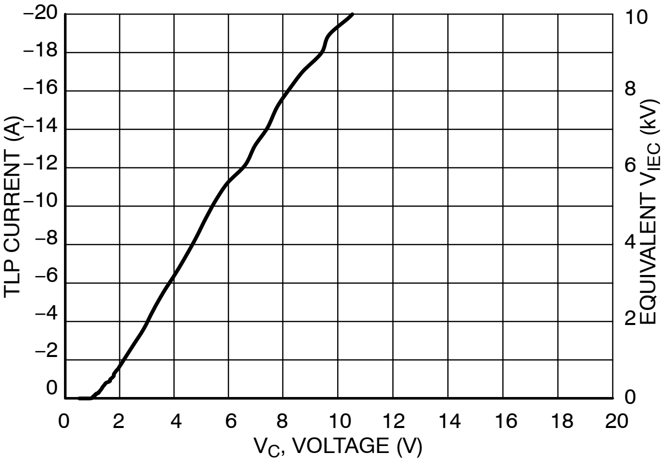


Figure 7. Negative TLP I−V Curve

NOTE: TLP parameter: Z_0 = 50 Ω, t_p = 100 ns, t_r = 300 ps, averaging window: t_1 = 30 ns to t_2 = 60 ns. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000−4−2 waveform at t = 30 ns with 2 A/kV. See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels. For more information on TLP measurements and how to interpret them please refer to AND9007/D.

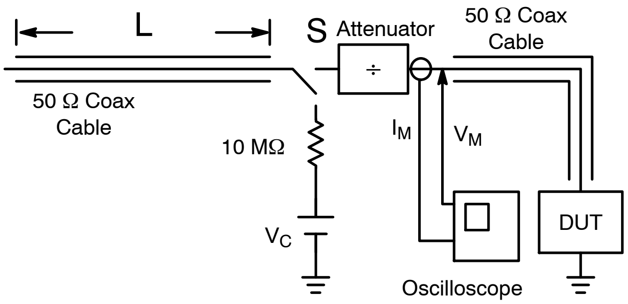


Figure 8. Simplified Schematic of a Typical TLP System

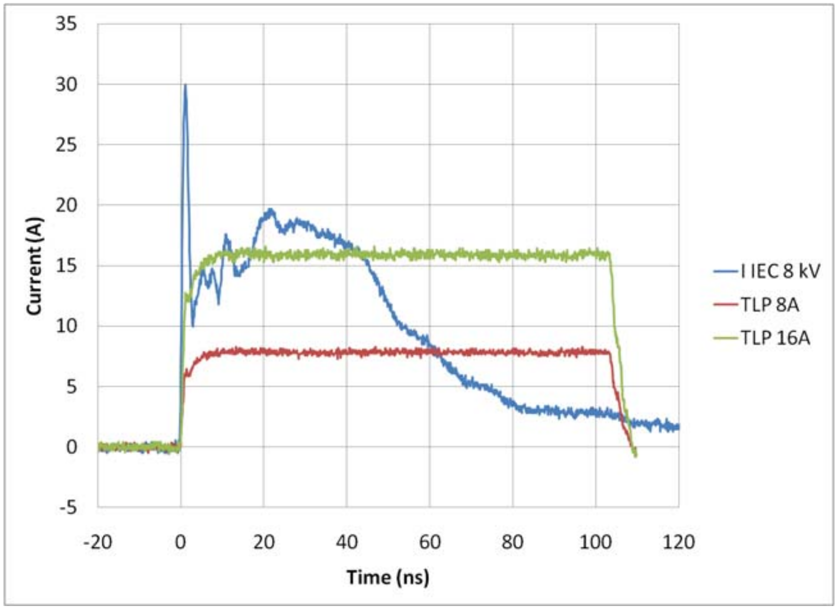


Figure 9. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

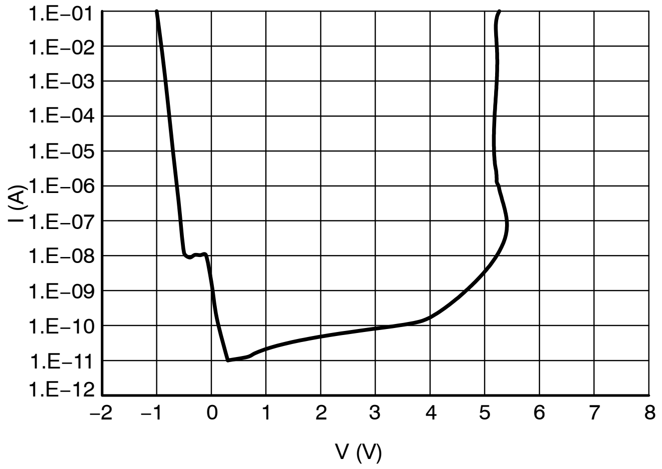


Figure 10. IV Characteristics

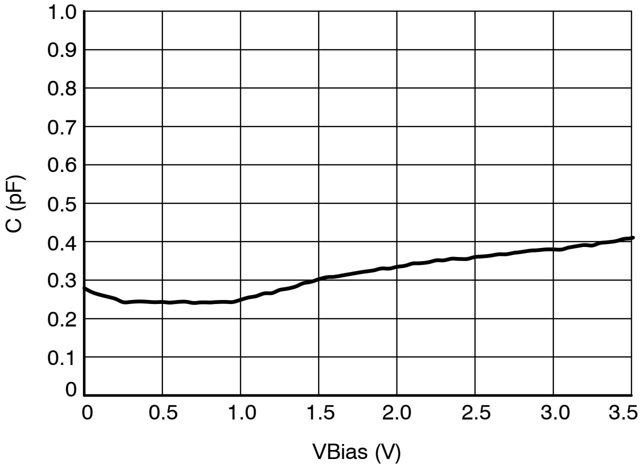


Figure 11. CV Characteristics

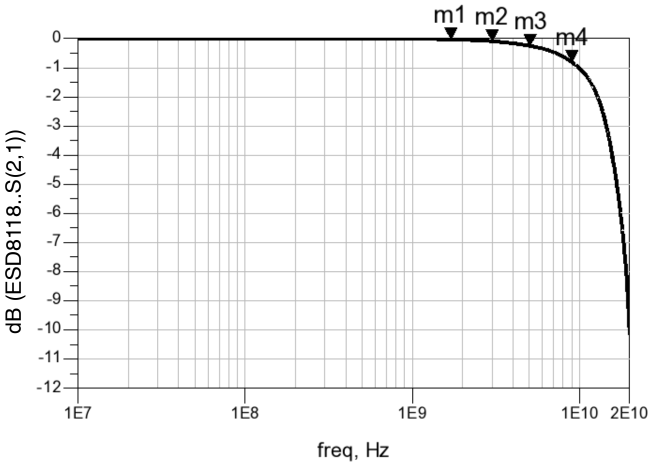


Figure 12. RF Insertion Loss

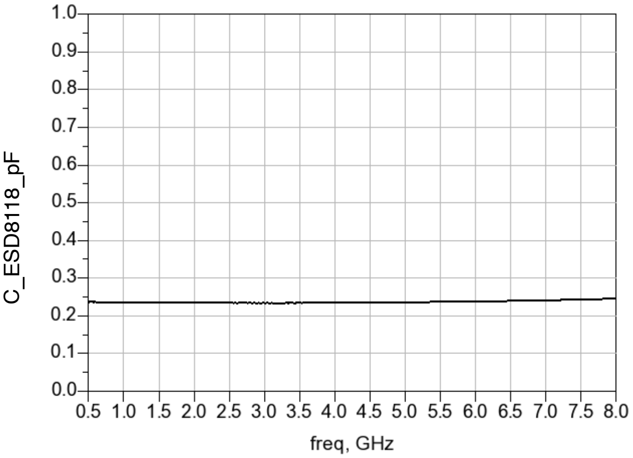
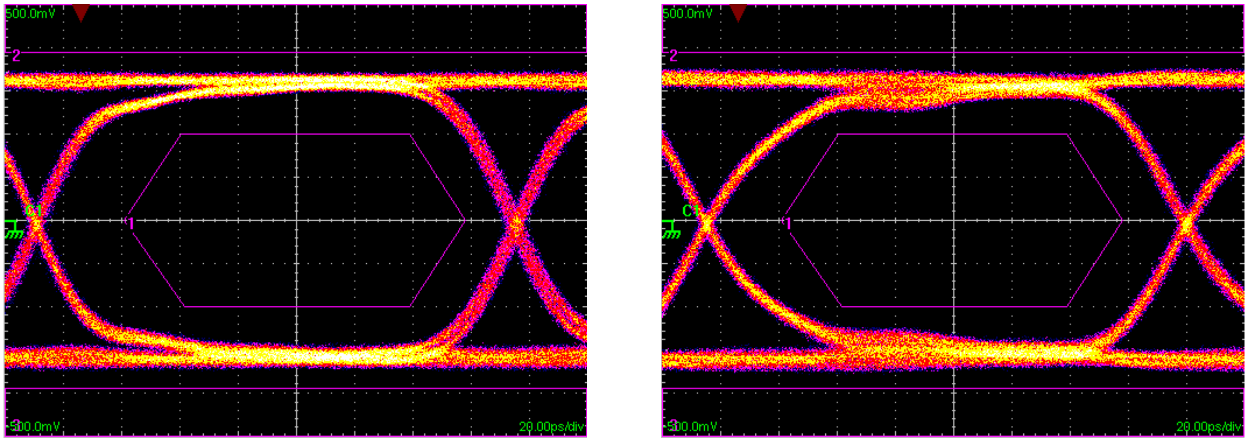


Figure 13. Capacitance over Frequency

TABLE 1. RF Insertion Loss: Application Description

Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	3rd Harmonic Frequency (GHz)	ESD8118 Insertion Loss (dB)
HDMI 1.3/1.4 HDMI 2.0	3.9 6.0	1.7 (m1) 3.0 (m2)	5.1 (m3) 9.0 (m4)	m1 = 0.030 m2 = 0.091 m3 = 0.254 m4 = 0.803



Without ESD8118

With ESD8118

Figure 14. HDMI2.0 Eye Diagram with and without ESD8118. 6 Gb/s

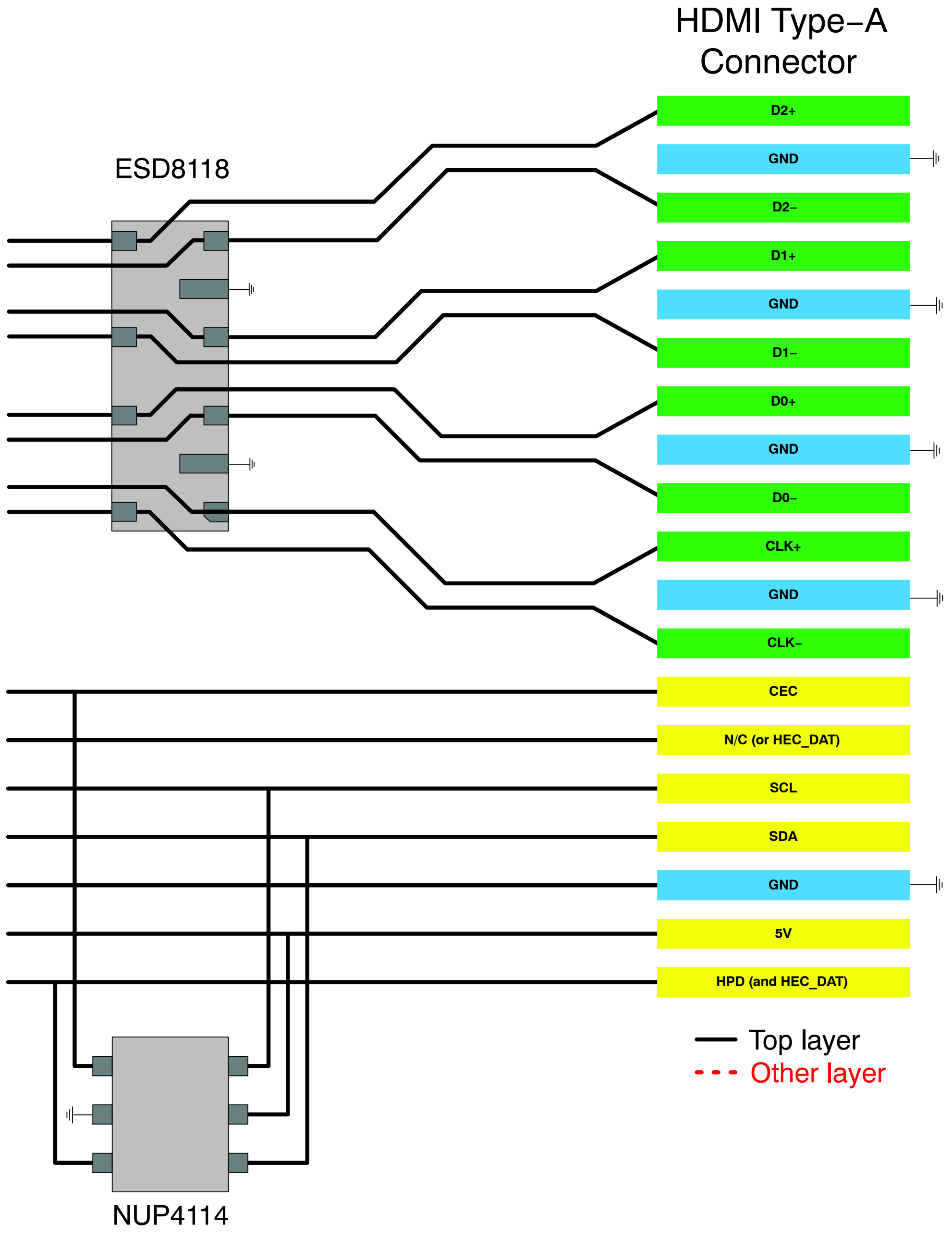


Figure 15. HDMI Layout Diagram

PCB Layout Guidelines

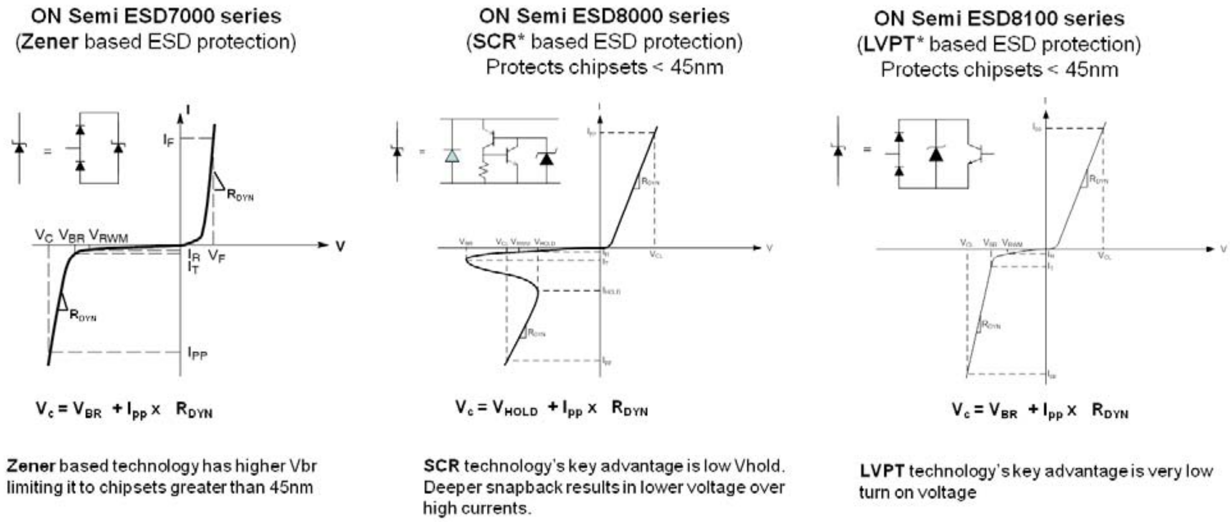
Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

- Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.
- Make sure to use differential design methodology and impedance matching of all high speed signal traces.
- Use curved traces when possible to avoid unwanted reflections.
- Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.
- Place grounds between high speed pairs and keep as much distance between pairs as possible to reduce crosstalk.

ESD Protection Device Technology

ON Semiconductor’s portfolio contains three main technologies for low capacitance ESD protection device which are highlighted below and in Figure 16.

- ESD7000 series: Zener diode based technology. This technology has a higher breakdown voltage (VBR) limiting it to protecting chipsets with larger geometries.
- ESD8000 series: Silicon controlled rectifier (SCR) type technology. The key advatange for this technology is a low holding voltage (VH) which produces a deeper snapback that results in lower voltage over high currents as shown in the TLP results in Figure 17. This technology provides optimized protection for chipsets with small geometries against thermal failures resulting in chipset damage (also known as “hard failures”).
- ESD8100 series: Low voltage punch through (LVPT) type technology. The key advatange for this technology is a very low turn-on voltage. This technology provides optimized protection for chipsets with small geometries against recoverable failures due to voltage peaks (also known as “soft failures”).


ON Semi ESD7000 series
(**Zener** based ESD protection)

ON Semi ESD8000 series
(**SCR*** based ESD protection)
Protects chipsets < 45nm

ON Semi ESD8100 series
(**LVPT*** based ESD protection)
Protects chipsets < 45nm

Zener based technology has higher Vbr limiting it to chipsets greater than 45nm

SCR technology’s key advantage is low Vhold. Deeper snapback results in lower voltage over high currents.

LVPT technology’s key advantage is very low turn on voltage

Figure 16. ON Semiconductor’s Low-cap ESD Technology Portfolio

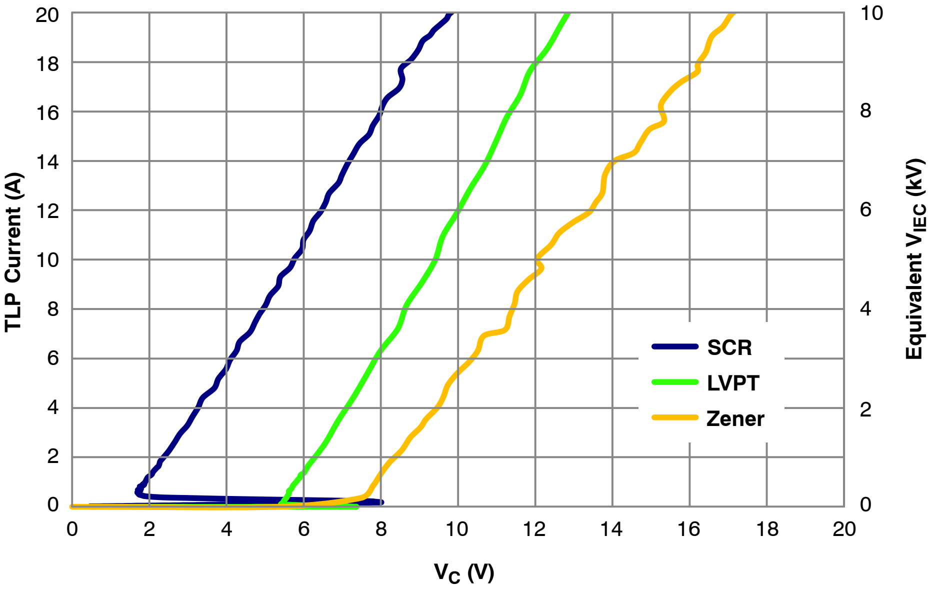
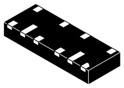


Figure 17. High Current, TLP, IV Characteristic of Each Technology

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



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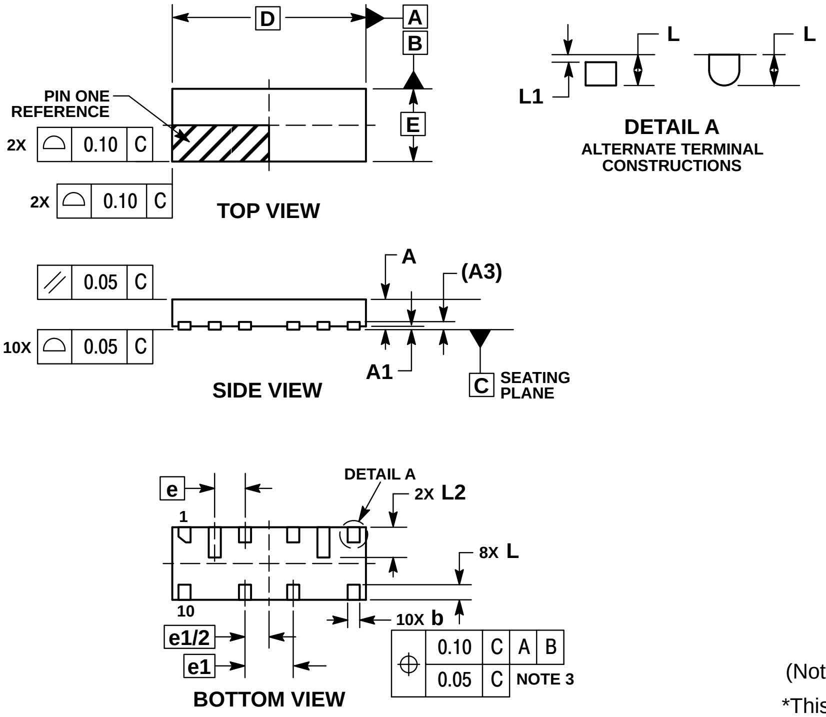
UDFN10 3.2x1.2, 0.5P
CASE 517CY
ISSUE O

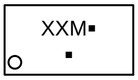
DATE 31 JUL 2014



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 mm FROM TERMINAL.

DIM	MILLIMETERS MIN	MILLIMETERS MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	3.20 BSC	
E	1.20 BSC	
e	0.50 BSC	
e1	0.80 BSC	
L	0.15	0.35
L1	---	0.10
L2	0.40	0.60

GENERIC MARKING DIAGRAM*

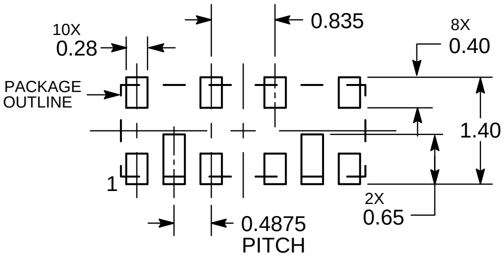


XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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