

ESD8011

ESD Protection Diodes

Ultra Low Capacitance ESD Protection Diode for High Speed Data Line

The ESD8011 ESD protection diodes are designed to protect high speed data lines from ESD. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Ultra Low Capacitance (0.10 pF Typ, I/O to GND)
- Protection for the Following IEC Standards:
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.x
- MHL 2.0
- SATA/SAS
- PCI Express

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	-55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-55 to +150	$^\circ\text{C}$
Lead Solder Temperature – Maximum (10 Seconds)	T_L	260	$^\circ\text{C}$
IEC 61000-4-2 Contact (ESD)	ESD	± 20	kV
IEC 61000-4-2 Air (ESD)	ESD	± 20	kV
Maximum Peak Pulse Current 8/20 μs @ $T_A = 25^\circ\text{C}$	I_{pp}	3.6	A
Maximum Peak Pulse Power 8/20 μs @ $T_A = 25^\circ\text{C}$	P_{pk}	34	W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.



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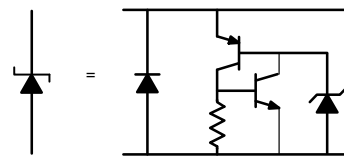
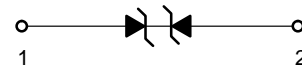
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MARKING DIAGRAM



R = Specific Device Code
(Rotated 90° clockwise)
M = Date Code

PIN CONFIGURATION AND SCHEMATIC



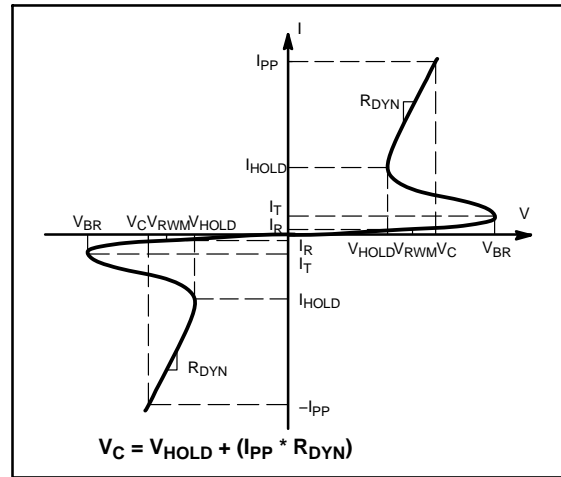
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V _{RWM}	Working Peak Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
V _{HOLD}	Holding Reverse Voltage
I _{HOLD}	Holding Reverse Current
R _{DYN}	Dynamic Resistance
I _{PP}	Maximum Peak Pulse Current
V _C	Clamping Voltage @ I _{PP} V _C = V _{HOLD} + (I _{PP} * R _{DYN})



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

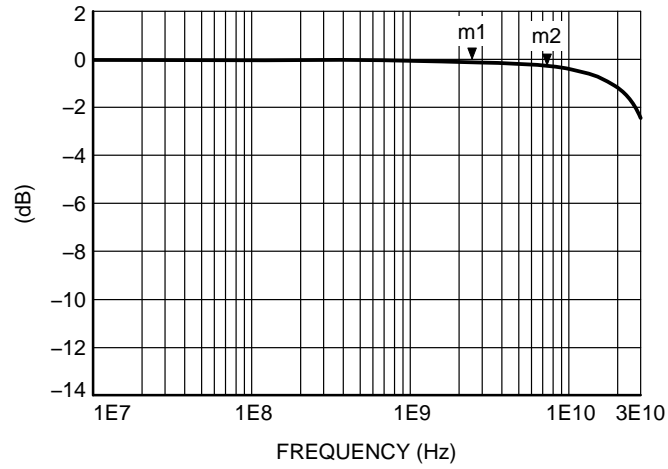
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V _{RWM}	I/O Pin to GND			5.5	V
Breakdown Voltage	V _{BR}	I _T = 1 mA, I/O Pin to GND	6.5	7.3		V
Reverse Leakage Current	I _R	V _{RWM} = 5.5 V, I/O Pin to GND			1.0	μA
Reverse Holding Voltage	V _{HOLD}	I/O Pin to GND		2.05		V
Holding Reverse Current	I _{HOLD}	I/O Pin to GND		17		mA
Clamping Voltage TLP (Note 2)	V _C	I _{PP} = 8 A } IEC61000-4-2 Level 2 Equivalent (±4 kV Contact, ±8 kV Air)		11.0		V
		I _{PP} = 16 A } IEC61000-4-2 Level 2 Equivalent (±8 kV Contact, ±16 kV Air)		19.0		V
Dynamic Resistance	R _{DYN}	Pin1 to Pin2 Pin2 to Pin1		1.0 1.0		Ω
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz		0.10	0.20	pF
Series Inductance	L _S	V _R = 0 V		0.3		nH

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- For test procedure see Figure 5 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t₁ = 30 ns to t₂ = 60 ns.

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TYPICAL CHARACTERISTICS



Interface	Data Rate (Gb/s)	Fundamental Frequency (GHz)	3 rd Harmonic Frequency (GHz)	ESD8011 Insertion Loss (dB)
USB 3.0	5	2.5 (m1)	7.5 (m2)	m1 = 0.087 m2 = 0.256

Figure 1. ESD8011 Insertion Loss

TYPICAL CHARACTERISTICS

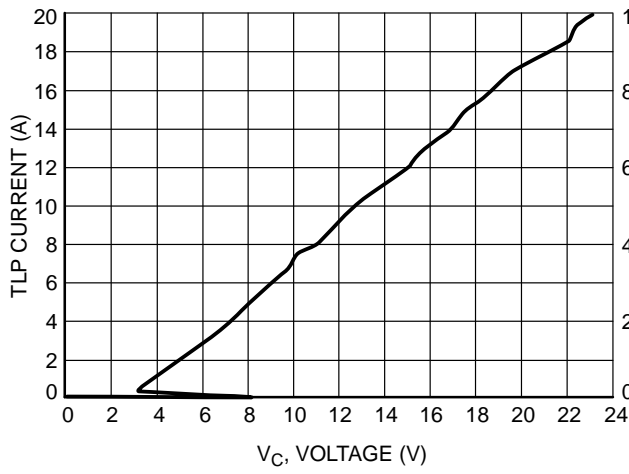


Figure 2. Positive TLP I-V Curve

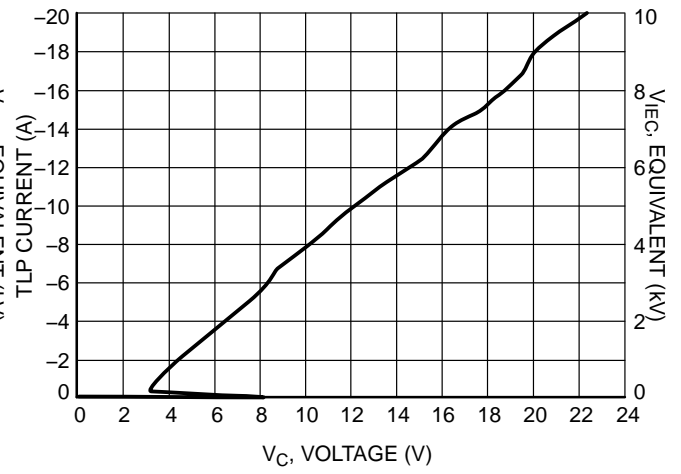


Figure 3. Negative TLP I-V Curve

Latch-Up Considerations

ON Semiconductor’s 8000 series of ESD protection devices utilize a snap-back, SCR type structure. By using this technology, the potential for a latch-up condition was taken into account by performing load line analyses of common high speed serial interfaces. Example load lines for latch-up free applications and applications with the potential for latch-up are shown below with a generic IV characteristic of a snapback, SCR type structured device overlaid on each. In the latch-up free load line case, the IV characteristic of the snapback protection device intersects the load-line in one unique point (V_{OP} , I_{OP}). This is the only

stable operating point of the circuit and the system is therefore latch-up free. In the non-latch up free load line case, the IV characteristic of the snapback protection device intersects the load-line in two points (V_{OPA} , I_{OPA}) and (V_{OPB} , I_{OPB}). Therefore in this case, the potential for latch-up exists if the system settles at (V_{OPB} , I_{OPB}) after a transient. Because of this, ESD8011 should not be used for HDMI applications – ESD8104 or ESD8040 have been designed to be acceptable for HDMI applications without latch-up. Please refer to Application Note AND9116/D for a more in-depth explanation of latch-up considerations using ESD8000 series devices.

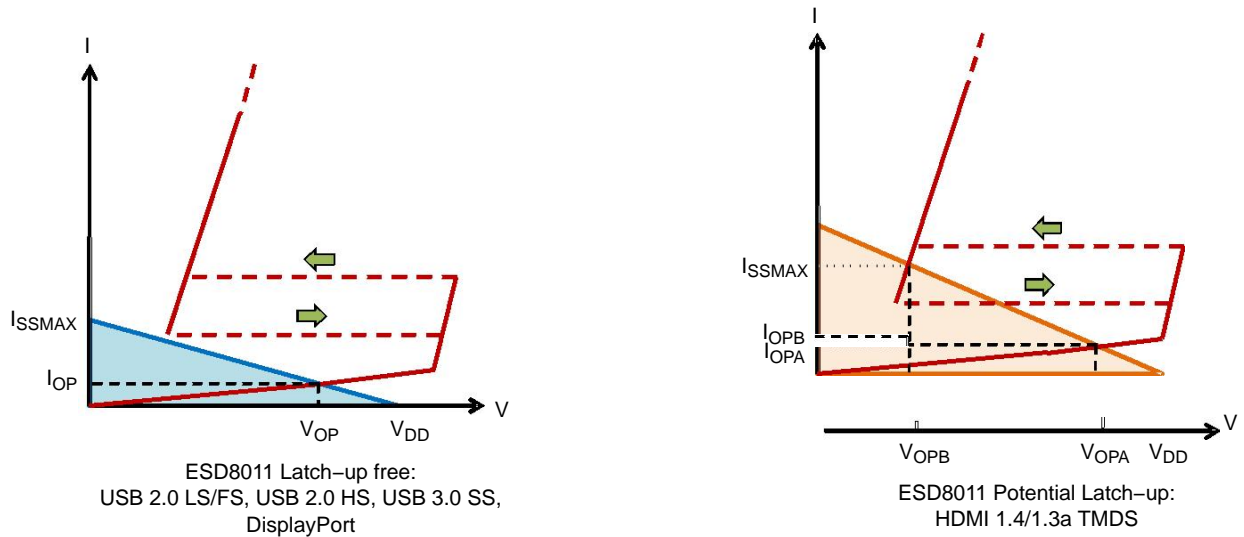


Figure 4. Example Load Lines for Latch-up Free Applications and Applications with the Potential for Latch-up

Table 1. SUMMARY OF SCR REQUIREMENTS FOR LATCH-UP FREE APPLICATIONS

Application	VBR (min)	IH (min)	VH (min)	ON Semiconductor ESD8000 Series
	(V)	(mA)	(V)	Recommended PN
HDMI 1.4/1.3a TMDS	3.465	54.78	1.0	ESD8104, ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004, ESD8011
USB 2.0 HS	0.482	N/A	1.0	ESD8004, ESD8011
USB 3.0 SS	2.800	N/A	1.0	ESD8004, ESD8006, ESD8011
DisplayPort	3.600	25.00	1.0	ESD8004, ESD8006, ESD8011

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

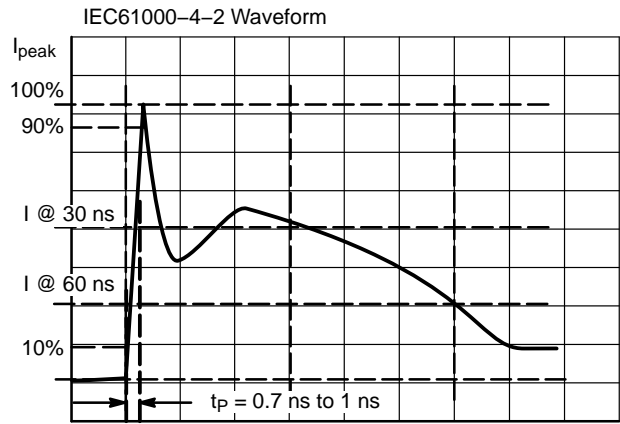


Figure 5. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 6. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 7 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

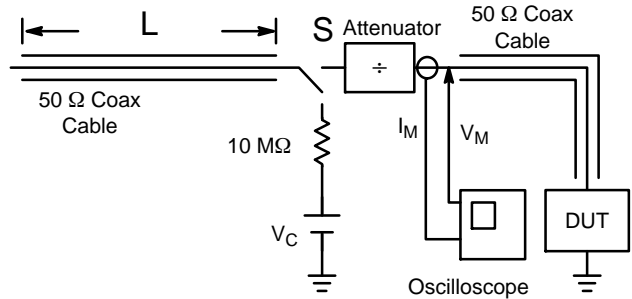


Figure 6. Simplified Schematic of a Typical TLP System

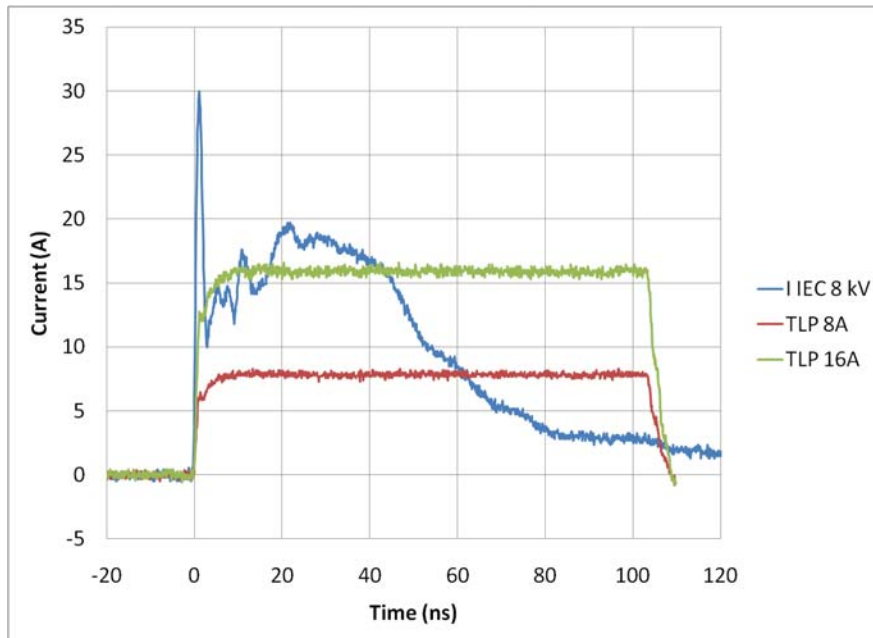


Figure 7. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

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ORDERING INFORMATION

Device	Package	Shipping†
ESD8011MUT5G	X3DFN2 (Pb-Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

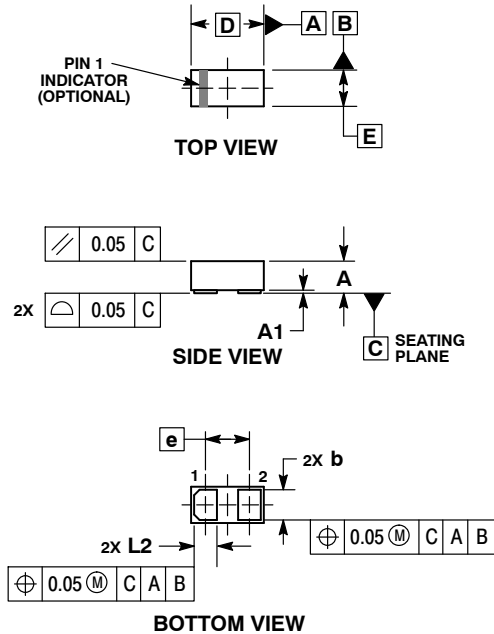
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X3DFN2, 0.62x0.32, 0.355P, (0201)
 CASE 152AF
 ISSUE A


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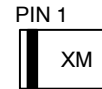
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- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

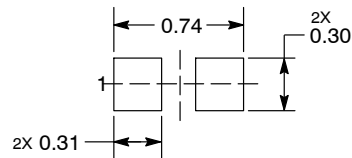
MILLIMETERS		
DIM	MIN	MAX
A	0.25	0.33
A1	---	0.05
b	0.22	0.28
D	0.58	0.66
E	0.28	0.36
e	0.355 BSC	
L2	0.17	0.23

GENERIC MARKING DIAGRAM*



X = Specific Device Code
 M = Date Code


RECOMMENDED MOUNTING FOOTPRINT*



DIMENSIONS: MILLIMETERS

See Application Note AND8398/D for more mounting details
 *For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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