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# LV8860V

Bi-CMOS IC

Fan Motor Driver

## Single-Phase Full-Wave Driver

### Overview

LV8860V is a driver IC used for single-phase fan motor. High-efficiency and low-noise are realized by reducing reactive power using Silent PWM.

The operating range of LV8860V is wide. LV8860V also corresponds to 24V. Therefore, it is optimal for office automation equipment and factory automation equipment.

### Functions

- Single-phase full wave operation by Silent PWM drive.
- Speed is controllable by PWM input.
- Hall bias output pin.
- Integrated Quick Start Circuit.
- FG (rotation detection) / RD (lock detection) output pin (open drain output)
- Integrated current limiter circuit (limit at  $I_O=450\text{mA}$  with  $R_f=0.5\Omega$  connection, limit value is determined based on  $R_f$ .)
- Integrated lock protector circuit and automatic recovery circuit.
- Integrated thermal shut-down (TSD) circuit.

### Specifications

Maximum Ratings at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC\text{ max}}$		36	V
OUT pin output current	$I_{OUT\text{ max}}$		0.7	A
Output withstand	$V_{OUT\text{ max}}$		36	V
RD/FG output pin withstand	$V_{RD/FG\text{ max}}$		36	V
RD/FG output maximum current	$I_{RD/FG\text{ max}}$		10	mA
RGL output maximum current	$I_{RGL\text{ max}}$		5	mA
HB output maximum current	$I_{HB\text{ max}}$		10	mA
PWM input pin withstand	$V_{PWM\text{ max}}$		6	V
Allowable power dissipation	$P_d\text{ max}$	* On a specified board	0.8	W
Operating temperature	$T_{opr}$		-40 to +95	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

\*Specified board: 114.3mm × 76.1mm × 1.6mm fiberglass epoxy printed circuit board

Caution 1) Absolute maximum ratings represent the value which cannot be exceeded for any length of time.

Caution 2) Even when the device is used within the range of absolute maximum ratings, as a result of continuous usage under high temperature, high current, high voltage, or drastic temperature change, the reliability of the IC may be degraded. Please contact us for the further details.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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## Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Operating supply voltage range	V <sub>CC op1</sub>	Recommended supply voltage range	7 to 34	V
	V <sub>CC op2</sub>	Boot guarantee supply voltage range	6 to 34	V
Hall input common phase input voltage range	V <sub>ICM</sub>		0.3 to VRGL-2.0	V
SSW pin input voltage range	SSW		1.0 to 3.0	V
Input PWM frequency range	PWMF		20 to 50	kHz

## Electrical Characteristics at Ta = 25°C, V<sub>CC</sub> = 24V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit consumption current	I <sub>CC</sub>	Active		2.2	3.5	mA
	I <sub>CC<sup>o</sup></sub>	Stand-by		1.7	2.7	mA
RGL pin output voltage	VRGL		4.7	5.0	5.3	V
RGH pin output voltage	VRGH		V <sub>CC</sub> -4.3	V <sub>CC</sub> -4.8	V <sub>CC</sub> -5.3	V
HB pin output voltage	VHB	IHB=5mA	1.16	1.25	1.28	V
Output ON resistance	R <sub>on</sub>	I <sub>O</sub> =0.3A, upper and lower ON resistance		1.4	2.0	Ω
Hall input bias current	IHIN				1.0	μA
Current limiter	VRF		200	225	250	mV
PWM pin input Low level	VPWML		0		1.0	V
PWM pin input High level	VPWMH		2.5		VRGL	V
PWM input minimum pulse width	TPWM			2		μs
RD/FG output pin Low voltage	VRD/FG	I <sub>RD/FG</sub> =3mA		0.22	0.3	V
FG output leakage current	IRDL/FGL	V <sub>RD/FG</sub> =24V			10	μA
FG comparator hysteresis width	ΔVHYS	including offset	±5	±12	±18	mV
Output ON time in Lock-detection	TACT		0.74	0.95	1.16	sec
Output OFF time in Lock-detection	TDET		7.0	9.0	11.0	sec
Output ON/OFF ratio in Lock-detection	TRTO	TRTO=TDET/TACT	7.5	9.0	11.0	
Thermal shutdown operating temperature	TSD	* Design guarantee		180		°C
Thermal shutdown hysteresis width	ΔTSD	* Design guarantee		40		°C

\* Design guarantee: Signifies target value in design. These parameters are not tested in an independent IC.

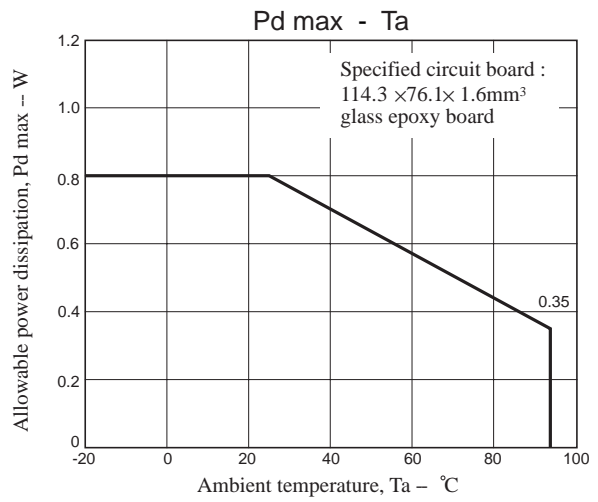
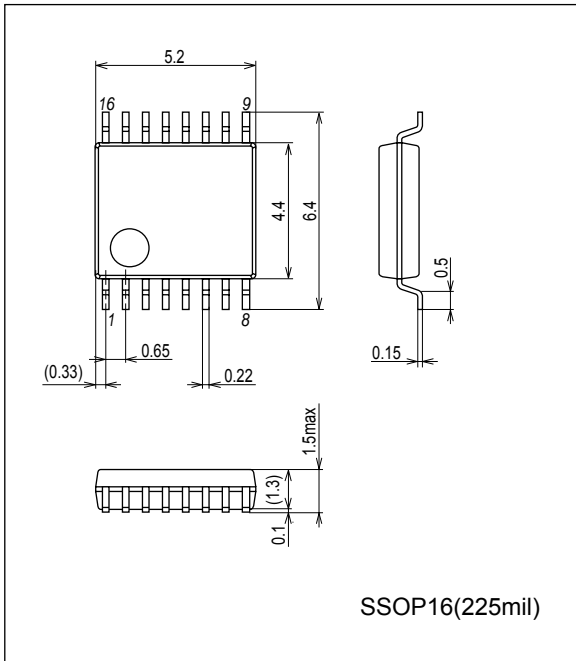
## Truth table

Operating state	IN1	IN2	PWM	OUT1	OUT2	FG	RD
Rotation – drive mode	H	L	H	H	L	L	L
	L	H		L	H	OFF	L
Rotation – regeneration mode	H	L	L	L	L	L	L
	L	H		L	L	OFF	L
Stand-by mode	-	-	L	L	OFF	OFF	L
Lock protector	H	L	-	OFF	L	L	OFF
	L	H		L	OFF	OFF	OFF

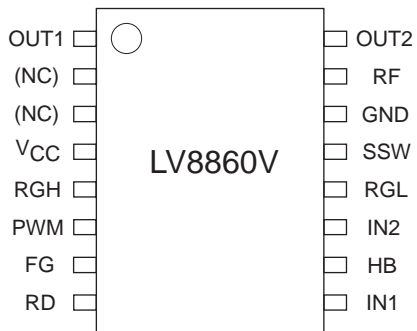
# LV8860V

## Package Dimensions

unit : mm (typ)  
3178B

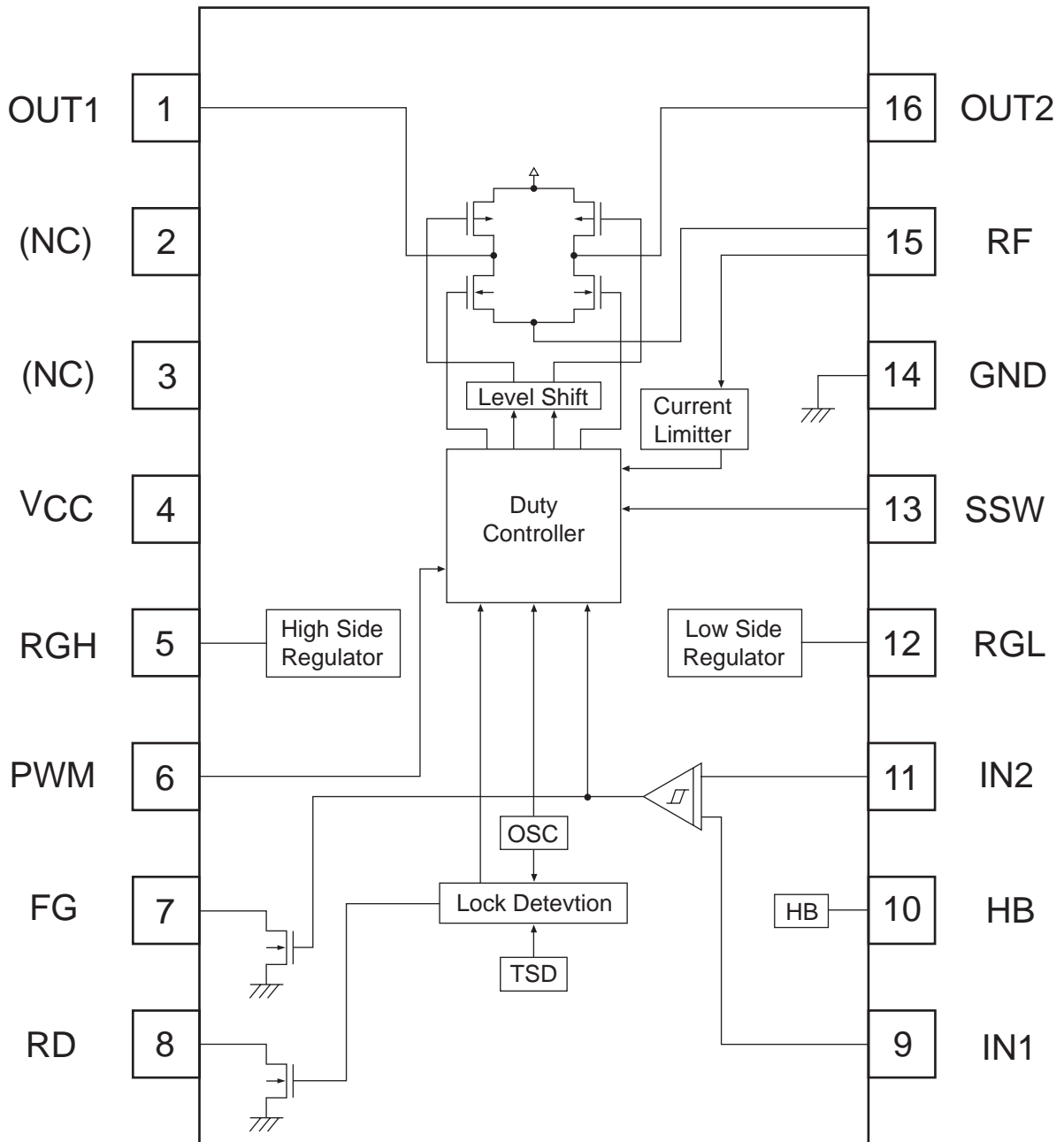


## Pin Assignment



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## Block Diagram



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## PIN function

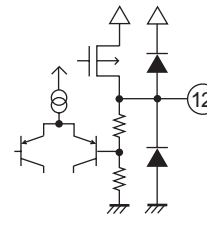
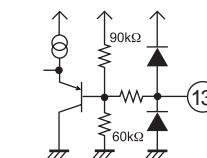
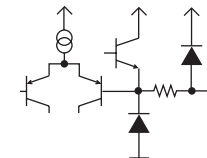
\*On circuit board,  $\nabla$  means  $V_{CC}$ ,  $\uparrow$  means RGL.

NO.	Pin name	Function	Equivalent circuit
1	OUT1	Output pin for motor driver	
16	OUT2		
2	NC	No connect pin	
3	NC	No connect pin	
4	$V_{CC}$	Power supply pin	
5	RGH	Regulator voltage output pin for the upper output Tr driver	
6	PWM	Input pin for PWM control * OPEN: pull up to High * When input is High → output is High When input is Low → output is Low	
7	FG	FG (rotation detection) pulse output pin	
8	RD	RD (lock detection) signal output pin * During rotation → output is Low During lock → output is High	
9	IN1	Hall input + pin	
11	IN2	Hall input - pin	
10	HB	Hall bias output pin	

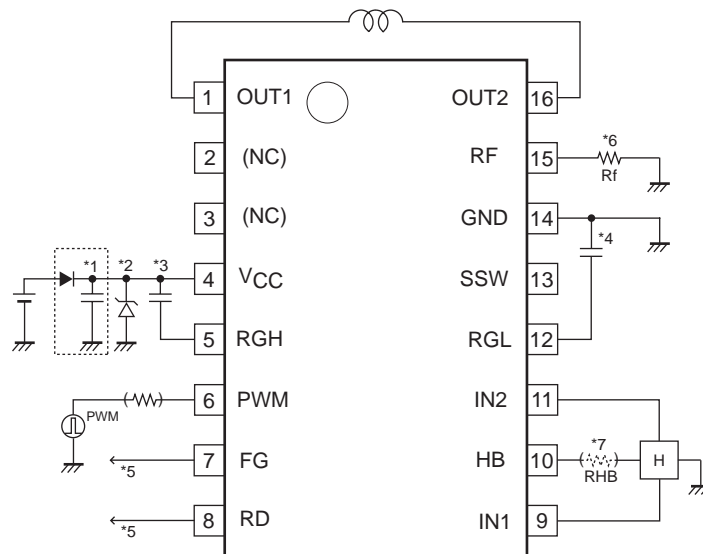
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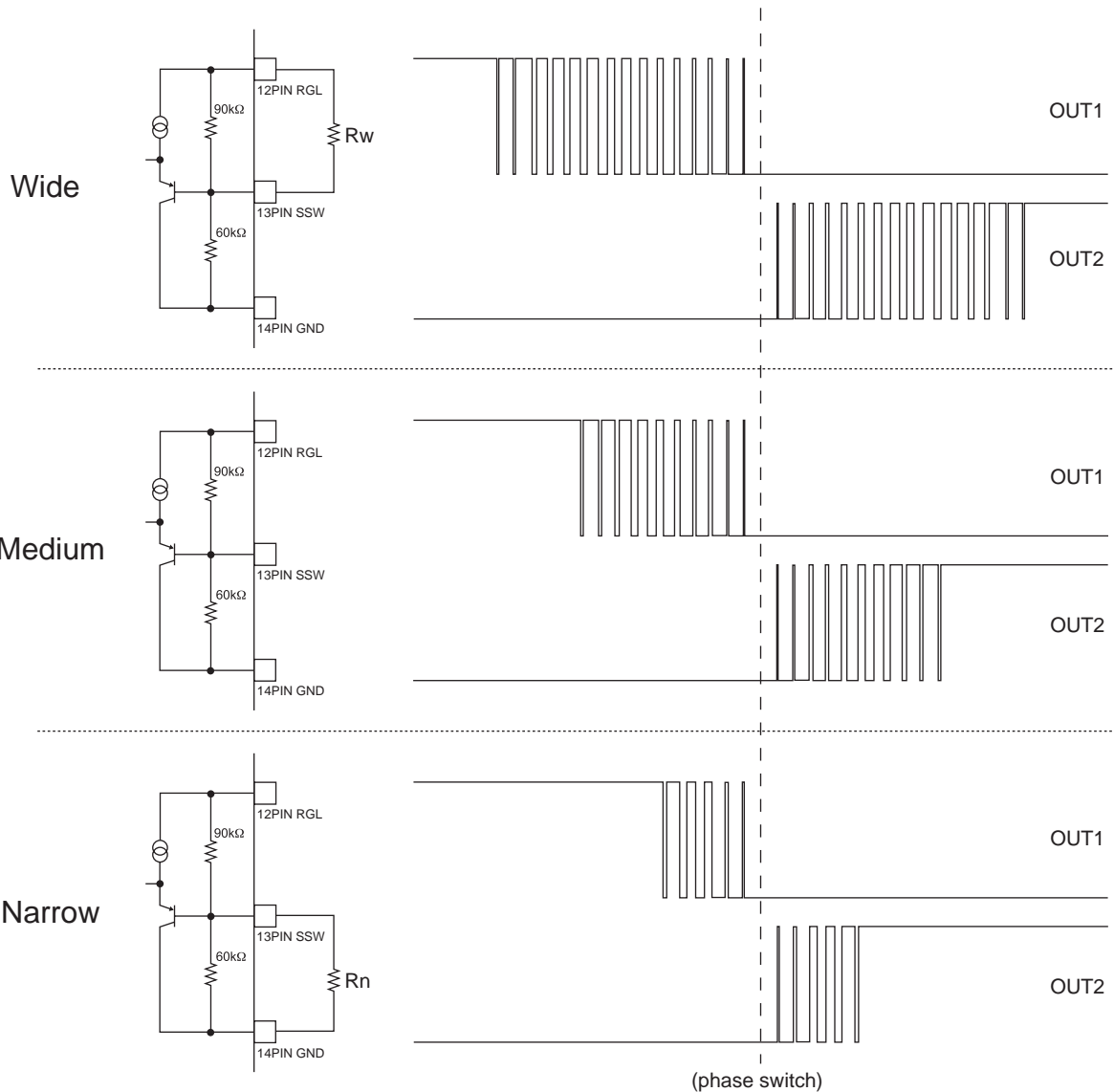
NO.	Pin name	Function	Equivalent circuit
12	RGL	Regulator voltage output pin for internal circuit and lower output Tr driver	
13	SSW	Voltage input pin for control between soft switches * OPEN: pin voltage is 2V * Soft switch zone is changed by connecting a resistance to RGL or GND to adjust pin voltage.	
14	GND	Ground pin	
15	RF	Resistive connection pin for current limiter	

## Sample Application Circuit



- \*1 When diode  $D_1$  is used to prevent destruction of IC from reverse connection, make sure to implement capacitor  $C_1$  to secure regenerative current route.
- \*2 If kickback at a phase change is greater, insert zener diode between GND and  $V_{CC}$  or implement the larger capacitor between GND and  $V_{CC}$  mentioned in \*1
- \*3 Make sure to implement enough capacitance  $0.1\mu\text{F}$  or greater between RGH pin and  $V_{CC}$  pin for stable performance.
- \*4 Make sure to implement enough capacitance  $0.1\mu\text{F}$  or greater between RGL pin and GND pin for stable performance.
- \*5 FG pin and RD pin are open drain output. Keep the pins open when unused.
- \*6 The current limiter is activated when the current detection resistor voltage exceeds 225mV between RF and GND. Where  $R_f=0.5\Omega$ , current limiter is activated at  $I_O=450\text{mA}$ . Setting is made using  $R_f$  resistance.
- \*7 Hall element outputs stable hall signal with good temperature characteristic when it is biased with constant voltage from HB pin. If you wish to alleviate heating of IC, do not use HB pin. When you do not use this Pin (Pin HB), pull down with resistor of around  $10\text{k}\Omega$  (recommended).

Adjustment of a direction between soft switches



LV8860V realizes high efficiency and low noise by controlling reactive power using soft switch before and after phase switch by variable PWM-duty.

The width of soft switch before and after switching is controlled by SSW pin voltage. Therefore, it is adjustable by connecting an external resistance to SSW. Adjustment voltage range is between 1V and 3V.

\* Without adjustment (SSW is open \* this is a reference width of soft switch)

... with IC's internal resistance:  $V_{SSW} = 5 \times 60k / (90k + 60k) = 2V$

\* To widen width of soft switch (connect  $R_w$  (resistance) between RGL and SSW.)

...  $V_{SSW} = 5 \times 60k / (60k + 1 / (1/R_w + 1/90k))$

ex.) Connect  $R_w = 75k\Omega$

$V_{SSW} = 5 \times 60k / (60k + 1 / (1/75k + 1/90k)) = 2.97V$

\* To narrow soft switch width (connect  $R_n$  (resistance) between SSW and GND.)

...  $V_{SSW} = 5 \times ((1 / (1/R_n + 1/60k)) / (90k + 1 / (1/R_n + 1/60k)))$

ex.) Connect  $R_n = 39k\Omega$

$V_{SSW} = 5 \times ((1/(1/39k + 1/60k)) / (90k + 1 / (1/39k + 1/60k))) = 1.04V$

## Setting value of input signal amplitude

The width of soft switch in LV8860V is controlled by input signal, IN1/IN2. The difference of input voltage ( $V_{INp-p}$ ) that creates width of soft switch is adjustable by SSW voltage (VSSW) of an external pin. The range of SSW input voltage is between 1V and 3V.

Difference of input signal amplitude in VSSW range:

- When VSSW = 1V (min),  $V_{INp-p} = 30\text{mV}$  → make sure to input Hall signal with amplitude difference greater than 30mV.
- When VSSW = 2V (open),  $V_{INp-p} = 90\text{mV}$  → make sure to input Hall signal with amplitude difference greater than 90mV.
- When VSSW = 3V (max),  $V_{INp-p} = 150\text{mV}$  → make sure to input Hall signal with amplitude difference greater than 150mV.

\* When input signal amplitude is greater than  $V_{INp-p}$  (as shown in Fig. A below).

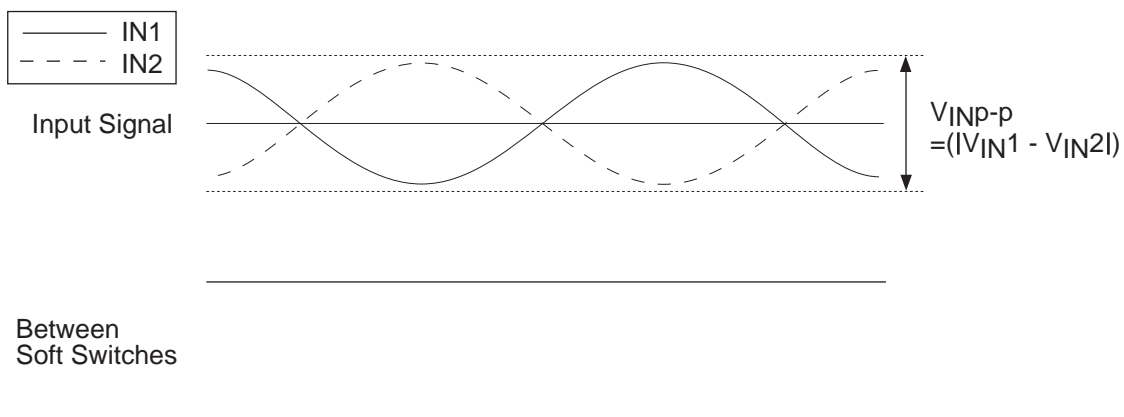
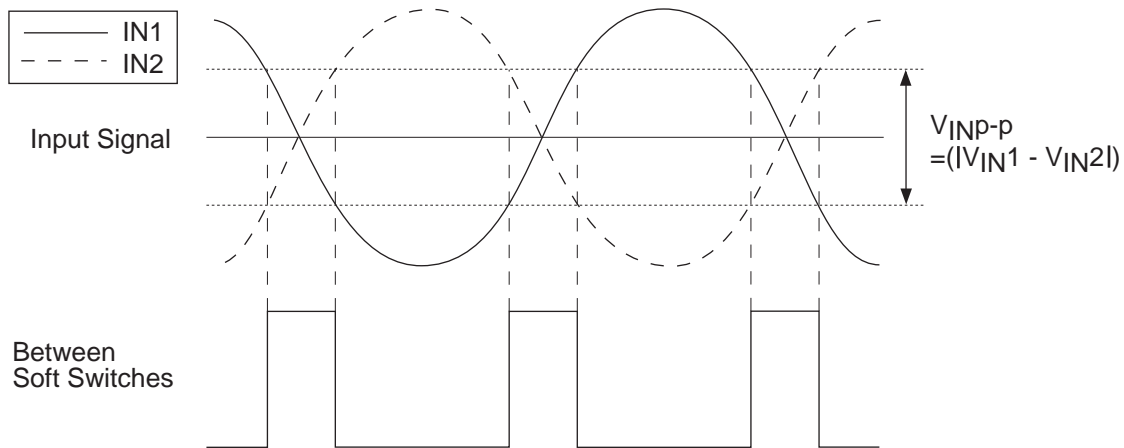
Width of soft switch is defined as shown in Fig. A

\* When input signal amplitude is less than  $V_{INp-p}$  (as shown in Fig. B below).

Since input signal is within the range of  $V_{INp-p}$  in all rotations, the entire zone is the soft switch zone.

Consequently, IC does not operate properly.

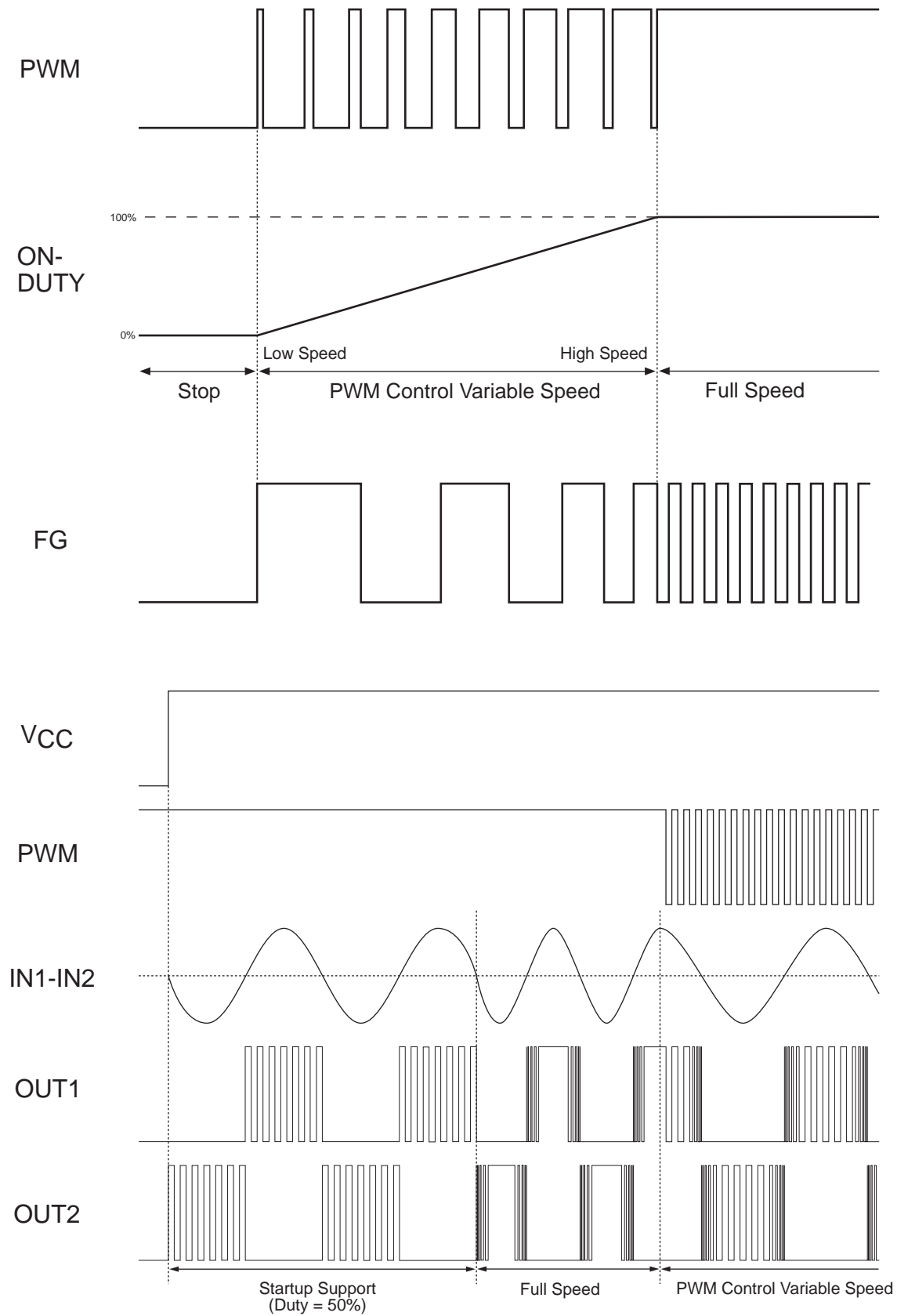
For such reason, make sure to input Hall signal with enough amplitude difference to SSW setting value so that IC operates properly.



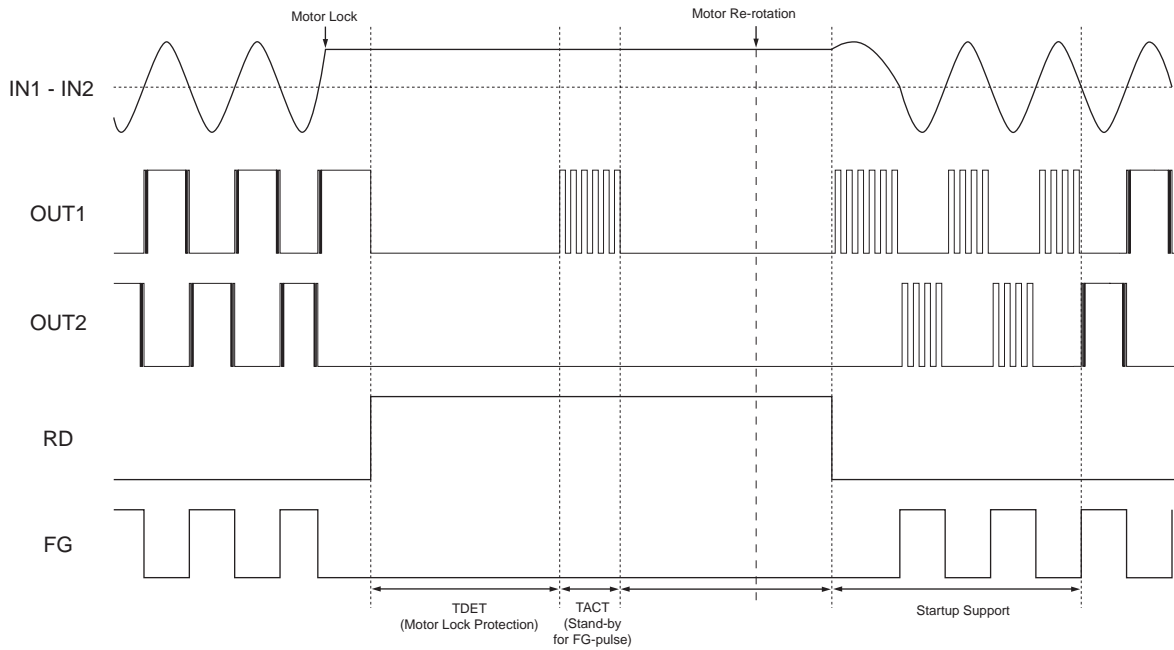


**Description of operation**

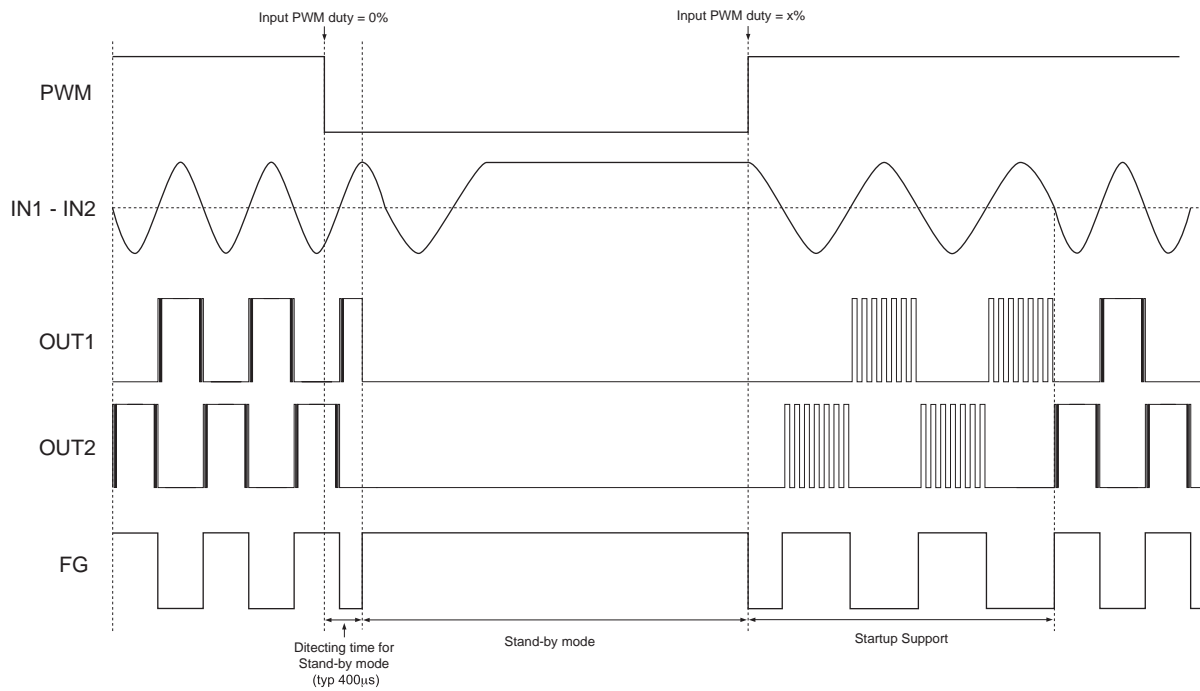
- PWM speed control waveform



• Lock protection operation waveform



• Stand-by mode operation waveform



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