# MUN5232DW1, NSBC143EDXV6, NSBC143EDP6

## Dual NPN Bias Resistor Transistors
## R1 = 4.7 k$\Omega$, R2 = 4.7 k$\Omega$

### NPN Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS
($T_A$ = 25°C, common for $Q_1$ and $Q_2$, unless otherwise noted)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector-Base Voltage | $V_{CBO}$ | 50 | Vdc |
| Collector-Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector Current – Continuous | $I_C$ | 100 | mAdc |
| Input Forward Voltage | $V_{IN(fwd)}$ | 30 | Vdc |
| Input Reverse Voltage | $V_{IN(rev)}$ | 10 | Vdc |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| MUN5232DW1T1G, SMUN5232DW1T1G | SOT−363 | 3,000/Tape & Reel |
| NSBC143EDXV6T1G | SOT−563 | 4,000/Tape & Reel |
| NSBC143EDP6T5G | SOT−963 | 8,000/Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
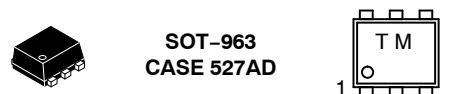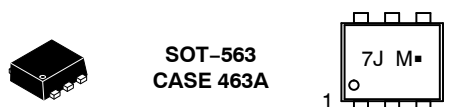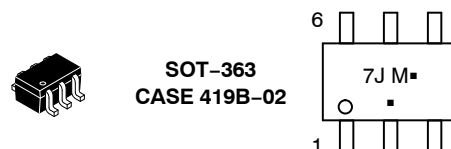
## ON Semiconductor®

### PIN CONNECTIONS



### MARKING DIAGRAMS



SOT−363
CASE 419B−02

SOT−563
CASE 463A

SOT−963
CASE 527AD
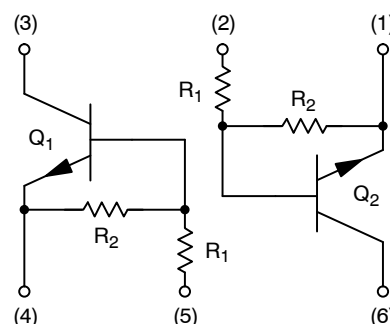
7J/T = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

# MUN5232DW1, NSBC143EDXV6, NSBC143EDP6

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| **MUN5232DW1 (SOT−363) ONE JUNCTION HEATED** | | | |
| Total Device Dissipation<br>  $T_A$ = 25°C     (Note 37)<br>      (Note 38)<br>  Derate above 25°C     (Note 37)<br>      (Note 38) | $P_D$ | 187<br>256<br>1.5<br>2.0 | mW<br><br>mW/°C<br> |
| Thermal Resistance,     (Note 37)<br>  Junction to Ambient     (Note 38) | $R_{\theta JA}$ | 670<br>490 | °C/W |
| **MUN5232DW1 (SOT−363) BOTH JUNCTION HEATED** (Note 39) | | | |
| Total Device Dissipation<br>  $T_A$ = 25°C     (Note 37)<br>      (Note 38)<br>  Derate above 25°C     (Note 37)<br>      (Note 38) | $P_D$ | 250<br>385<br>2.0<br>3.0 | mW<br><br>mW/°C<br> |
| Thermal Resistance,<br>  Junction to Ambient     (Note 37)<br>      (Note 38) | $R_{\theta JA}$ | 493<br>325 | °C/W |
| Thermal Resistance,<br>  Junction to Lead   (Note 37)<br>      (Note 38) | $R_{\theta JL}$ | 188<br>208 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| **NSBC143EDXV6 (SOT−563) ONE JUNCTION HEATED** | | | |
| Total Device Dissipation<br>  $T_A$ = 25°C     (Note 37)<br>  Derate above 25°C     (Note 37) | $P_D$ | 357<br>2.9 | mW<br>mW/°C |
| Thermal Resistance,<br>  Junction to Ambient     (Note 37) | $R_{\theta JA}$ | 350 | °C/W |
| **NSBC143EDXV6 (SOT−563) BOTH JUNCTION HEATED** (Note 39) | | | |
| Total Device Dissipation<br>  $T_A$ = 25°C     (Note 37)<br>  Derate above 25°C     (Note 37) | $P_D$ | 500<br>4.0 | mW<br>mW/°C |
| Thermal Resistance,<br>  Junction to Ambient     (Note 37) | $R_{\theta JA}$ | 250 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| **NSBC143EDP6 (SOT−963) ONE JUNCTION HEATED** | | | |
| Total Device Dissipation<br>  $T_A$ = 25°C     (Note 40)<br>      (Note 41)<br>  Derate above 25°C     (Note 40)<br>      (Note 41) | $P_D$ | 231<br>269<br>1.9<br>2.2 | MW<br><br>mW/°C<br> |
| Thermal Resistance,<br>  Junction to Ambient     (Note 40)<br>      (Note 41) | $R_{\theta JA}$ | 540<br>464 | °C/W |
| **NSBC143EDP6 (SOT−963) BOTH JUNCTION HEATED** (Note 39) | | | |
| Total Device Dissipation<br>  $T_A$ = 25°C     (Note 40)<br>      (Note 41)<br>  Derate above 25°C     (Note 40)<br>      (Note 41) | $P_D$ | 339<br>408<br>2.7<br>3.3 | MW<br><br>mW/°C<br> |
| Thermal Resistance,<br>  Junction to Ambient     (Note 40)<br>      (Note 41) | $R_{\theta JA}$ | 369<br>306 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

37. FR−4 @ Minimum Pad.
38. FR−4 @ 1.0 × 1.0 Inch Pad.
39. Both junction heated values assume total power is sum of two equally powered channels.
40. FR−4 @ 100 mm$^2$, 1 oz. copper traces, still air.
41. FR−4 @ 500 mm$^2$, 1 oz. copper traces, still air.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C, common for $Q_1$ and $Q_2$, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector-Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector-Emitter Cutoff Current ($V_{CE}$ = 50 V, $I_B$ = 0) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter-Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | $I_{EBO}$ | – | – | 1.5 | mAdc |
| Collector-Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector-Emitter Breakdown Voltage (Note 42) ($I_C$ = 2.0 mA, $I_B$ = 0) | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 42) ($I_C$ = 5.0 mA, $V_{CE}$ = 10 V) | $h_{FE}$ | 15 | 30 | – | |
| Collector-Emitter Saturation Voltage (Note 42) ($I_C$ = 10 mA, $I_B$ = 1.0 mA) | $V_{CE(sat)}$ | – | – | 0.25 | V |
| Input Voltage (Off) ($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) | $V_{i(off)}$ | – | 1.2 | – | Vdc |
| Input Voltage (On) ($V_{CE}$ = 0.2 V, $I_C$ = 20 mA) | $V_{i(on)}$ | – | 2.4 | – | Vdc |
| Output Voltage (On) ($V_{CC}$ = 5.0 V, $V_B$ = 2.5 V, $R_L$ = 1.0 kΩ) | $V_{OL}$ | – | – | 0.2 | Vdc |
| Output Voltage (Off) ($V_{CC}$ = 5.0 V, $V_B$ = 0.25 V, $R_L$ = 1.0 kΩ) | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor | R1 | 3.3 | 4.7 | 6.1 | kΩ |
| Resistor Ratio | $R_1/R_2$ | 0.8 | 1.0 | 1.2 | |

42. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.
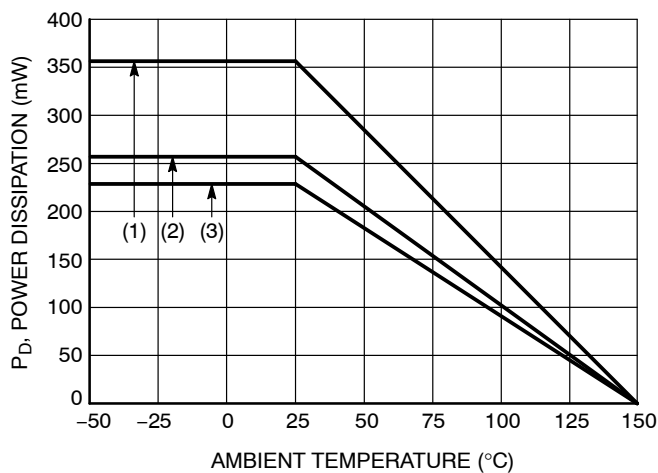


(1) SOT−363; 1.0 × 1.0 Inch Pad
(2) SOT−563; Minimum Pad
(3) SOT−963; 100 mm$^2$, 1 oz. Copper Trace

**Figure 98. Derating Curve**

## TYPICAL CHARACTERISTICS
### MUN5232DW1, NSBC143EDXV6
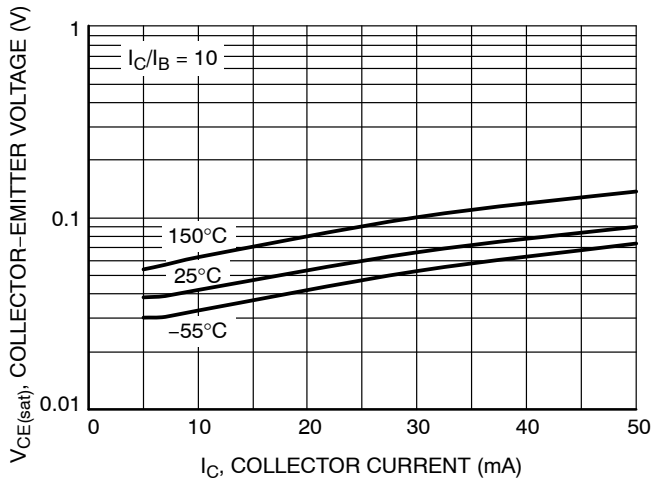
**Figure 99. $V_{CE(sat)}$, vs. $I_C$**
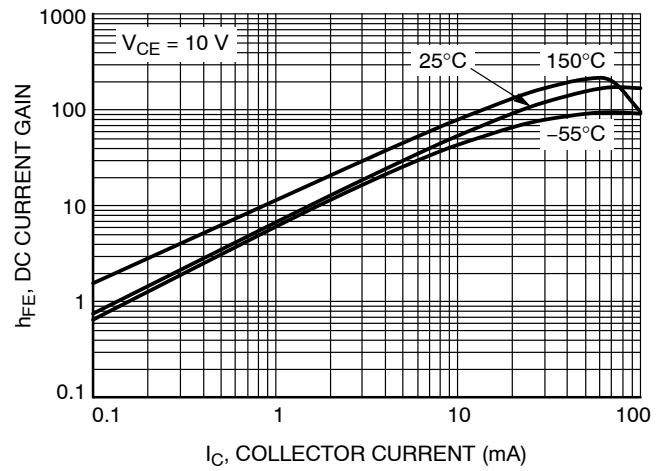
**Figure 100. DC Current Gain**
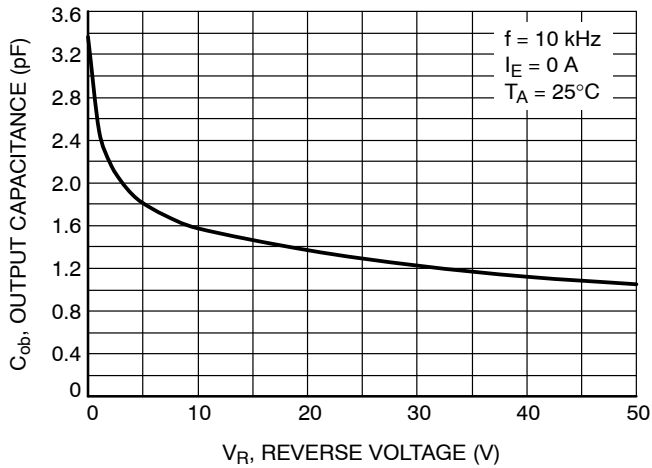
**Figure 101. Output Capacitance**
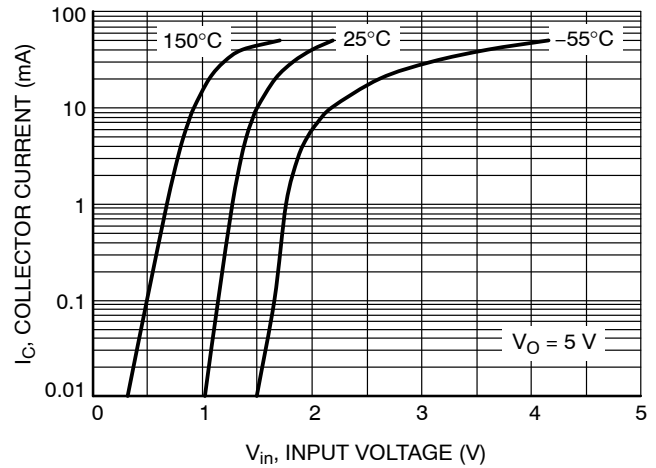
**Figure 102. Output Current vs. Input Voltage**
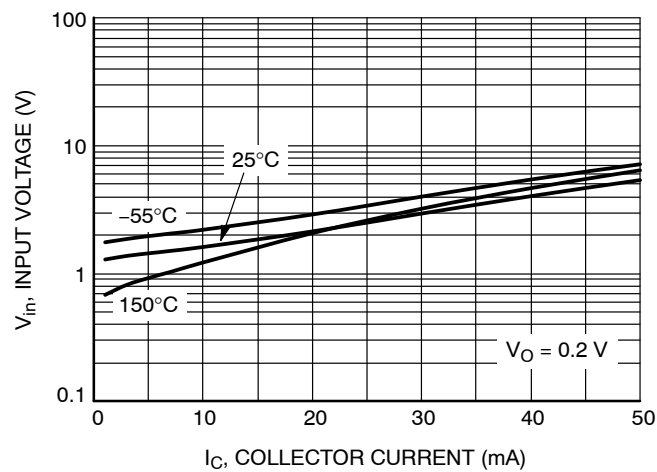
**Figure 103. Input Voltage vs. Output Current**
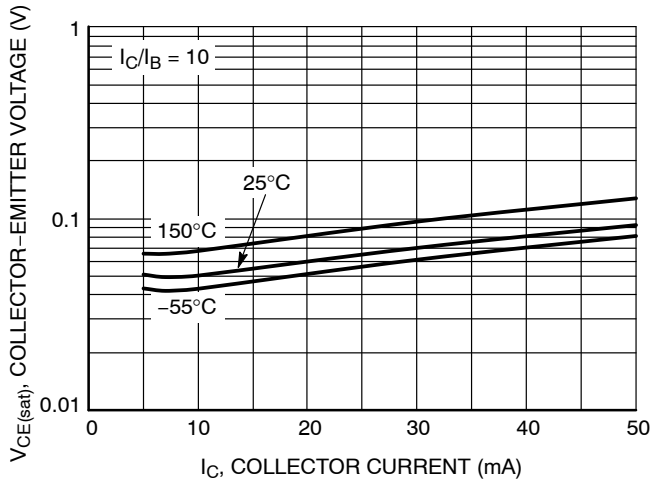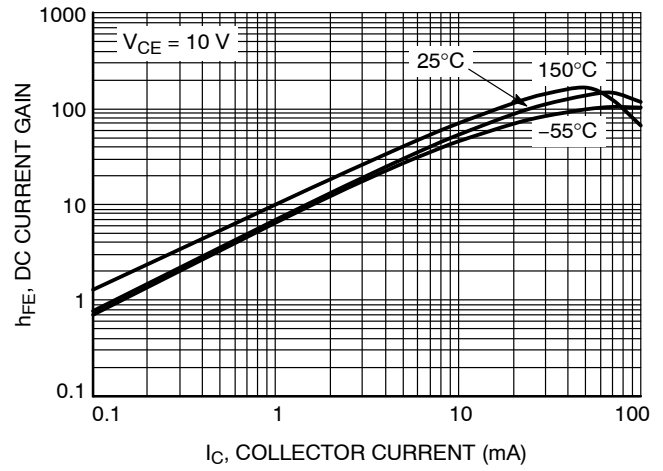
## TYPICAL CHARACTERISTICS
### NSBC143EDP6



**Figure 104. $V_{CE(sat)}$, vs. $I_C$**
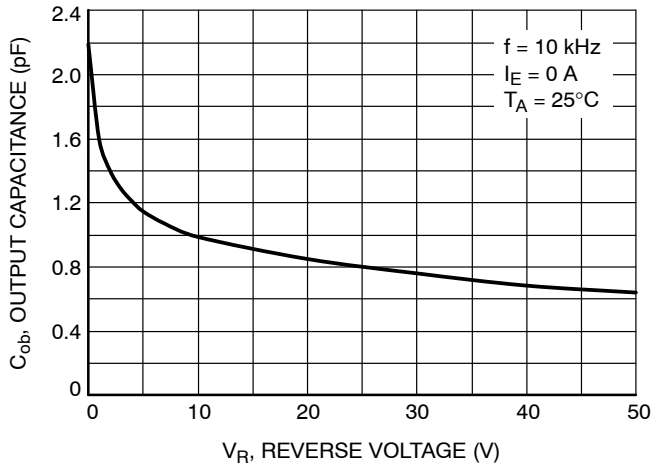


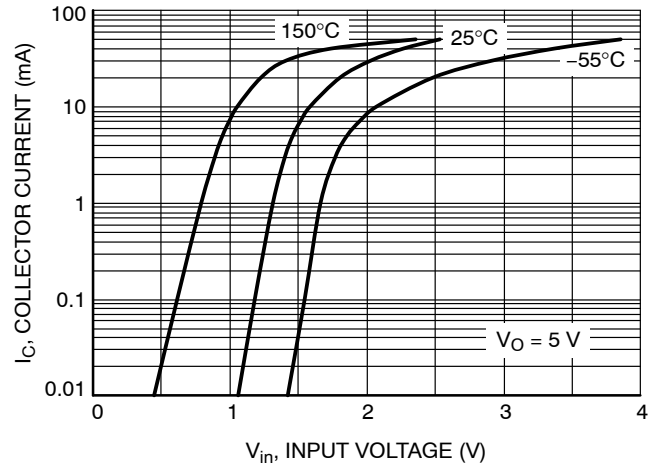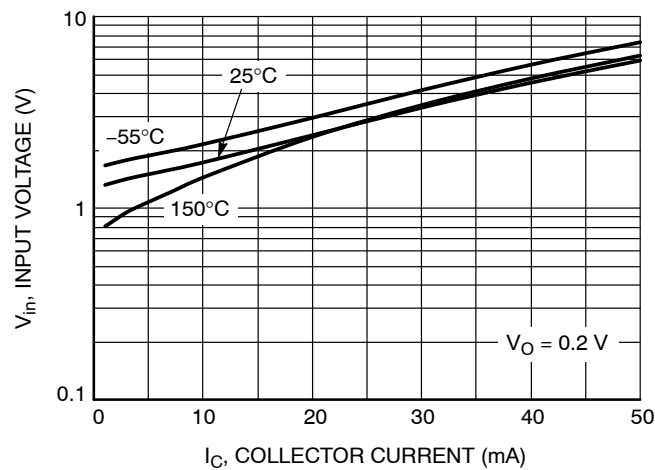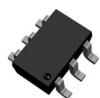**Figure 105. DC Current Gain**



**Figure 106. Output Capacitance**



**Figure 107. Output Current vs. Input Voltage**



**Figure 108. Input Voltage vs. Output Current**

**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

TOP VIEW

SIDE VIEW

END VIEW

DETAIL A
SCALE 2:1

DETAIL A

SEATING PLANE

RECOMMENDED MOUNTING FOOTPRINT*

6X 0.30
6X 0.66
2.50
0.65 PITCH

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*

XXXM▪
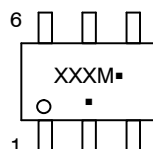
XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| DIM | MILLIMETERS | | |
|-----|------|------|------|
|     | MIN. | NOM. | MAX. |
| A   | − − − | − − − | 1.10 |
| A1  | 0.00 | − − − | 0.10 |
| A2  | 0.70 | 0.90 | 1.00 |
| b   | 0.15 | 0.20 | 0.25 |
| c   | 0.08 | 0.15 | 0.22 |
| D   | 2.00 BSC | | |
| E   | 2.10 BSC | | |
| E1  | 1.25 BSC | | |
| e   | 0.65 BSC | | |
| L   | 0.26 | 0.36 | 0.46 |
| L2  | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |

**STYLES ON PAGE 2**

| DOCUMENT NUMBER: | 98ASB42985B | | |
|---|---|---|---|
| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | | **PAGE 1 OF 2** |

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

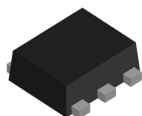| DOCUMENT NUMBER: | 98ASB42985B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | **SC−88 2.00x1.25x0.90, 0.65P** | | **PAGE 2 OF 2** |

SOT−563−6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

DATE 15 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

PIN 1 REFERENCE

TOP VIEW

SIDE VIEW
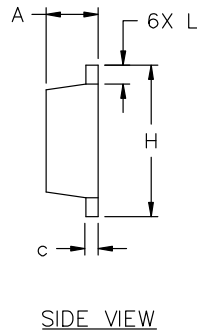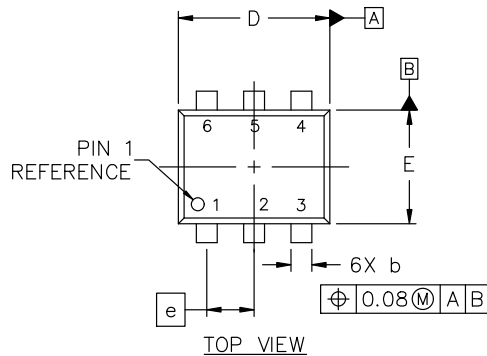
| DIM | MILLIMETERS | | |
|-----|------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.50 | 0.55 | 0.60 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.08 | 0.13 | 0.18 |
| D | 1.50 | 1.60 | 1.70 |
| E | 1.10 | 1.20 | 1.30 |
| e | 0.50 BSC | | |
| H | 1.50 | 1.60 | 1.70 |
| L | 0.10 | 0.20 | 0.30 |

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
   2. BASE 1
   3. COLLECTOR 2
   4. EMITTER 2
   5. BASE 2
   6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
   2. EMITTER 2
   3. BASE 2
   4. COLLECTOR 2
   5. BASE 1
   6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
   2. CATHODE 1
   3. ANODE/ANODE 2
   4. CATHODE 2
   5. CATHODE 2
   6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
   2. COLLECTOR
   3. BASE
   4. EMITTER
   5. COLLECTOR
   6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
   2. CATHODE
   3. ANODE
   4. ANODE
   5. CATHODE
   6. CATHODE

STYLE 6:
PIN 1. CATHODE
   2. ANODE
   3. CATHODE
   4. CATHODE
   5. CATHODE
   6. CATHODE

STYLE 7:
PIN 1. CATHODE
   2. ANODE
   3. CATHODE
   4. CATHODE
   5. ANODE
   6. CATHODE

STYLE 8:
PIN 1. DRAIN
   2. DRAIN
   3. GATE
   4. SOURCE
   5. DRAIN
   6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
   2. GATE 1
   3. DRAIN 2
   4. SOURCE 2
   5. GATE 2
   6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
   2. N/C
   3. CATHODE 2
   4. ANODE 2
   5. N/C
   6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
   2. BASE 2
   3. COLLECTOR 1
   4. EMITTER 1
   5. BASE 1
   6. COLLECTOR 2
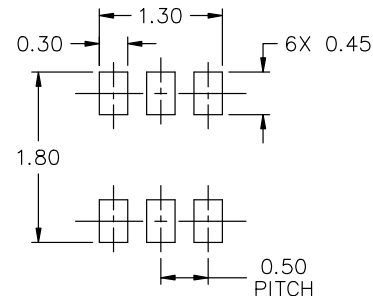
**GENERIC MARKING DIAGRAM***

XXM▪
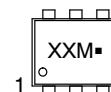
XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| DOCUMENT NUMBER: | 98AON11126D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOT−563−6 1.60x1.20x0.55, 0.50P | PAGE 1 OF 1 |

**SOT−963 1.00x1.00x0.37, 0.35P**
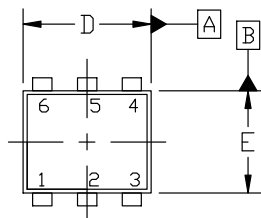CASE 527AD
ISSUE F
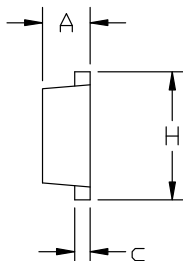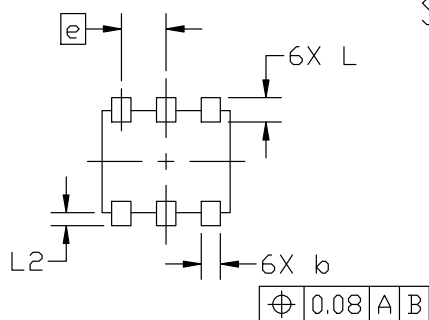
DATE 20 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

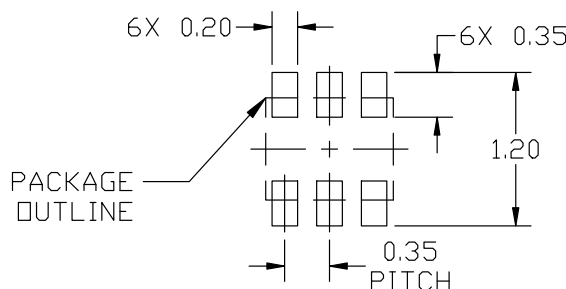| DIM | MILLIMETERS | | |
|-----|------|------|------|
|     | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| c | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.19 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |

TOP VIEW

SIDE VIEW

BOTTOM VIEW

⊕ 0.08 A B

6X 0.20
6X 0.35
1.20
0.35 PITCH

PACKAGE OUTLINE

RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

**GENERIC
MARKING DIAGRAM***

XXM
1
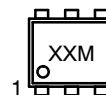
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## ADDITIONAL INFORMATION

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