ON Semiconductor

Design Note – DN05009/D
High Efficiency 3A Buck Regulator w/ Light Load Efficiency

Device	Application	Input Voltage	Output Voltage	Output Current	Topology
NCP3170A	Consumer Electronic	5V & 12V	1.0V-5.0V	3.0A	Buck

Circuit Description

This circuit is proposed for a wide varying +12V input (4.5V-18V) where there is a need to step-down the voltage to various low voltage outputs from 1.0V to 5.0V. The requirement specified optimization of transient performance with only using two 22uF ceramic output capacitors. This design note shows how to utilize Type-III compensation with an OTA to build a high performance power supply. Target efficiency is >80% with a thermally acceptable board temperature.

The NCP3170A is a synchronous PWM switching buck regulator which utilizes current mode control for simple power supply design. The NCP3170A operates from 4.5 V to 18 V, producing up to 3 A, and is capable of producing output voltages as low as 0.8 V. To reduce the number of external components, a number of features are internally set including soft start, power good detection, and switching frequency. The NCP3170A is currently available in an SOIC−8 package.

Key Features

- High Efficiency (90mΩ/25mΩ MOSFETs)
- 4.5 V to 18 V Operating Input Voltage Range
- FMEA Fault Tolerant During Pin Short Test
- Fixed 500 kHz and 1 MHz PWM Operation
- Cycle−by−Cycle Current Monitoring
- PowerGood Pin for Power Sequencing
- Dedicated ENABLE pin
- Turn on Into Pre−bias
- Short Circuit Protection
- Fixed Switching Frequency
- Enhanced Light Load Efficiency

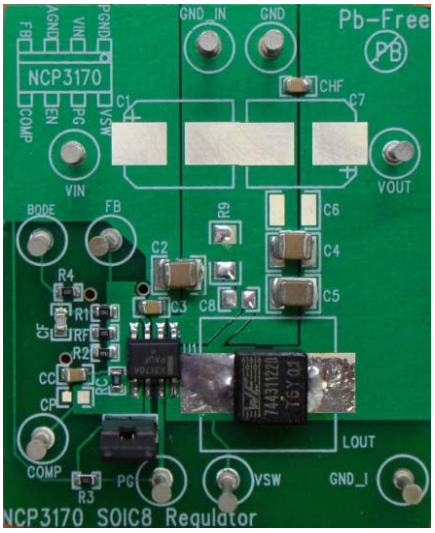

Figure 1: NCP3170A Demonstration PCB

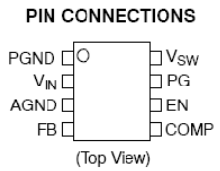

Figure 2: NCP3170A Pinout

Table 1: Pin Description

PIN	PIN NAME	DESCRIPTION
1	PGND	The power ground pin is the high current path for the device. The pin should be soldered to a large copper area to reduce thermal resistance. PGND needs to be electrically connected to AGND.
2	VIN	The input voltage pin powers the internal control circuitry and is monitored by multiple voltage comparators. The VIN pin is also connected to the internal power PMOS switch and linear regulator output. The VIN pin has high di/dt edges and must be decoupled to ground close to the pin of the device.
3	AGND	The analog ground pin serves as small-signal ground. All small-signal ground paths should connect to the AGND pin and should also be electrically connected to power ground at a single point, avoiding any high current ground returns.
4	FB	Inverting input to the OTA error amplifier. The FB pin in conjunction with the external compensation serves to stabilize and achieve the desired output voltage with current mode compensation.
5	COMP	The loop compensation pin is used to compensate the transconductance amplifier which stabilizes the operation of the converter stage. Place compensation components as close to the converter as possible. Connect a RC network between COMP and AGND to compensate the control loop.
6	EN	Enable pin. Pull EN to logic high to enable the device. Pull EN to logic low to disable the device. Do not leave it open.
7	PG	Power good is an open drain 500uA pull down indicating output voltage is within the power good window. If the power good function is not used, it can be connected to the VSW node to reduce thermal resistance. Do not connect PG to the VSW node if the application is turning on into pre-bias.
8	VSW	The VSW pin is the connection of the drains of the internal N and P MOSFETS. At switch off, the inductor will drive this pin below ground as the body diode and the NMOS conducts with a high dv/dt.

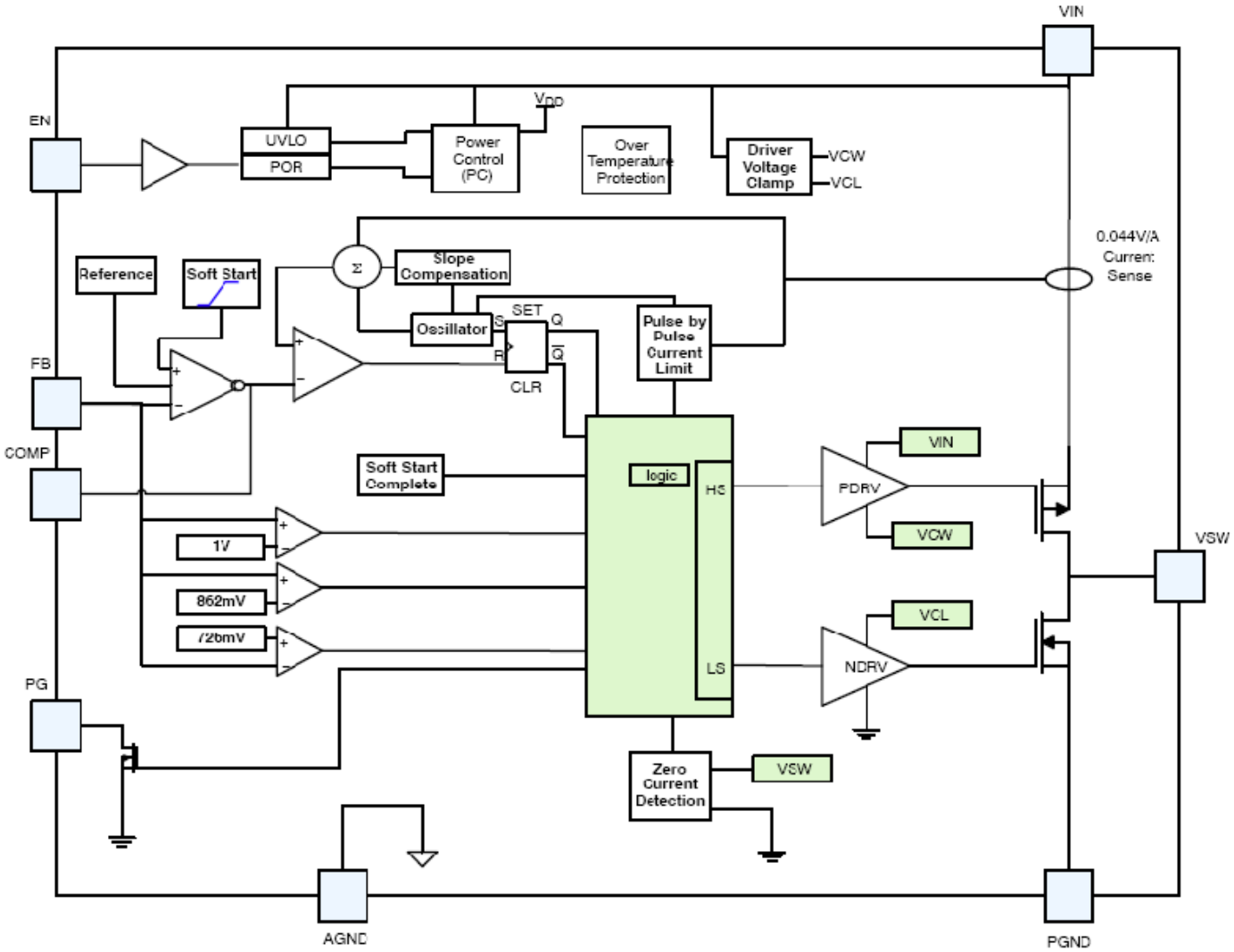

Figure 3: NCP3170A Block Diagram

Circuit Description

The following solution is presented to support DC to DC power needs. The module has an input voltage range from 4.5 V to 18 V. The module provides one regulated output, but configurations are shown for 1.0 V to 5.0 V outputs. If the end-user requires a better transient response than can be obtained by using the OTA in its standard configuration (as shown in Figure 4A), then they can change the configuration to that shown in Figure 4B, where the OTA is treated like an error amplifier. The designer must be careful when using an OTA as an error amplifier in that the output current is much lower than a traditional error amplifier. A traditional error amplifier has a source sink current of 1 mA, where the NCP3170A OTA error amplifier has a source sink current of 20 μA. Since the NCP3170A has a limited source sink current, it is essential to limit the current running in the resistor divider to 10% to 30% of the source sink current of the OTA. To choose an output voltage and limit the resistor divider current, the equations in Figure 5 can be used.

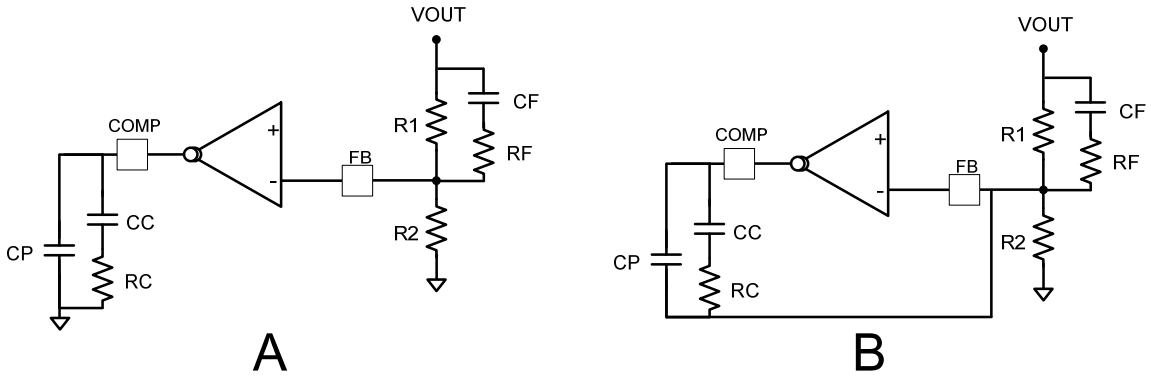

Figure 4: Typical Transconductance Amplifier Configuration A and OTA Configured Like an Error Amplifier B

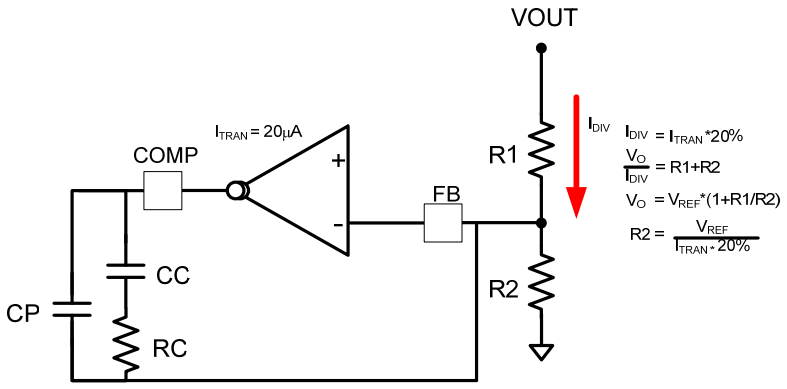

Figure 5: Selection of Resistor Divider Impendence

Performance Information

The following figures show typical performance of the evaluation board.

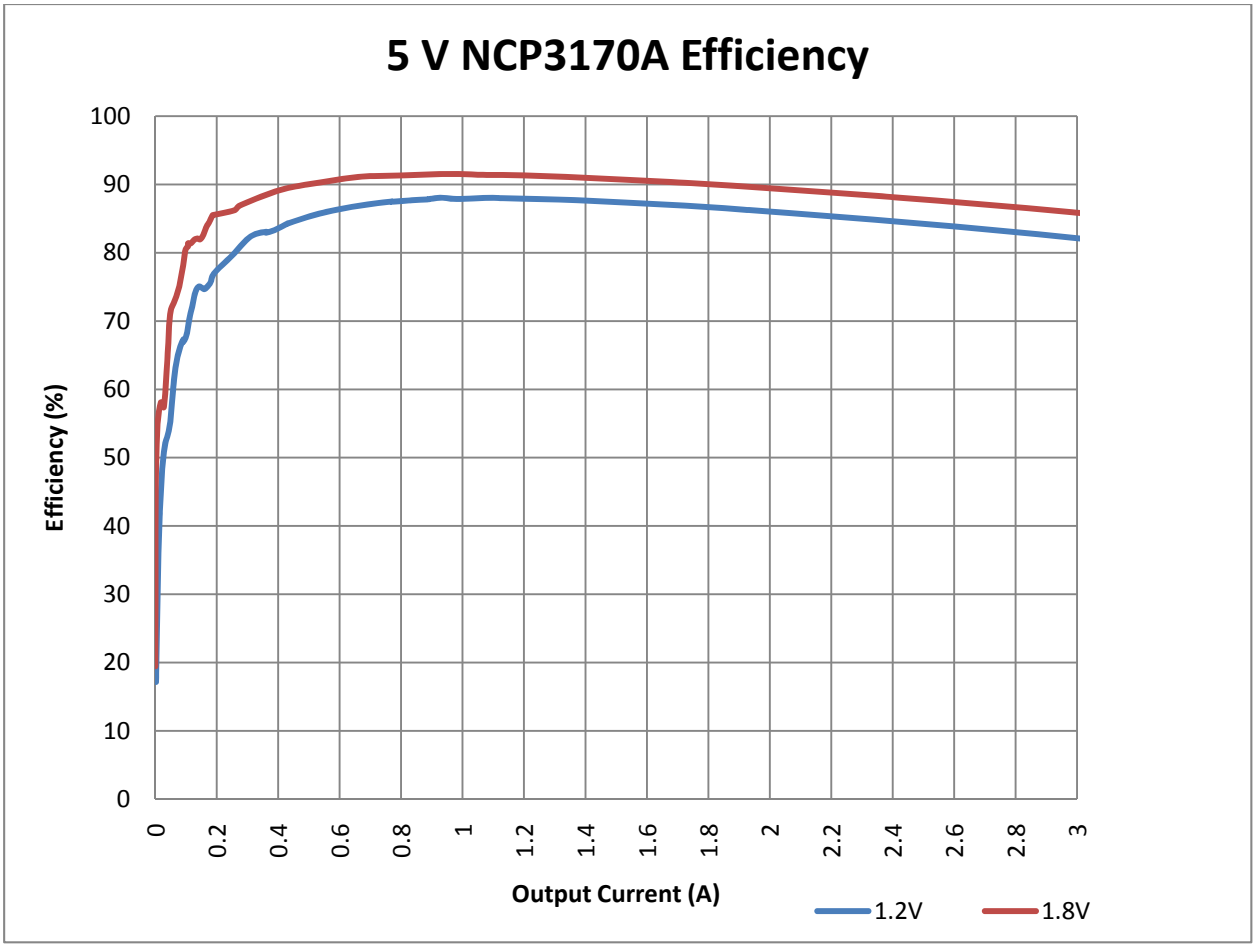

Figure 6: NCP3170A 5 V Efficiency

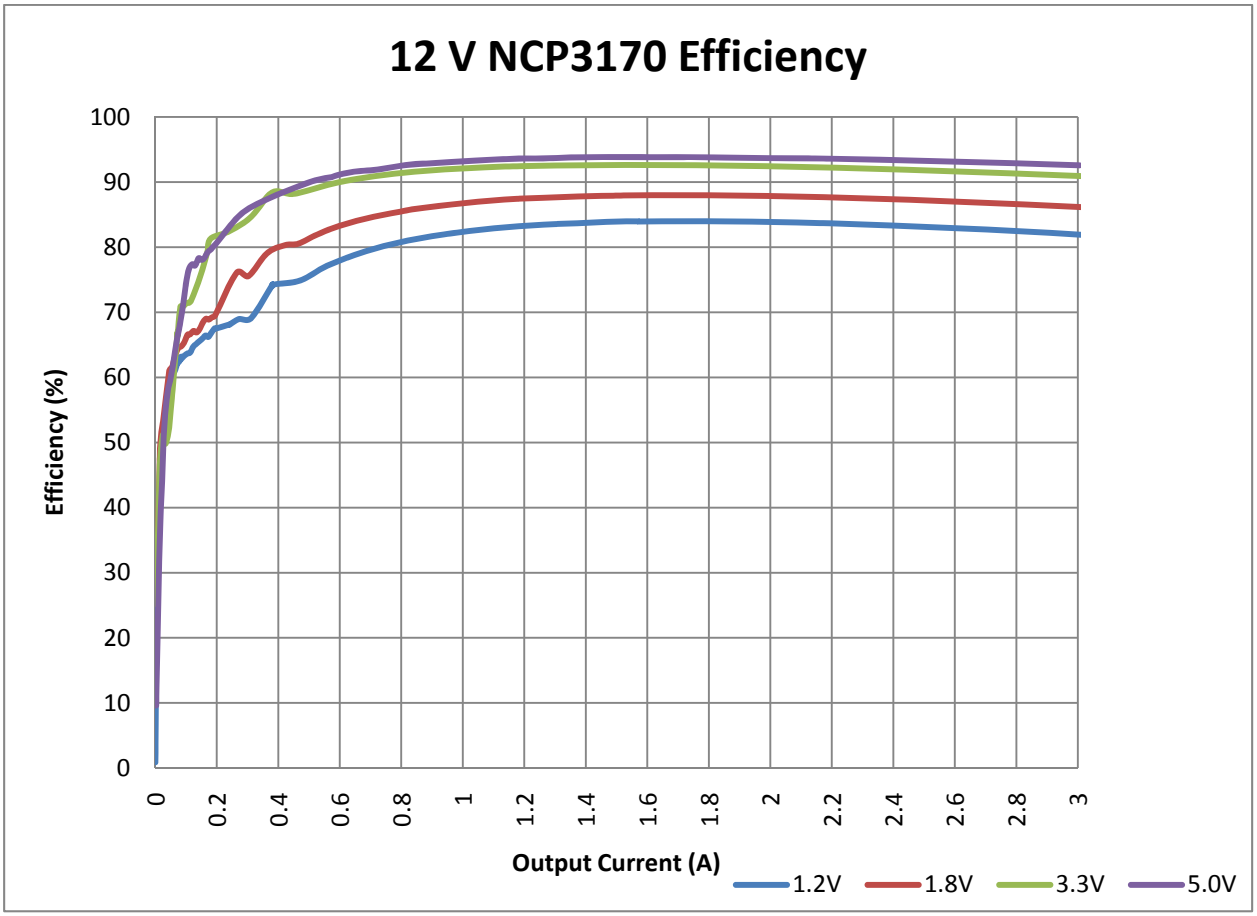

Figure 7: NCP3170A 12 V Efficiency

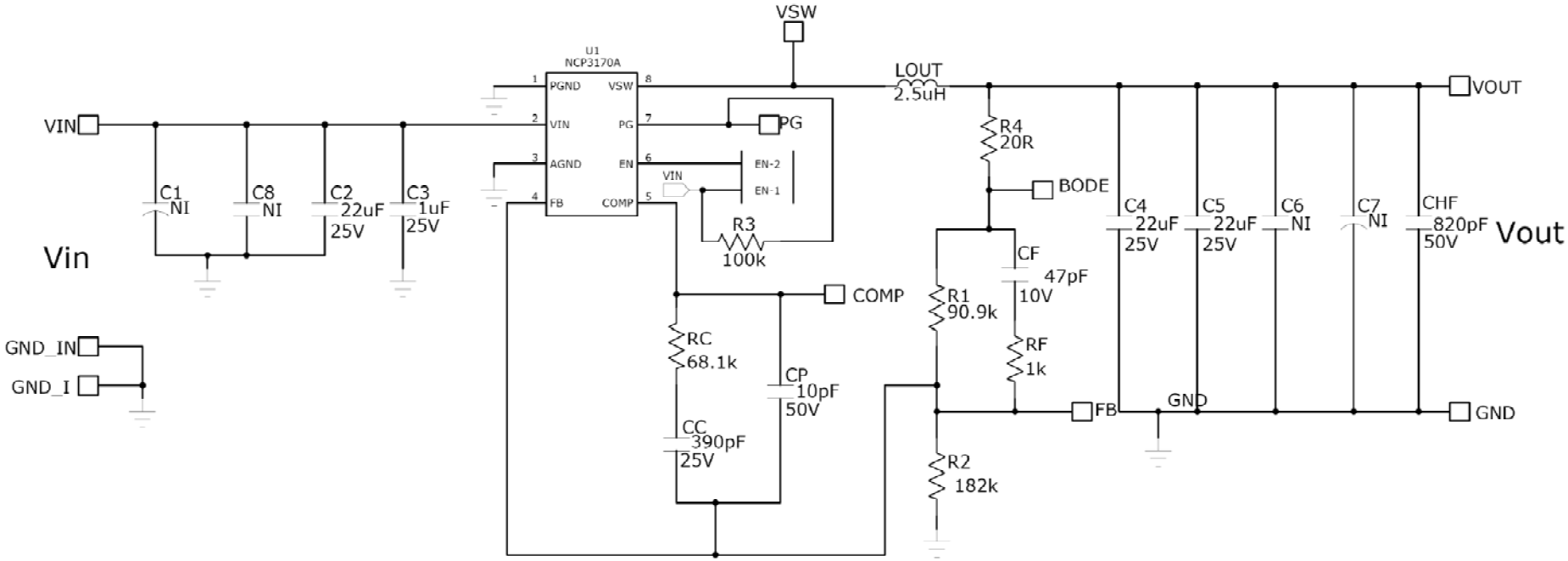

Figure 8: NCP3170A 12 V to 1.2 V Schematic

Table 2: BOM for the NCP3170A 12 V to 1.2 V Design

Reference	Qty	Description	Value	Tolerance	Footprint	Manufacturer	Manufacturer Part Number
C3	1	SMT Ceramic Capacitor	1uF	±10%	603	TDK	C1608X5R1E105K
CF	1	SMT Ceramic Capacitor	150pF	±5%	603	Murata	GRM1885C1H151JA01D
CC	1	SMT Ceramic Capacitor	390pF	±5%	603	TDK	C1608C0G2E391J
CHF	1	SMT Ceramic Capacitor	47pF	±5%	603	AVX	06035A470JAT2A
CP	1	SMT Ceramic Capacitor	10pF	±5%	603	AVX	06035A100JAT2A
C2 C4-5 C8	3	SMT Ceramic Capacitor	22uF	±20%	1210	AVX	12103D226MAT2A
C6	1	SMT Ceramic Capacitor	NI	±10%	1210		
C1	1	Surface Mount E-Cap	NI	±20%	(8mm x 6.2)mm		
C7	1	Surface Mount E-Cap	NI	±20%	(8.3 x 8.3)mm		
LOUT	1	SMT Inductor	2.5uH	20%	(10.2x 10.2 x 6.4)mm	Wurth	7447798250
U1	1	Switching PWM Regulator	500kHz	NA	SOIC8	ON Semiconductor	NCP3170A
R2	1	SMT Resistor	182k	±1.0%	603	Vishay / Dale	CRCW0603182KFKEA
R3	1	SMT Resistor	100k	±1.0%	603	Vishay / Dale	CRCW0603100KFKEA
R4	1	SMT Resistor	20R	±1.0%	603	Vishay / Dale	CRCW060320R0FKEA
RC	1	SMT Resistor	68.1k	±1.0%	603	Vishay / Dale	CRCW060368K1FKEA
R1	1	SMT Resistor	90.9k	±1.0%	603	Vishay / Dale	CRCW060390K9FKEA
RF	1	SMT Resistor	1k	±1.0%	603	Vishay / Dale	CRCW06031K00FKEA

Table 3: BOM Changes to Achieve Desired Output

VIN (V)	V_{out} (V)	C2 (µF)	L_{out} (µH)	Bias Current Percentage (Resistor Divider Current / OTA Maximum Current)	R1 (kΩ)	R2 (kΩ)	Rf (kΩ)	Cf (pF)	Cc (pF)	Rc (kΩ)	Cp (pF)
12	1.0	22 X 1	2.5	20	49.9	200	1	68	390	68.1	10
12	1.1	22 X 1	2.5	20	75	200	1	56	390	68.1	10
12	1.2	22 X 1	2.5	20.2	90.9	182	1	47	390	68.1	10
12	1.5	22 X 1	3.6	20.1	174	200	1	56	220	97.6	10
12	1.8	22 X 1	3.6	19.6	255	205	1	56	220	97.6	10
12	2.5	22 X 1	4.7	19.7	432	200	1	47	150	82.5	12
12	3.3	22 X 1	4.7	19.7	634	200	1	27	100	95.3	12
12	5.0	22 X 1	7.2	26.6	787	150	1	18	68	95.3	12
5	1.0	22 X 1	2.5	20	49.9	200	1	82	390	78.8	6.8
5	1.1	22 X 1	2.5	20	75	200	1	47	220	110	4.7
5	1.2	22 X 1	2.5	20.2	90.9	182	1	47	220	110	6.8
5	1.5	22 X 2	3.6	20.1	174	200	1	47	82	110	8.2
5	1.8	22 X 2	3.6	19.6	255	205	1	47	82	110	10
5	3.3	22 X 3	1.8	19.7	634	200	1	27	47	95.3	12

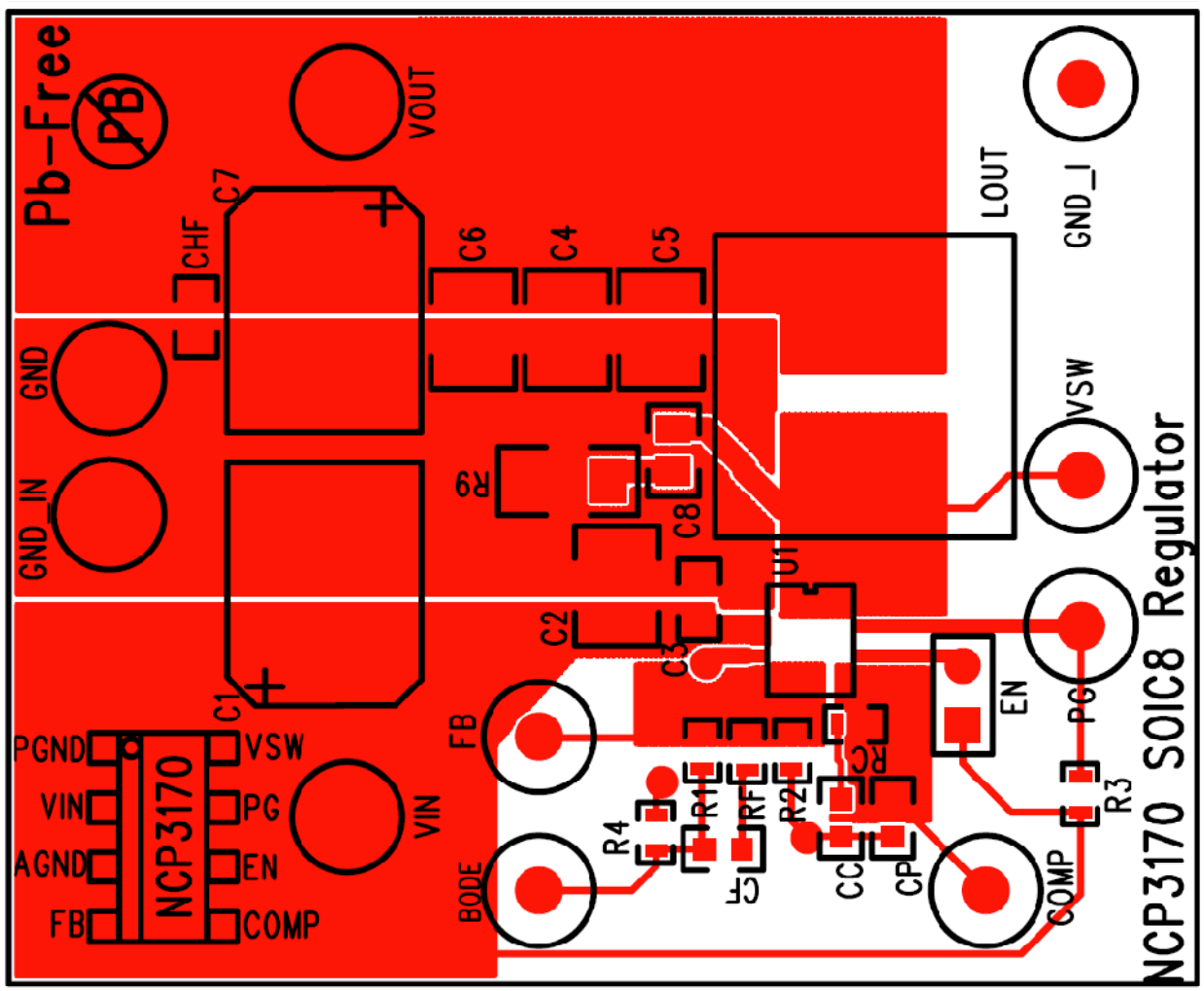

Figure 9: Layout Top

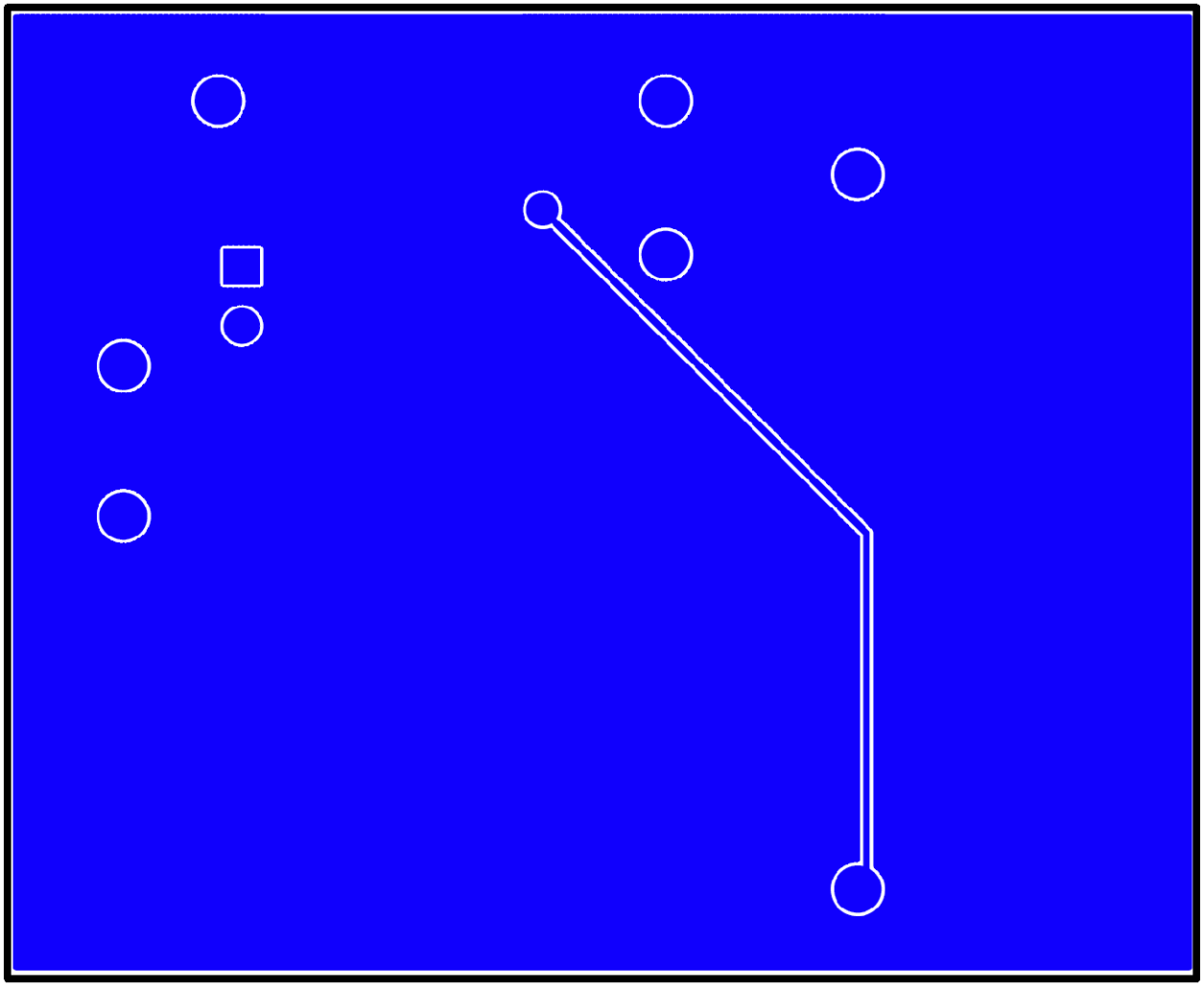

Figure 10: Layout Bottom

Each power supply in Table 3 was stabilized and the resulting frequency response met the stability criteria when measured at a load of 3 A and 1.5 A. Each power supply was then subjected to transient currents that slewed at 2.5 A/µs and the results were recorded for both over shoot and undershoot as shown in Figures 11 and 12. The transient response was taken from 3 A to 100 mA and is recorded for each case in Figures 13 through 27. It is important to note that the transient performance can be improved by increasing the bandwidth or adding output capacitance. The following is an effort to use two 22µF ceramic capacitors while keeping the positive and negative voltage excursions below 20% of the regulated output voltage. The designer could achieve better results be placing more capacitance on the output of the power stage while maintaining the same bandwidth.

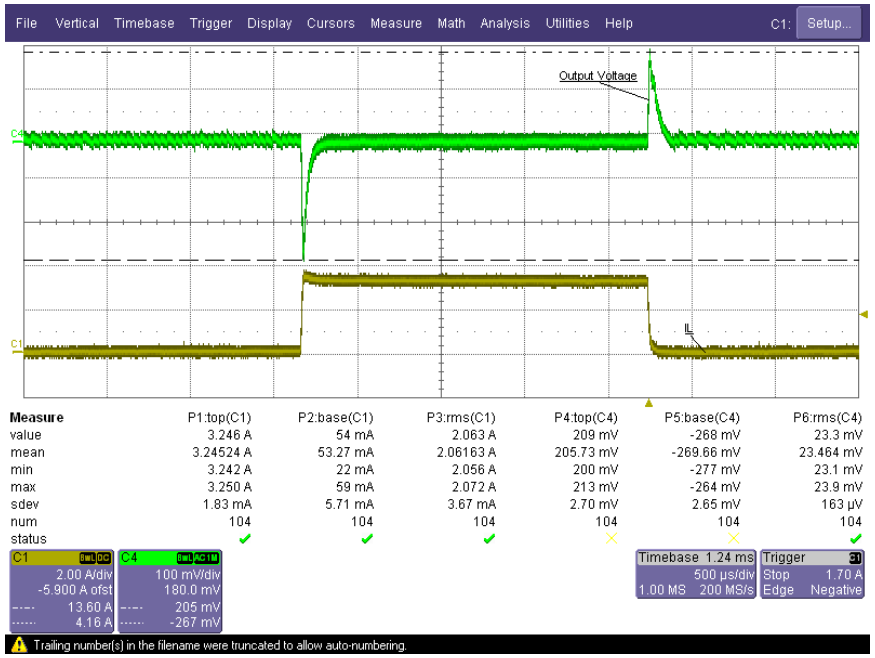

Figure 11: Transient Capture of 12 V to 1.5 V, 0 A to 3 A

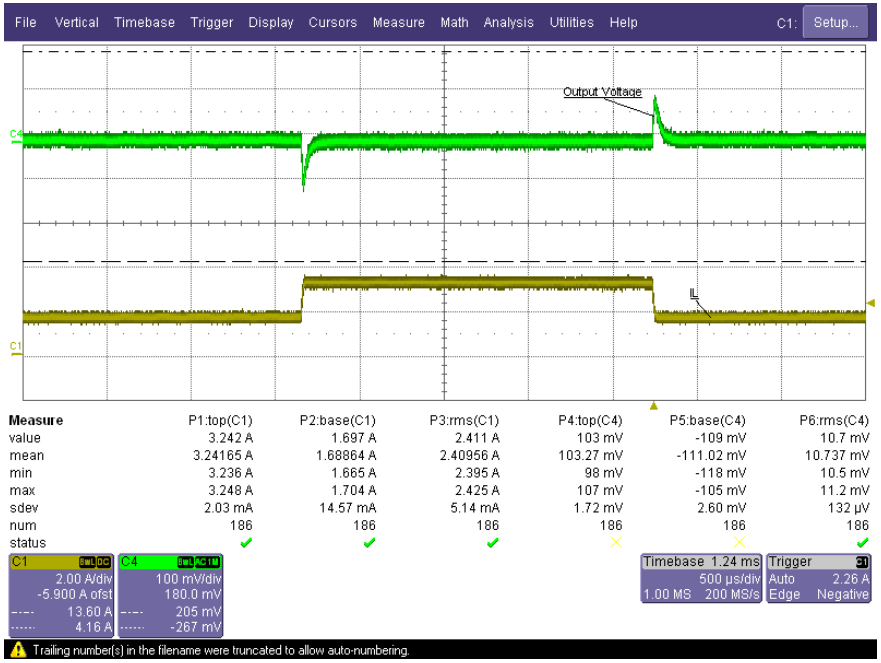

Figure 12: Transient Capture of 12 V to 1.5 V, 1.5 A to 3 A

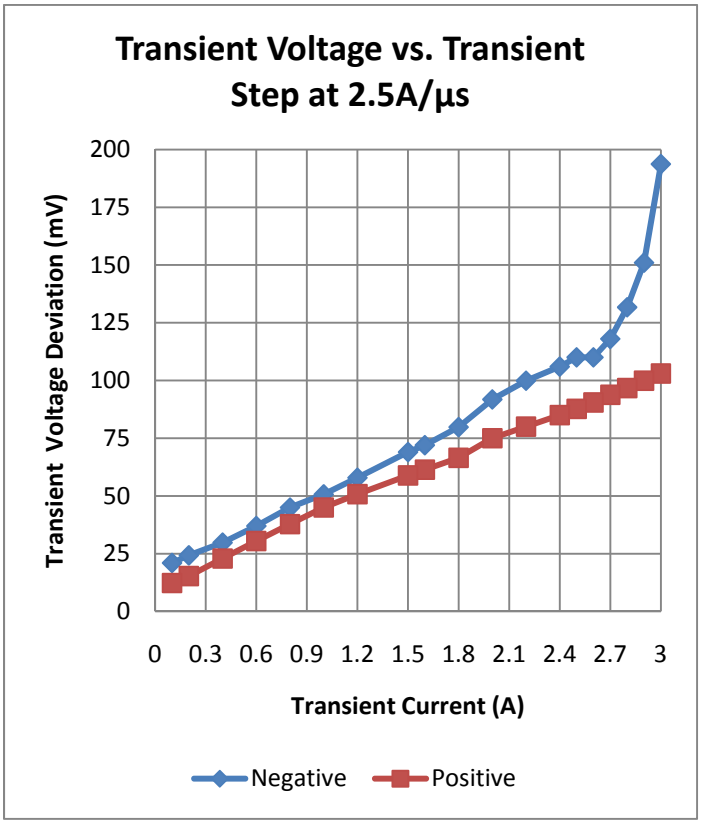

Figure 13: 5 V to 1 V Transient Voltage Graph

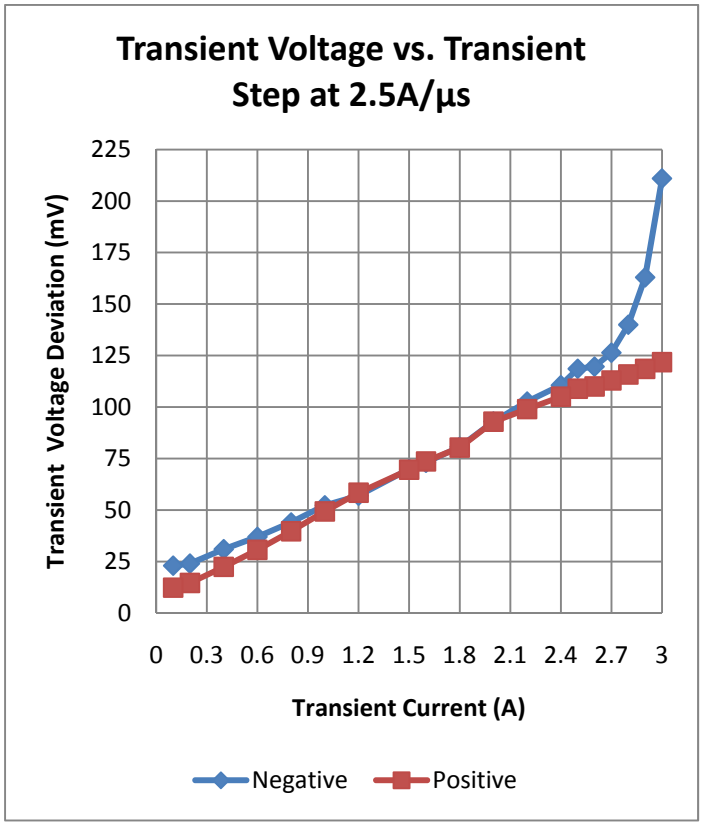

Figure 14: 5 V to 1.1 V Transient Voltage Graph

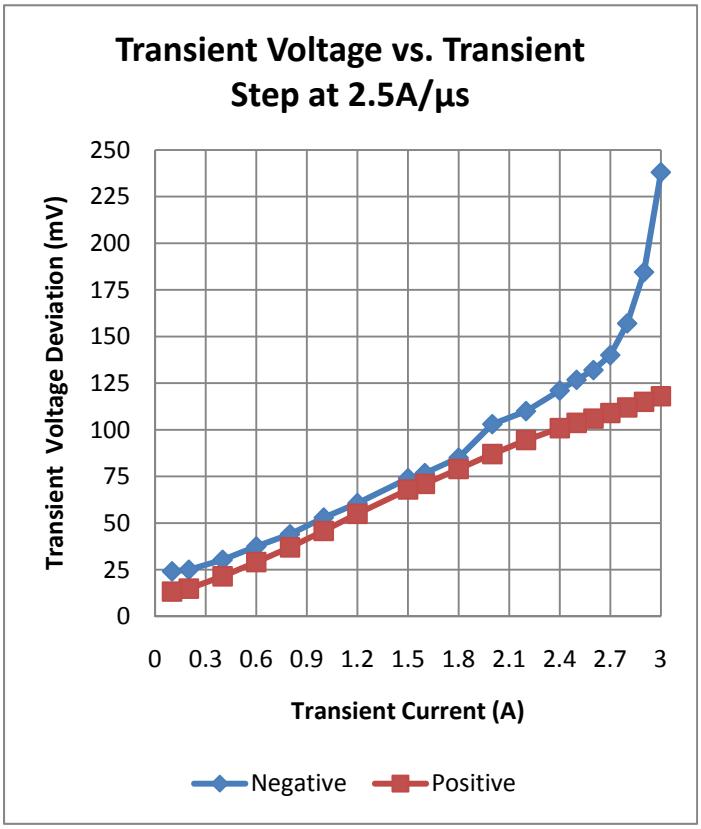

Figure 15: 5 V to 1.2 V Transient Voltage Graph

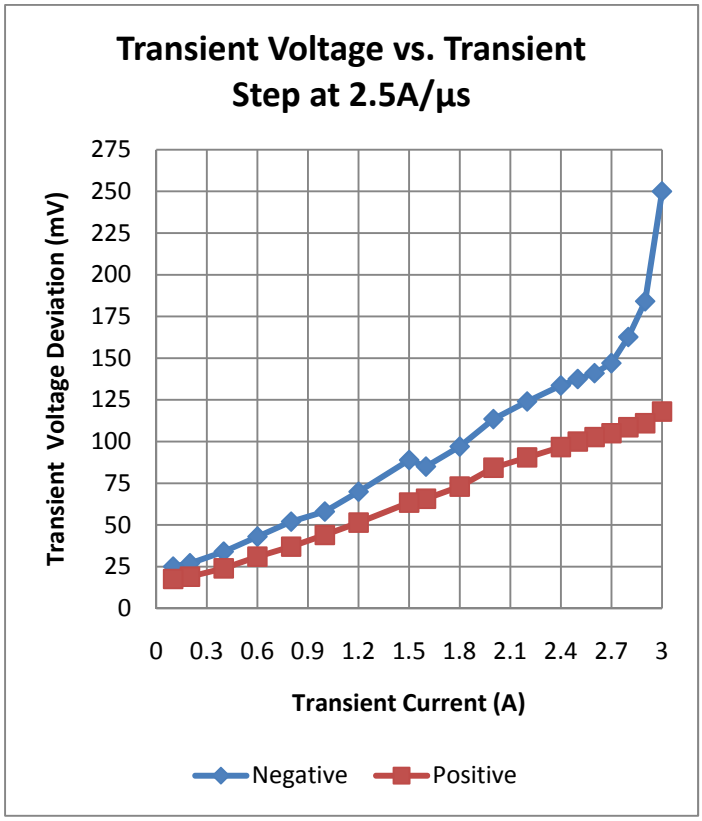

Figure 16: 5 V to 1.5 V Transient Voltage Graph

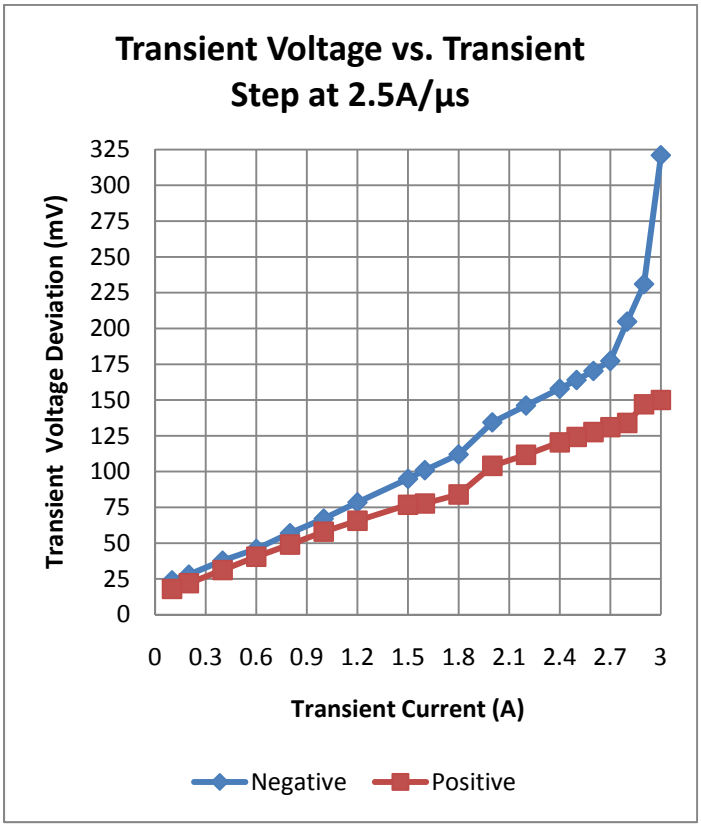

Figure 17: 5 V to 1.8 V Transient Voltage Graph

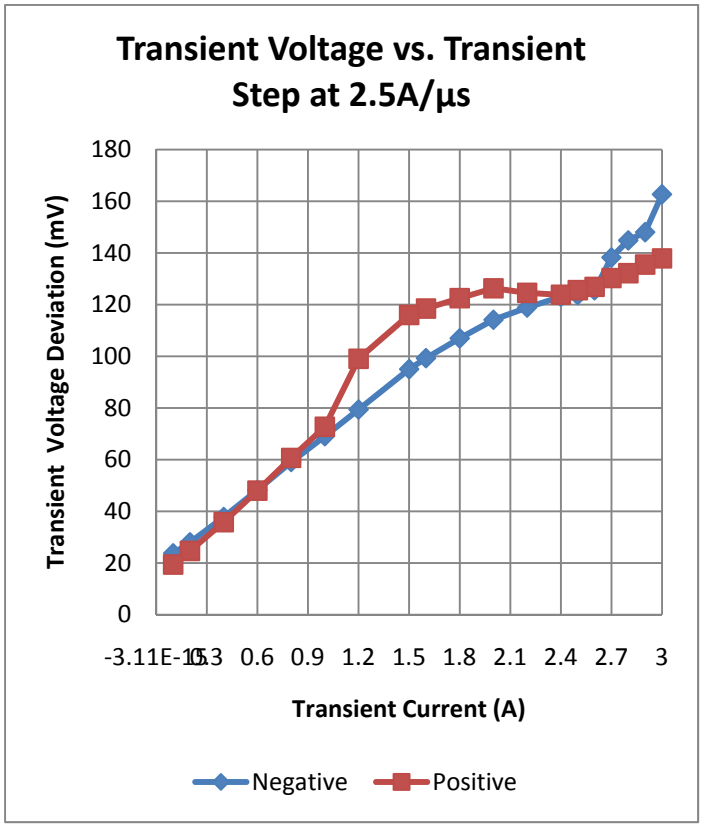

Figure 18: 12 V to 1.0 V Transient Voltage Graph

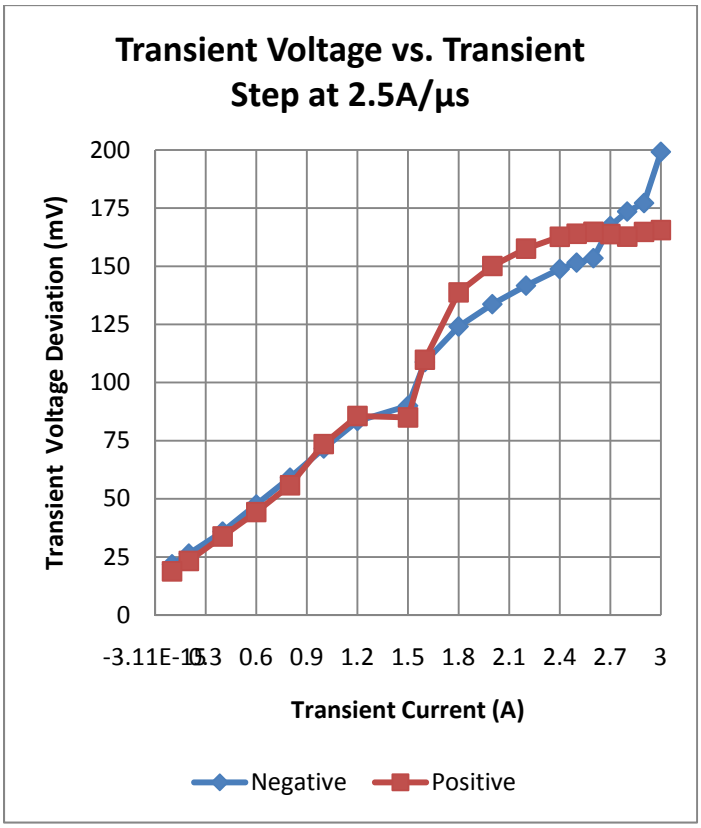

Figure 19: 12 V to 1.1 V Transient Voltage Graph

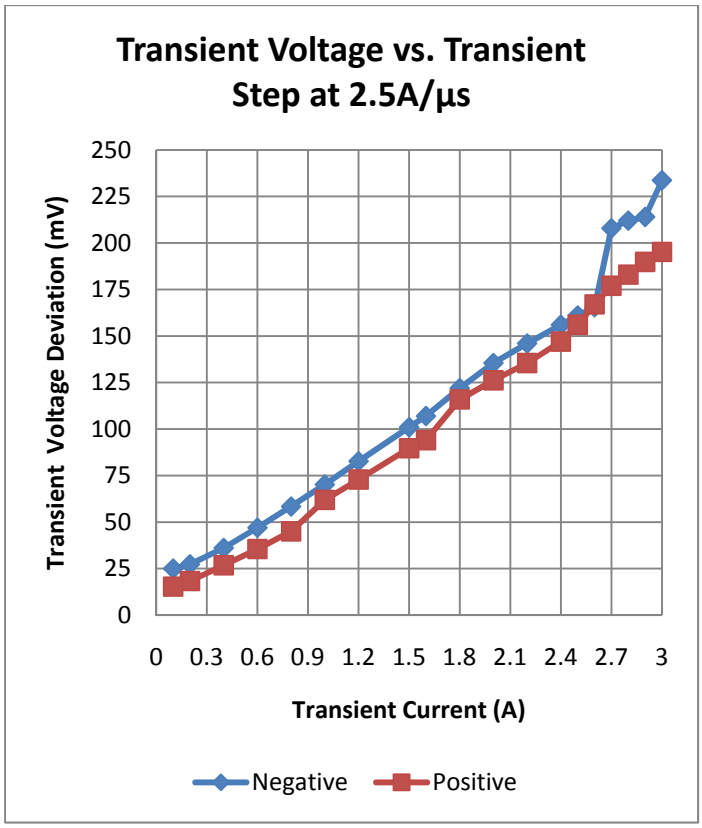

Figure 20: 12 V to 1.2 V Transient Voltage Graph

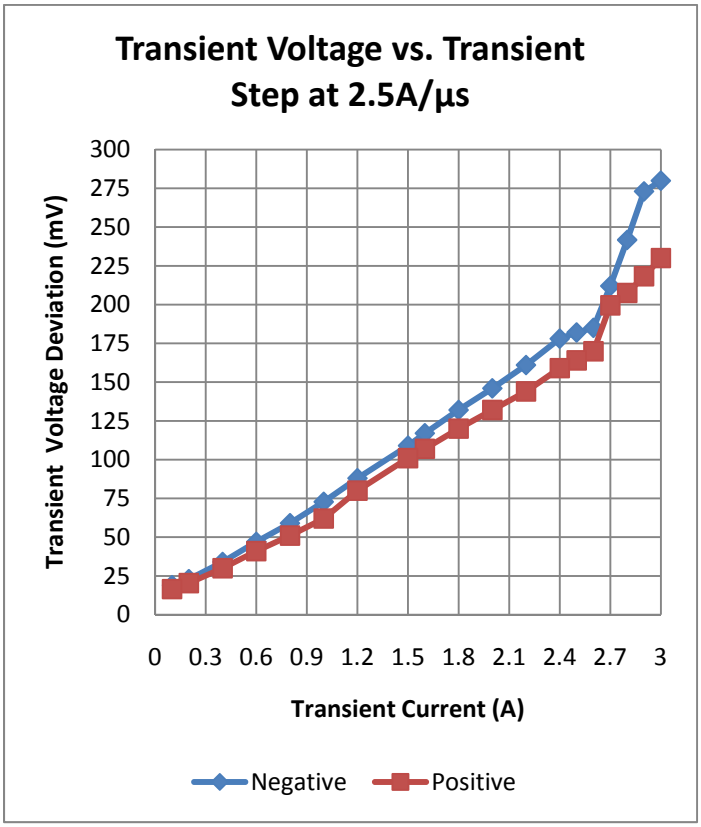

Figure 21: 12 V to 1.5 V Transient Voltage Graph

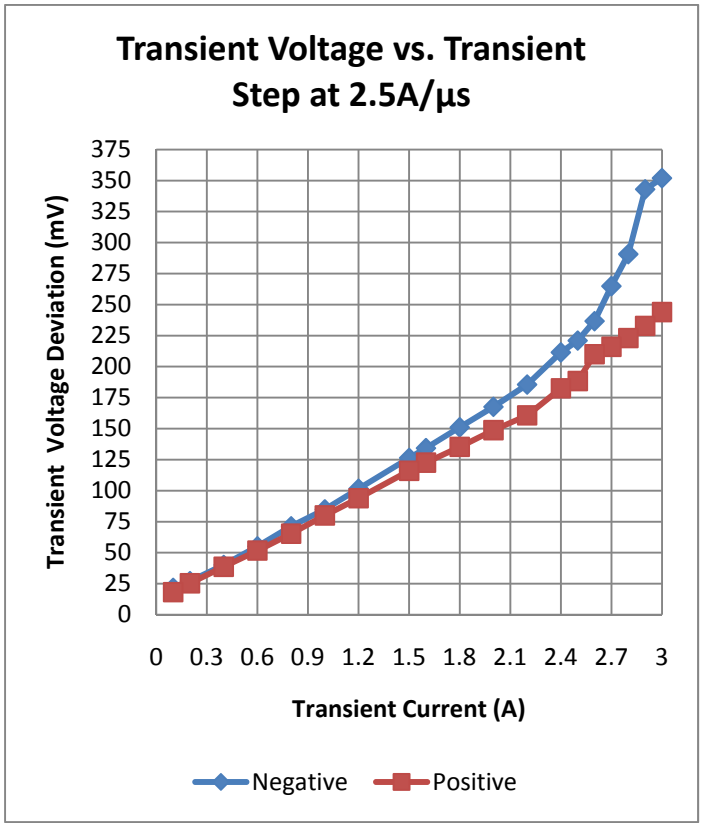

Figure 22: 12 V to 1.8 V Transient Voltage Graph

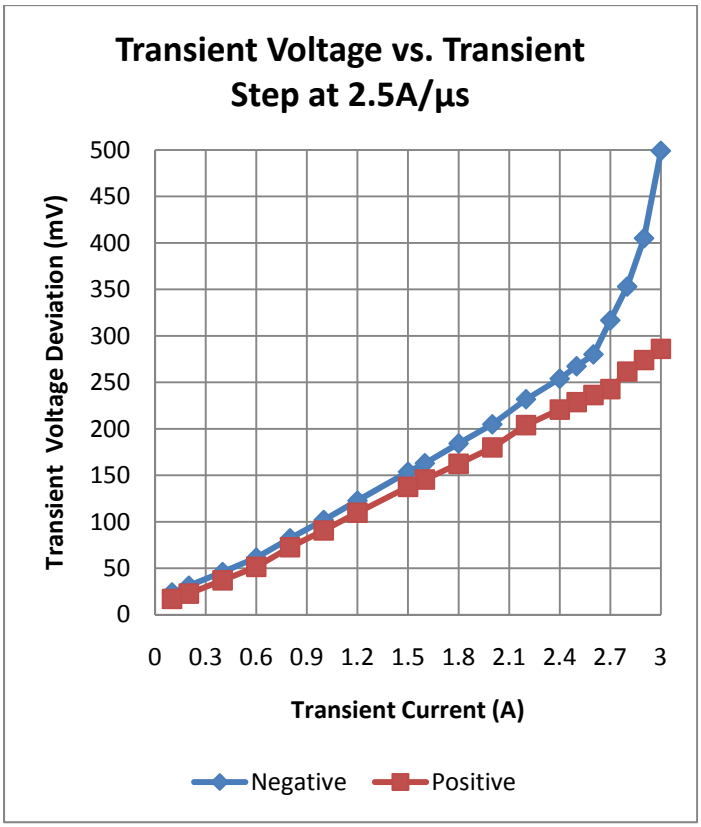

Figure 23: 12 V to 2.5 V Transient Voltage Graph

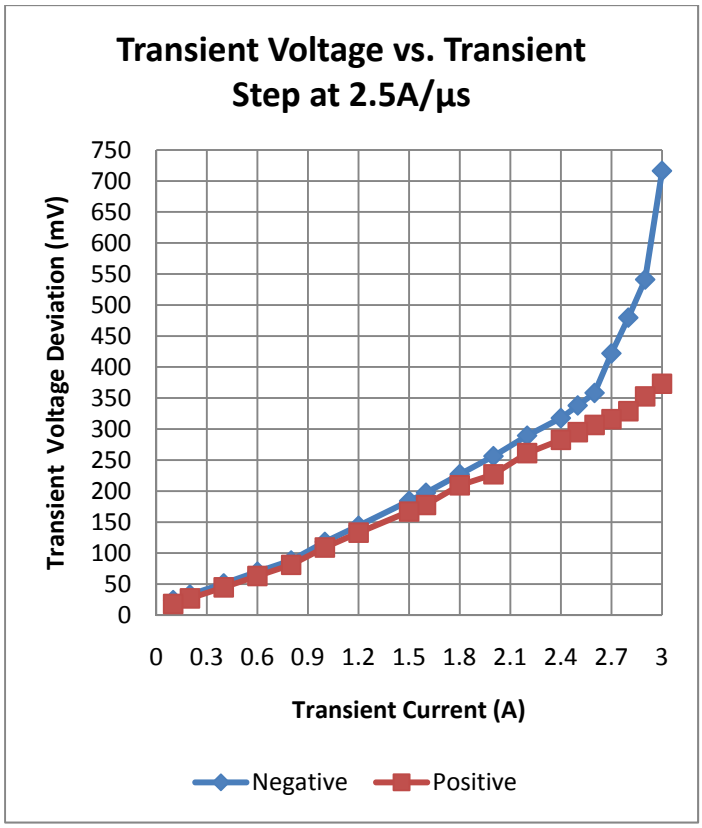

Figure 24: 12 V to 3.3 V Transient Voltage Graph

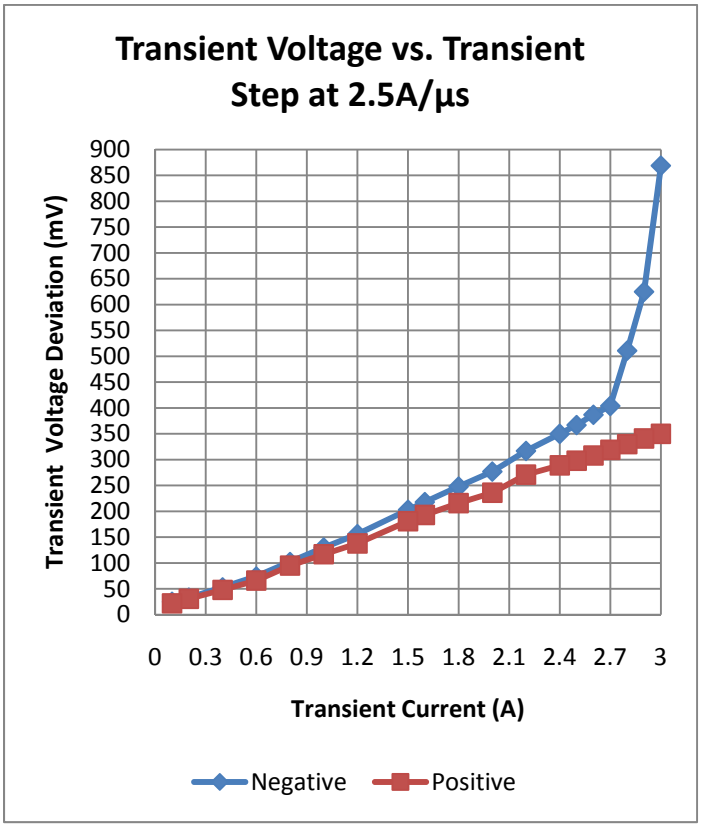

Figure 25: 12 V to 5.0 V Transient Voltage Graph

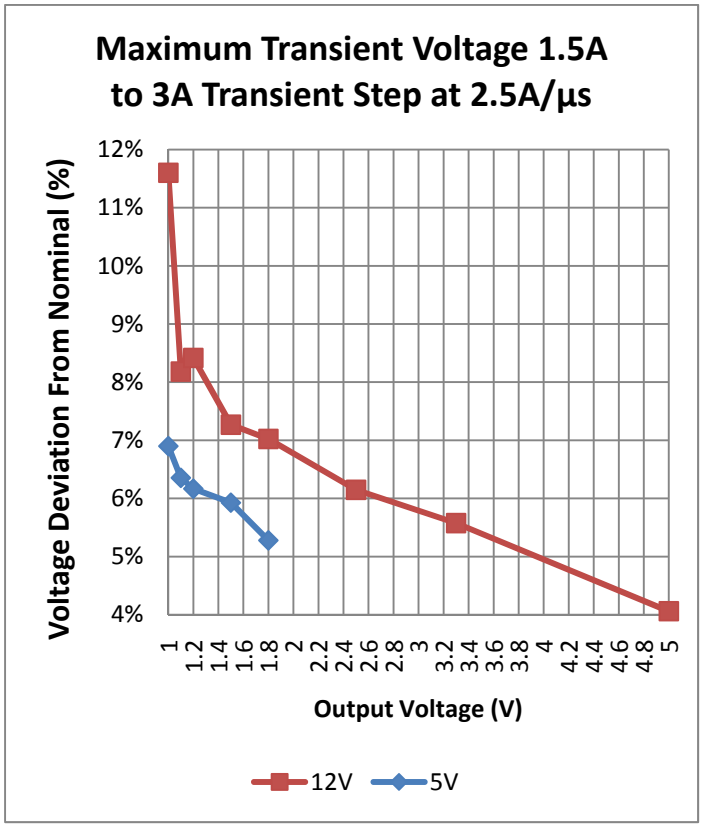

Figure 26: Transient Voltage for 1.5 A to 3 A

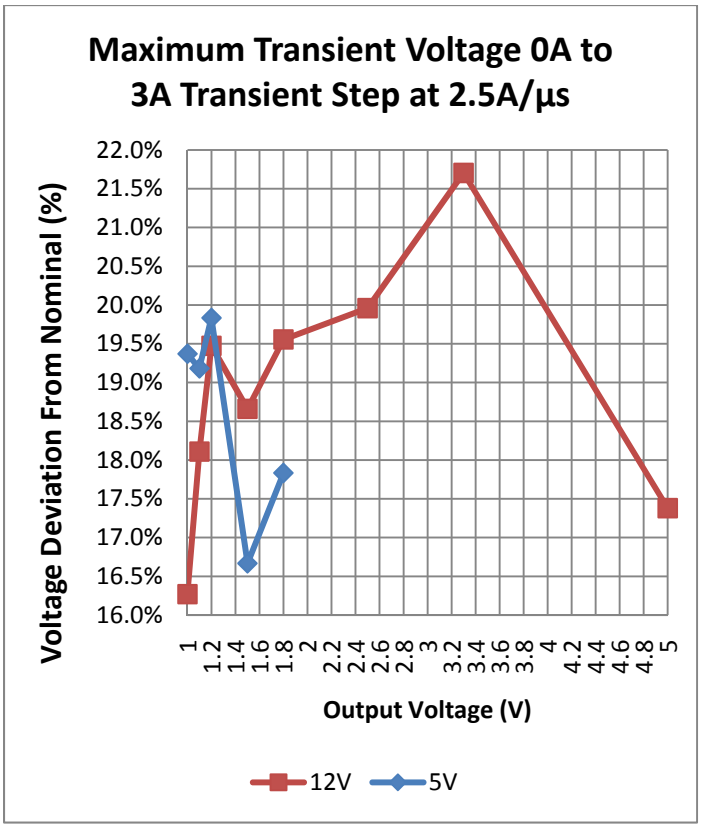

Figure 27: Maximum Transient Voltage for 0 A to 3A

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