CAT34C04

4-Kb Serial SPD EEPROM for DDR4 DIMM

Description

The CAT34C04 is a 4−Kb serial EEPROM, which implements the JEDEC JC42.4 (EE1004−v) Serial Presence Detect (SPD) specification for DDR4 DIMMs and supports the Standard (100 kHz), Fast (400 kHz) and Fast Plus (1 MHz) I^2C protocols.

One of the two available 2−Kb EEPROM banks (referred to as SPD pages in the EE1004−v specification) is activated for access at power−up. After power−up, banks can be switched via software command. Each of the four 1−Kb EEPROM blocks can be Write Protected by software command.

Features

- JEDEC JC42.4 (EE1004−v) Serial Presence Detect (SPD) Compliant
- Temperature Range: −40°C to +125°C
- Supply Range: 1.7 V − 3.6 V
- I^2C / SMBus Interface
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- 16−Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Low Power CMOS Technology
- 2 x 3 x 0.5 mm UDFN Package
- These Devices are Pb−Free and are RoHS Compliant

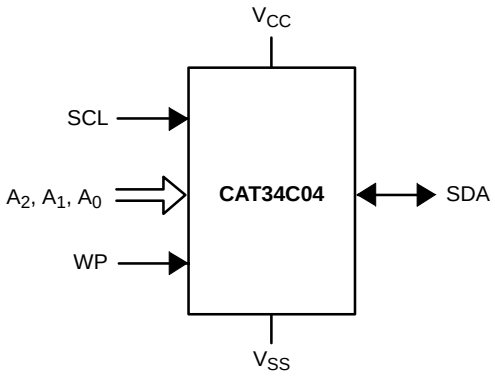

Figure 1. Functional Symbol

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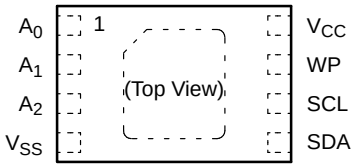
UDFN−8
HU4 SUFFIX
CASE 517AZ

PIN CONFIGURATION



UDFN (HU4)

For the location of Pin 1, please consult the corresponding package drawing.

MARKING DIAGRAM

UDFN−8

D2U	= Specific Device Code
A	= Assembly Location Code
LL	= Assembly Lot Number (Last Two Digits)
Y	= Production Year (Last Digit)
M	= Production Month (1 − 9, O, N, D)
▪	= Pb−Free Package

PIN FUNCTIONS

Pin Name	Function
A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect Input
V_{CC}	Power Supply
V_{SS}	Ground
DAP	Backside Exposed DAP at V_{SS}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any pin (except A_0) with respect to Ground (Note 1)	−0.5 to +6.5	V
Voltage on pin A_0 with respect to Ground	−0.5 to +10.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. The A_0 pin can be raised to a HV level for SWP command execution. SCL and SDA inputs can be raised to the maximum limit, irrespective of V_{CC}.

Table 2. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Units
N_{END} (Note 2)	Endurance	1,000,000	Write Cycles
T_{DR}	Data Retention	100	Years

2. Page Mode, V_{CC} = 2.5 V, 25°C

Table 3. THERMAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions/Comments	Max	Unit
Thermal Resistance θ_{JA}	Junction−to−Ambient (Still Air)	92	°C/W

3. Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature and T_A is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2−layer PCB.

Table 4. D.C. OPERATING CHARACTERISTICS (Vcc = 1.7 V to 3.6 V, TA = −40°C to +125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz or 1 MHz			1	mA
I_{CCW}	Write Current	Write, during t_{WR} (Note 4)			1	mA
I_{SB}	Standby Current	All I/O Pins at GND or Vcc	Vcc < 2.2 V		1	μA
			Vcc ≥ 2.2 V		2	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}			2	μA
V_{IL}	Input Low Voltage			−0.5	0.3*Vcc	V
V_{IH}	Input High Voltage			0.7*Vcc	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	$V_{CC} \geq$ 2.2 V, I_{OL} = 20 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.2 V, I_{OL} = 6.0 mA			0.2	V
V_{POR+}	Power On Reset Threshold	(Note 4)			1.3	V
V_{POR-}	Power Off Reset Threshold	(Note 4)		0.8		V

4. Tested initially and after a design or process change that affects this parameter

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. A.C. CHARACTERISTICS (Note 6) V_{CC} = 1.7 V to 3.6 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Standard V_{CC} = 1.7 V − 3.6 V		Fast V_{CC} = 1.7 V − 3.6 V		Fast−Plus V_{CC} = 2.2 V − 3.6 V		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL} (Note 5)	Clock Frequency	10	100	10	400	10	1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.26		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.50		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.26		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.26		µs
$t_{HD:DI}$	Data In Hold Time	0		0		0		µs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 7)	SDA and SCL Rise Time		1,000		300		120	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300		120	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.26		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		µs
$t_{HD:DAT}$	Data Out Hold Time	200	3450	200	900	0	350	ns
T_i (Note 7)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		µs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		µs
t_{WR}	Write Cycle Time		4		4		4	ms
t_{INIT} (Notes 7, 8)	Power-up to Ready Mode		0.5		0.5		0.5	ms
t_{POFF} (Note 9)	Warm power cycle off time	0.2		0.2		0.2		ms
$t_{TIMEOUT}$ (Note 10)	Detect clock low timeout	25	35	25	35	25	35	ms

5. The minimum clock frequency of 10 kHz is an SMBus recommendation; the minimum operating clock frequency is limited only by the SMBus time−out. The device also meets the Fast and Standard I^2C specifications, except that T_i and t_{DH} are shorter, as required by the 1 MHz Fast Plus protocol.
6. Test conditions according to “A.C. Test Conditions” table.
7. Tested initially and after a design or process change that affects this parameter.
8. t_{INIT} is the delay between the Power−On Reset threshold (V_{POR+}) and the device is ready to accept commands.
9. Power−Off delay to ensure a proper Reset when the V_{CC} drops below V_{POR-}
10. A timeout condition can only be ensured if SCL is driven low for $t_{TIMEOUT(Max)}$ or longer; then, CAT34C04 is reset and ready to receive a new START condition. CAT34C04 does not reset if SCL is driven low for less than $t_{TIMEOUT(Min)}$. The interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time−out count takes place when SCL is low in the time interval between START and STOP.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Load	Current Source: I_{OL} = 6 mA; C_L = 100 pF

Table 7. PIN CAPACITANCE (T_A = 25°C, V_{CC} = 3.6 V, f = 1 MHz)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}	SDA, Pin Capacitance	V_{IN} = 0		8	pF
	Input Capacitance (other pins)	V_{IN} = 0		6	pF

Table 8. INPUT IMPEDANCE

Symbol	Parameter	Test Conditions	Min	Max	Unit
Z_{IL}	Input Impedance for A0, A1, A2, WP Pins	V_{IN} < 0.3 * Vcc	30		kΩ
Z_{IH}	Input Impedance for A0, A1, A2, WP Pins	V_{IN} > 0.7 * Vcc	800		kΩ

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the memory. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on−chip pull−down resistor. The Write Protect pin should be tied directly either to Vcc or GND.

Power−On Reset (POR)

The CAT34C04 incorporates Power−On Reset (POR) circuitry which protects the device against powering up to an undetermined logic state. As V_{CC} exceeds the POR trigger level, the device will power up into standby mode. The device will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi−directional POR behavior protects the CAT34C04 against brown−out failure following a temporary loss of power. The POR trigger level is set below the minimum operating V_{CC} level.

Device Interface

The CAT34C04 supports the Inter−Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2−wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT34C04 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT34C04 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2.

I^2C/SMBus Protocol

The I^2C/SMBus uses two ‘wires’, one for clock (SCL) and one for data (SDA). The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all Slaves. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address (the preamble) determine whether the command is a read/write command (1010b) or a utility command (0110b), as described in Table 9. The next 3 bits, A2, A1 and A0, select one of 8 possible Slave devices. The last bit, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is being performed.

Acknowledge

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9th clock cycle (Figure 3). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9th clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 4.

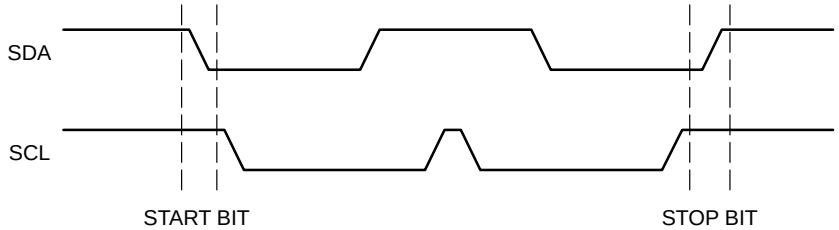


Figure 2. Start/Stop Timing

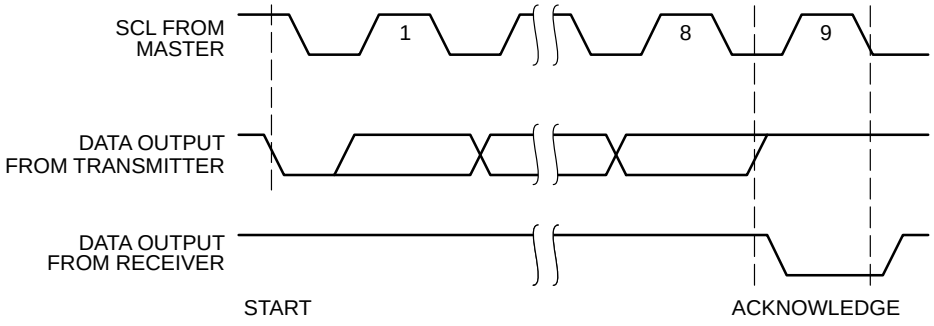


Figure 3. Acknowledge Timing

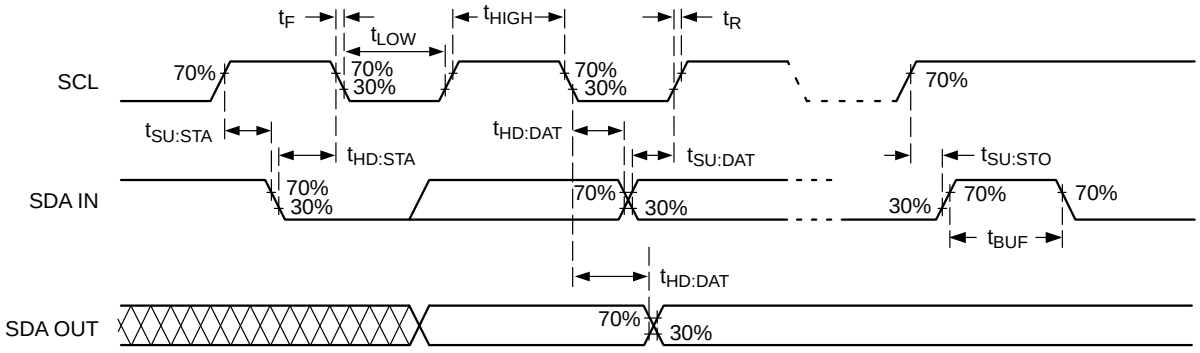


Figure 4. Bus Timing

Table 9. COMMAND SET (Notes 11, 12)

Function	Abbr	Function Specific Preamble				Select Address			R/W_n	A0 Pin
		b7	b6	b5	b4	b3	b2	b1	b0	
Read EE Memory	RSPD	1	0	1	0	LSA2	LSA1	LSA0	1	0 or 1
Write EE Memory	WSPD								0	
Set Write Protection, block 0	SWP0	0	1	1	0	0	0	1	0	V_{HV}
Set Write Protection, block 1	SWP1					1	0	0	0	V_{HV}
Set Write Protection, block 2	SWP2					1	0	1	0	V_{HV}
Set Write Protection, block 3	SWP3					0	0	0	0	V_{HV}
Clear All Write Protection	CWP					0	1	1	0	V_{HV}
Read Protection Status, block 0	RPS0					0	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 1	RPS1					1	0	0	1	0, 1 or V_{HV}
Read Protection Status, block 2	RPS2					1	0	1	1	0, 1 or V_{HV}
Read Protection Status, block 3	RPS3					0	0	0	1	0, 1 or V_{HV}
Set SPD Page Address to 0 (Select Lower Bank)	SPA0					1	1	0	0	0, 1 or V_{HV}
Set SPD Page Address to 1 (Select Upper Bank)	SPA1					1	1	1	0	0, 1 or V_{HV}
Read SPD Page Address	RPA					1	1	0	1	0, 1 or V_{HV}
Reserved	–					All Other Encodings				

11. LSAx stands for Logic State of Address pin x.
12. If V_{HV} is not applied on the A0 pin during SWP/CWP commands, the CAT34C04 will respond with NoACK after the 3rd byte and will not execute the SWP/CWP instruction. During RPS/SPA/RPA commands the state of pin A0 must be stable for the duration of the sequence.

EEPROM Bank Selection

Upon power−up, the address pointer is initialized to 00h pointing to the first location in the lower 2−Kb bank (SPD page 0).

Only one SPD page is visible (active) at any given time. The lower SPD page is automatically selected at power−up. The upper SPD page can be activated (and the lower one implicitly de−activated) by executing the SPA1 utility command. The SPA0 utility command can then be used to re−activate the lower SPD page without powering down. The identity of the active SPD page can be retrieved with the RPA command.

SPD page selection related command details are presented in Table 11c, Table 11d, Figure 12 and Figure 13.

Write Operations

EEPROM Byte Write

To write data to the EEPROM, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to ‘0’), followed by a starting data byte address, followed by data. The matching Slave will acknowledge the Slave address, EEPROM byte address and the data byte (Figure 5). The Master then ends the session by creating a STOP condition on the bus. The STOP starts the internal Write cycle for the (non−volatile) EEPROM data (Figure 6).

EEPROM Page Write

Each of the two 2−Kb banks is organized as 16 pages of 16 bytes each (not to be confused with the SPD page, which refers to the entire 2−Kb bank). One of the 16 memory pages is selected by the 4 most significant bits of the byte address, while the 4 least significant bits point to the byte position within the page. Up to 16 bytes can be written in one Write cycle (Figure 7).

During data load, the internal byte position pointer is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier data will be replaced by later data in a ‘wrap−around’ fashion within the 16−byte wide data buffer. The internal Write cycle then starts following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34C04 is busy writing to EEPROM, or is ready to accept commands. Polling is executed by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS). The CAT34C04 will not acknowledge the Slave address as long as internal EEPROM Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT34C04. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 8). If the WP pin is HIGH during the strobe interval, the CAT34C04 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT34C04 is shipped ‘unprotected’, i.e. none of the Software Write Protection (SWP) flags is set. The entire memory is erased, i.e. all bytes are 0xFF.

Read Operations

Immediate Read

A CAT34C04 presented with a Slave address containing a ‘1’ in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting EEPROM data from the current address pointer location. The Master stops this transmission by responding with NoACK, followed by a STOP (Figure 9).

Selective Read

The Read operation can be started from a specific address, by preceding the Immediate Read sequence with a ‘data less’ Write sequence. The Master sends out a START, Slave address and byte address, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figure 10).

Sequential EEPROM Read

EEPROM data can be read out indefinitely, as long as the Master responds with ACK (Figure 11). The internal address pointer is automatically incremented after every data byte sent to the bus. If the end of the active 2−Kb bank is reached during continuous Read, then the address count ‘wraps−around’ to the beginning of the active 2−Kb bank, etc. Sequential Read works with either Immediate Read or Selective Read, the only difference being that in the latter case the starting address is intentionally updated.

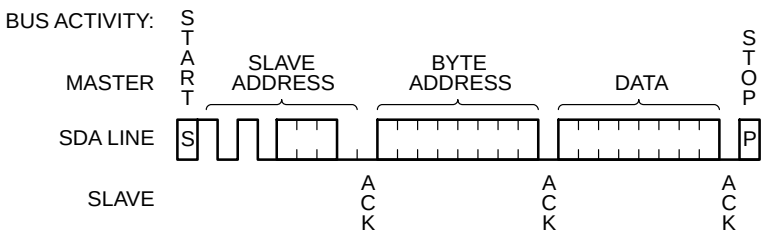


Figure 5. EEPROM Byte Write

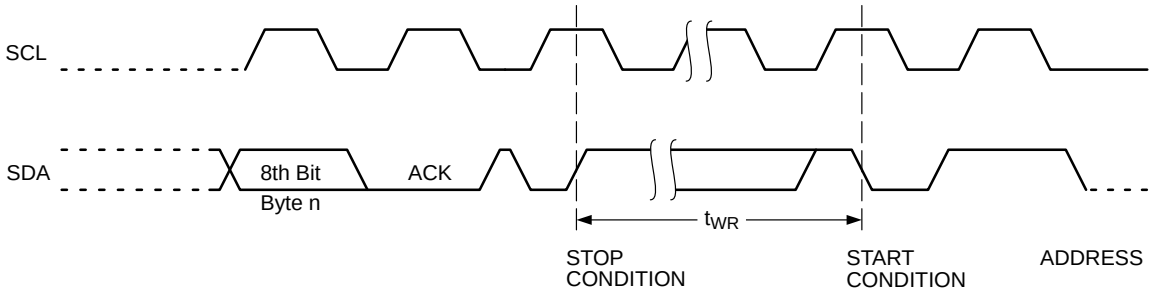
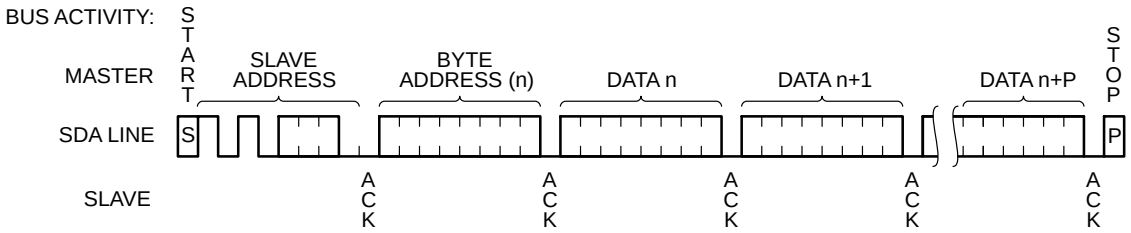


Figure 6. EEPROM Write Cycle Timing



NOTE: In this example n = XXXX 0000(B); X = 1 or 0

Figure 7. EEPROM Page Write

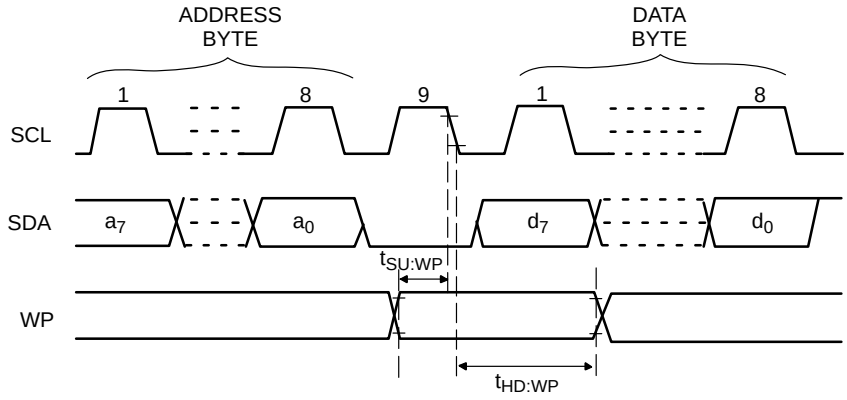


Figure 8. WP Timing

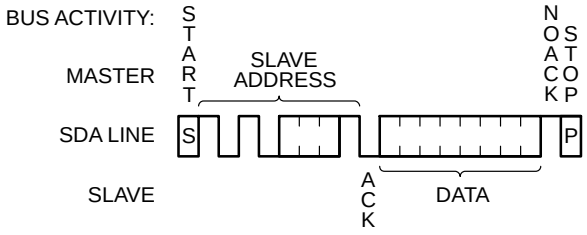


Figure 9. EEPROM Immediate Read

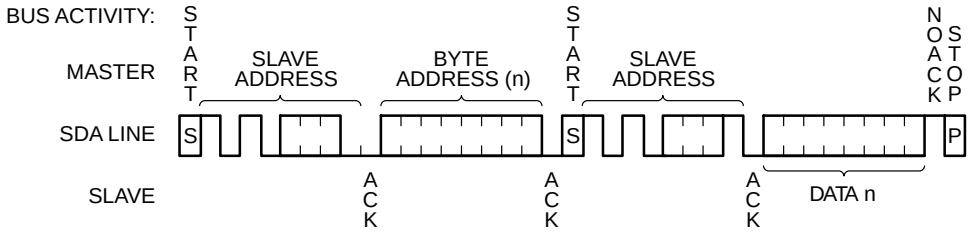


Figure 10. EEPROM Selective Read

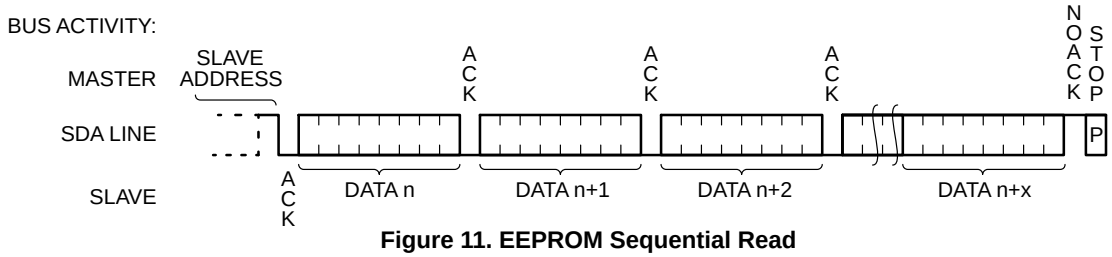


Figure 11. EEPROM Sequential Read

Software Write Protection

Each 1−Kb memory block can be individually protected against Write requests. Block identities are:

Block 0: byte address 0x00...0x7F (SPD page address = 0)
Block 1: byte address 0x80...0xFF (SPD page address = 0)
Block 2: byte address 0x00...0x7F (SPD page address = 1)
Block 3: byte address 0x80...0xFF (SPD page address = 1)

Block Software Write Protection (SWP) flags can be set or cleared in the presence of a very high voltage V_{HV} on address pin A0. The V_{HV} condition must be established on pin A0 before the START and maintained just beyond the STOP. The D.C. OPERATING CONDITIONS for SWP operations are shown in Table 10.

SWP command details are listed in Tables 11a and 11b.

SWP Slave addresses follow the standard I^2C convention, i.e. to read the state of a SWP flag, the LSB of the Slave address must be ‘1’, and to set or clear a flag, it must be ‘0’. For Set/Clear commands a dummy byte address and dummy data byte must be provided (Figure 12). In contrast to a regular memory Read, a SWP Read does not return data. Instead the CAT34C04 will respond with NoACK if the flag is set and with ACK if the flag is not set (Figure 13).

Table 10. SWPn AND CWP D.C. OPERATION CONDITION

Symbol	Parameter	Test Conditions	Min	Max	Units
ΔV_{HV}	A_0 Overdrive (V_{HV} − V_{CC})	1.7 V < V_{CC} < 3.6 V	4.8		V
I_{HVD}	A_0 High Voltage Detector Current			0.1	mA
V_{HV}	A_0 Very High Voltage		7	10	V

Table 11a. SWP SET COMMAND DETAIL (following Slave Address)

Command	Block(x) Protection	Slave Response	Address Byte	Slave Response	Data Byte	Slave Response	Write Cycle
SWPx(Note 13)	Not Set	ACK	(Dummy)	ACK	(Dummy)	ACK	Yes
	Set	NoACK	(Dummy)	NoACK	(Dummy)	NoACK	No
CWP	X	ACK	(Dummy)	ACK	(Dummy)	ACK	Yes

Table 11b. SWP QUERRY COMMAND DETAIL (following Slave Address)

Command	Block(x) Protection	Slave Response	Data Byte	Master (Response)	Data Byte	Master (Response)	
RPSx (Nots 13, 14)	Not Set	ACK	Dummy	(NoACK)	Dummy	(NoACK)	
	Set	NoACK	Dummy	(NoACK)	Dummy	(NoACK)	

Table 11c. SPD PAGE SELECT COMMAND DETAIL (following Slave Address)

Command	SPD Active Page	Slave Response	Address Byte	Slave Response	Data Byte	Slave Response	Write Cycle
SPAx (Notes 15, 16)	X	ACK	(Dummy)	ACK	(Dummy)	NoACK	No

Table 11d. SPD ACTIVE PAGE QUERRY COMMAND DETAIL (following Slave Address)

Command	SPD Active Page	Slave Response	Data Byte	Master (Response)	Data Byte	Master (Response)	
RPA (Notes 13, 14, 17)	0	ACK	Dummy	(NoACK)	Dummy	(NoACK)	
	1	NoACK	Dummy	(NoACK)	Dummy	(NoACK)	

13. The Master can terminate the sequence by issuing a STOP once the CAT34C04 responds with NoACK
14. The Master can terminate the sequence by responding with (NoACK) followed by STOP after any dummy data byte.
15. Setting the SPD Page Address to ‘0’ selects the lower 2−Kb EEPROM bank, setting it to ‘1’ selects the upper 2−Kb EEPROM bank.
16. The lower 2−Kb EEPROM bank (corresponding to SPD page address ‘0’) is active (visible) immediately following power−up.
17. The device will respond with ACK when the lower 2−Kb EEPROM bank is active and with NoACK when the upper 2−Kb EEPROM bank is active.

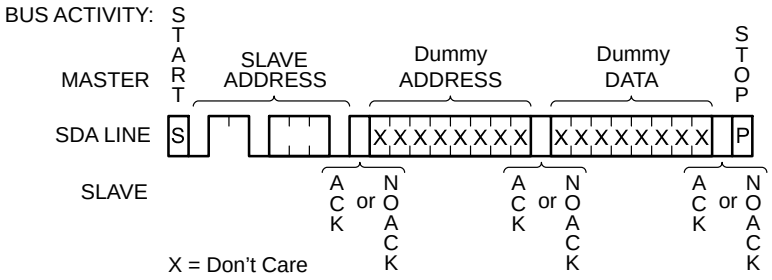


Figure 12. SWP & SPA Timing

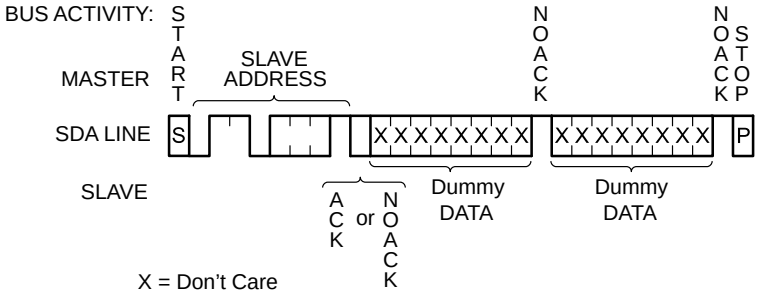


Figure 13. RPS & RPA Timing

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