AX8052 ERRATA

Errata
Silicon Errata for AX8052

ON Semiconductor®

www.onsemi.com

Introduction

This document lists silicon erratas, as well as features of the AX8052 that may be unexpected to the user. Note that this errata is applicable to all products containing the AX8052: AX8052F100, AX8052F143, AX8052F151 and AX8052F131.

This document refers to the silicon revisions listed in the table below.

Table 1.

Revision	SILICONREV Register
V1	0x8E
V1C	0x8F
V2	0x90

System Controller

Wakeup from Deep Sleep on Falling Edge of PB3

When in Deep Sleep mode, the Microcontroller is woken up from Deep Sleep by a falling edge on PB3. Care must be taken to avoid loosing wakeup events; that means hardware driving the PB3 pin must be designed to ensure generating a falling edge on PB3 while the microcontroller is in deep sleep.

Affected Revisions: V1
Fixed in Revision: V1C, V2

Setting RESET_N Low Does Not Wake Up the Chip from Deep Sleep

Workaround: For debugging, it is recommended to connect pin 7 of the Debug Adapter to PB3. The debug adapter will generate a falling edge when resetting the chip.

Chip−internal Power On Reset is not affected. Most applications therefore do not need to generate reset events on the RESET_N pin and can leave the pin open; they are unaffected by this issue. Applications needing to reset the chip using the RESET_N chip and requiring the use of the Deep Sleep mode are recommended to generate a falling edge on PB3 whenever RESET_N is pulled low.

Affected Revisions: V1
Fixed in Revision: V1C, V2

RESET_N Does Not Set GPIOENABLE to 1 after the Chip Once Entered Deep Sleep

Once the chip entered (and exited) Deep Sleep, subsequent low pulses on RESET_N will not set GPIOENABLE to 1. Therefore, GPIO Pins will not be enabled and continue to drive the value before reset.

Workaround: Set GPIOENABLE in software.

Affected Revisions: V1
Fixed in Revision: V1C, V2

Wakeup from Sleep Mode Resets System Controller Registers

System Controller and GPIO register values correctly retained during sleep mode. When waking up from sleep mode, these registers are accidentally reset to their power−up default values, just before the CPU starts executing code from the reset vector address.

I/O pin signal levels are retained however, until the CPU writes one to GPIOENABLE after wakeup.

The main implications are that after Wakeup:

1. Wakeup timer is reset
2. PINCHGA, PINCHGB, PINCHGC may not be used to determine the wakeup cause
3. External crystal oscillators are stopped

Workaround:

1. Wakeup timer needs to be restarted after wakeup from sleep mode
2. External means must be used if it is desired to know which GPIO pin caused the wakeup
3. External crystal oscillators must be restarted after wakeup from sleep mode

Affected Revisions: V1
Fixed in Revision: V1C, V2

Clock Monitor Incorrectly Triggers Switch Back to FRCOSC

The clock monitor incorrectly triggers switching back to FRCOSC. The clock monitor can therefore not be used reliably.

Workaround: Do not switch to a non−working clock. If there is any doubt a clock may be working before switching, software should check whether it works. This can be done using a general purpose timer. Two general purpose timers and an input capture unit may be used to easily measure the frequency ratio between any two clocks.

Affected Revisions: V1
Fixed in Revision: V1C, V2

LPOSC Calibration Should Not Be Used

The built−in automatic LPOSC calibration logic can cause LPOSC output glitches when enabled, and should therefore not be used.

Setting LPOSCKFILT to a value significantly lower than the maximum k_{FILT} value given in the programming manual (such as 100^{th} of the maximum k_{FILT} value) will limit the frequency and the effect on the tuning word of the glitches. However, occasional glitches will still occur and propagate to the LPOSC consumers. The application must be able to tolerate the occasional LPOSC glitch (eg. if a timer is driven by LPOSC, it may occasionally increment twice per LPOSC period).

Workaround: Enable LPOSC calibration, but set LPOSCKFILT to zero. When an LPOSC Calibration interrupt is signaled (see register OSCCALIB), read the period register (LPOSCPER) and manually compute the new LPOSC tuning word. Delay writing the computed tuning word to LPOSCFREQ until approximately $1/4^{th}$ of the LPOSC period after the LPOSC Calibration interrupt was signaled.

Affected Revisions: V1
Fixed in Revision: V1C and V2

FRCOSC Calibration from Radio Clock

If the Radio Clock is selected as calibration source for automatic FRCOSC calibration, calibration is only performed if the Radio Clock is also selected as system clock source (Register CLKCON), or the Radio Clock is selected as the source clock for one (or both) of the wake−up timer counters.

Affected Revisions: V1
Fixed in Revision: V1C, V2

Changing Clock Sources May Accidentally Enable XOSC or LPXOSC

Changing the clock source of any peripheral may accidentally enable the Crystal Oscillator or the Low Power Crystal Oscillator.

If crystals are connected to PA0/PA1 and PA3/PA4 and these pins are configured as analog inputs, the oscillators will switch off again after two falling clock cycles, and therefore this is not a problem.

Otherwise, these oscillators may be switched off again manually by calling libmf routines turn_off_xosc() and turn_off_lpxosc(). These routines require to toggle PA0/PA1 and PA3/PA4, respectively.

The accidental enabling of the Crystal Oscillators may be avoided by carefully switching clock sources as follows:

- System Clock (CLKCON)
  - Only switch to and from any clock source via FRCOSC
  - When switching from FRCOSC to LPXOSC, first switch to LPOSC, then to LPXOSC.
    When switching from LPXOSC to FRCOSC, first switch to LPOSC, then FRCOSC.
- Wakeup Timer (WTCFGA, WTCFGB)
  For setting WTCFGx to value y, use the following code sequence:
  1. WTCFGx |= 0x04;
  2. WTCFGx = 0x0F;
  3. WTCFGx &= y | 0xFC;
  4. WTCFGx = y;
- ADC (ADCCLKSRC)
  Only switch ADC clock sources while all ADCCHxCONFIG registers are set to 0xFF
- SPI Master (SPSCKSRC)
  Only switch SPI Master clock sources while SPMODE is *not* set to SPI Master, i.e. SPMODE ≠ 01
- Timer (TxCLKSRC)
  Only switch Timer clock sources while TxMODE is set to Off, i.e. TxMODE = 000

Starting with revision V1C, the microcontroller features the MISCCTRL register, where both the Crystal Oscillator and the Low Power Crystal Oscillator may be disabled permanently.

Affected Revisions: V1
Fixed in Revision: V1C, V2

Current Consumption after Entering Standby Mode

Several Milliseconds to several hundred Milliseconds after entering sleep mode, device current consumption may briefly rise to approximately 2 mA and fall to normal levels again.

It is recommended to add seven NOP instructions immediately after the write instruction that sets PCON bits 1:0 to 01, or alternatively to use the libmf function enter_sleep() to prevent this current spike.

Affected Revisions: V1
Fixed in Revision: V1C, V2

CPU Clock Rates Less than 10 kHz Not Recommended

ON Semiconductor does not recommend to run the Microcontroller Core at less than 10 kHz (less than 10000 Instructions/s). Instead, the Microcontroller should be run from a faster clock source, and be put in standby or sleep mode when the system is idle.

Affected Revisions: V1
Fixed in Revision: V1C, V2

Temperature Sensor Should Be Converted with the CPU in Standby Mode

When converting the temperature sensor value, the CPU should be set to Standby mode. Otherwise, the converted temperature values will be noisier and the average will be affected as well. Wake−up from Standby mode can be effected either by an ADC interrupt handler, or using the code sequence below:

```
start conversion (see ADCCONV register)
  for (;;) {
        EA = 0;
        if (ADCCONV & 0x80)
                        break;
        EIE_6 = 1;
        enter_standby();
        EIE_6 = 0;
        EA = 1;
  }
  EA = 1;
  read ADCCH0VAL0
  read ADCCH0VAL1
```

The ADC clock source (register ADCCLKSRC) should be set to the same clock as the system clock (register CLKCON). The divider should be set so that the conversion rate falls into the range given by the datasheet. The ADC clock source should not be set to system clock (register ADCCLKSRC(2:0) should not be set to 110), because the system clock is turned off during standby. Most commonly, the microcontroller runs from the internal fast RC oscillator (CLKCON = 0x00), in this case the recommended ADC clock setting for temperature conversion is ADCCLKSRC = 0x30.

Affected Revisions: V1, V1C
Fixed in Revision: V2

Power−On Reset

A power−up voltage ramp start voltage of 0.3 V or less is required for V1 silicon to reliably signal power−on Reset. For V1C, a start voltage of 0.6 V or less is required.

Starting with revision V2 the POR generation circuitry is fully level sensitive, triggering POR at a VDD_IO level of typically 1 V and insensitive to the ramp start voltage or speed.

Affected Revisions: V1, V1C
Fixed in Revision: V2

RESET_N during VDDIO Ramp−Up

If the external RESET_N input is asserted (held low) during VDDIO Voltage Ramp−Up, an elevated current draw may be observed on VDDIO. As soon as RESET_N is deasserted, the current returns to normal levels. Subsequent assertions of RESET_N while VDDIO remains supplied will not cause any elevated current draw. This additional current will not damage the chip, it is however recommended to keep RESET_N pulses short.

Affected Revisions: V1, V1C
Fixed in Revision: V2

Timer TxIRQRO, TxIRQRU, TxIRQEO , TxIRQEU Clear on Read takes Precedence over Set

The timer status bits TxIRQRO , TxIRQRU, TxIRQEO , TxIRQEU are designed to clear on read. Clearing on read takes precedence in the affected chips. So software polling the status bits in a tight loop miss overflow or underflow events whenever the event coincides with reading the status register in the same clock cycle. It is recommended to use an interrupt handler on the affected chips to mitigate this issue.

Affected Revisions: V1, V1C
Fixed in Revision: V2

GPADC Missing Codes

The GPADC converter exhibits missing codes at mid−level (or zero in differential mode) input.

Affected Revisions: V1, V1C, V2

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5817−1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative