AS0142AT-ADD/D

Product Preview

AS0142AT Advance Data Sheet Addendum

1/4−Inch Color CMOS Image Sensor and Signal Processor Stack Chip

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ADDENDUM

Introduction

This document supplements ON Semiconductor's AS0142AT Advance Datasheet with reference information on:

- Ordering Information
- Package Pinout Overview
- Pinout Description
- AS0142AT Regulator Mode Connection

For further information on this 1/4−inch Color CMOS Image Sensor and Signal Processor Stack Chip housed within 143 balls iEBGA package, the Advance Datasheet should be referenced.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

REFERENCE INFORMATION

Table 1. ORDERING INFORMATION

Part Number	Product Description	Orderable Product Attribute Description
AS0142ATSC00XUSM0−DRBR−E	Rev1, Engineering Sample, iEBGA Package	Dry−pack without Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0−DPBR−E	Rev1, Engineering Sample, iEBGA Package	Dry−pack with Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0−TRBR−E	Rev1, Engineering Sample, iEBGA Package	Tape & Reel without Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0−TPBR−E	Rev1, Engineering Sample, iEBGA Package	Tape & Reel with Protective Film; Double Side ARC Glass
AS0142ATSC00XUSM0H3−GEVB	AS0142 Rev 1 iEBGA Sample housed in DEMO 3 Headboard	N/A

Table 2. PACKAGE PINOUT OVERVIEW

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VDD_1V8	VAA_2V8	VAA_2V8	VAA_2V8	LDO_1V2	LDO_1V2	DOUT1	EXT_REG	DOUT0	DOUT2	VDD_1V2	VDD_1V2	**A**
B	VDD_1V8	VDD_1V8	NC	REG_1V8	REG_1V8	LDO_1V2	XTAL	DOUT7	ENLDO	DOUT9	VDD_1V2	PD_1	**B**
C	1V8_PHY	NC	NO BALL	NC	REG_1V8	2V8_PHY	DOUT4	EXTCLK	DOUT5	DOUT10	DOUT3	DOUT6	**C**
D	NC	NC	1V8_IO	DGND	DGND	DGND	DGND	DGND	DGND	DOUT11	DOUT8	1V8/2V8/3V3_IO	**D**
E	PD_1	PD_1	1V8_IO	DGND	DGND	DGND	DGND	DGND	DGND	DOUT12	DOUT13	1V8/2V8/3V3_IO	**E**
F	PU_1	RESET_BAR	SPI_CS_BAR	DGND	DGND	DGND	DGND	DGND	DGND	DOUT14	DOUT15	1V8/2V8/3V3_IO	**F**
G	SCLK	PU_1	SPI_SCLK	DGND	DGND	DGND	DGND	DGND	DGND	DOUT16	DOUT17	RESERVED	**G**
H	FLASH	PD_2	STANDBY	DGND	DGND	DGND	DGND	DGND	DGND	DOUT20	AGND	AGND	**H**
J	PD_2	GPIO_5	PD_1	DGND	DGND	DGND	DGND	DGND	DGND	DOUT18	AGND	AGND	**J**
K	PD_2	SDATA	SADDR	GPIO_2	GPIO_1	GPIO_4	DOUT19	FRAME_SYNC	DOUT23	DOUT21	AGND	AGND	**K**
L	NC	GPIO_6	SPI_SDO	SPI_SDI	OTPM_2V8	PD_1	GPIO_3	FRAME_VALID	PD_1	META_LINE_VALID	TRIGGER_OUT	PD_1	**L**
M	NC	NC	NC	NC	NC	NC	NC	LINE_VALID	DOUT22	PIXCLK	NC	PD_2	**M**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	

Table 3. PINOUT DESCRIPTION

Pinout Category	Pinout Name(s)	Pinout Direction	Correspondent Ball(s)	Ball(s) Total	Note(s)
Power	1V8/2V8/3V3_IO	Supply	D12, E12, F12	3	·Host Interface Supply, 1.8V/ 2.8V/ 3.3V capable
	1V8_IO	Supply	D3, E3	2	·Sensor Interface Supply, 1.8V nominal
	2V8_PHY	Supply	C6	1	·Host HiSPi Supply, 2.8V nominal
	1V8_PHY	Supply	C1	1	·Sensor HiSPi Supply, 1.8V nominal
	OTPM_2V8	Supply	L5	1	·Host OTPM Supply, 2.8V nominal
	VAA_2V8	Supply	A2, A3, A4	3	·Sensor Array Supply, 2.8V nominal
	REG_1V8	Supply	B4, B5, C5	3	·Host Regulator Supply, 1.8V nominal
	VDD_1V8	Supply	A1, B1, B2	3	·Sensor Digital Core Supply, 1.8V nominal
	LDO_1V2	Supply	A5, A6, B6	3	·Host Regulator Output, 1.2V nominal ·Sense Line embedded
	VDD_1V2	Supply	A11, A12, B11	3	·Host Digital Core Supply, 1.2V nominal
	AGND	Supply − GND	H11, H12, J11, J12, K11, K12	6	·Analog related Stack Chip Ground
	DGND	Supply − GND	D4 to D9, E4 to E9, F4 to F9, G4 to G9, H4 to H9, J4 to J9	36	·Digital related Stack Chip Ground
Host Regulator Control	ENLDO	Input	B9	1	·Host Regulator enable (REG_1V8 domain)
	EXT_REG	Input	A8	1	·External Supply enable (VDD_1V2 domain)
Master Clock	EXTCLK	Input	C8	1	·This can either be a square−wave generated from an oscillator (in which case the XTAL input must be left unconnected), or direct connection to a crystal
	XTAL	Output	B7	1	·If EXTCLK is connected to one pin of a crystal, the other pin of the crystal is connected to XTAL pin; otherwise this signal must be left unconnected.
SPI Interface	SPI_CS_BAR	Output	F3	1	·Chip select out to SPI flash or EEPROM memory
	SPI_SCLK	Output	G3	1	·Clock output for interfacing to an external SPI flash or EEPROM memory
	SPI_SDI	Input	L4	1	·Data in from SPI flash or EEPROM memory ·Pin with Internal Pull Up Resistor ·When no SPI device detected, the logic state of this pin decides whether AS0142AT should perform Auto−Configure ·0: Do not Auto−Configure; Two−wire interface will be used to configure the device (i.e. Host−Configure mode) ·1: Auto−Configure
	SPI_SDO	Output	L3	1	·Data out to SPI flash or EEPROM memory

Table 3. PINOUT DESCRIPTION

Pinout Category	Pinout Name(s)	Pinout Direction	Correspondent Ball(s)	Ball(s) Total	Note(s)
Two Wired	SCLK	Input	G1	1	·Host two−wire serial clock ·Recommended 1.5 KOhm to 1V8/2V8/3V3_IO
	SDATA	I/O	K2	1	·Host two−wire serial data ·Recommended 1.5 KOhm to 1V8/2V8/3V3_IO
General Purpose I/O	GPIO[6:1]	I/O	L2, J2, K6, L7, K4, K5	6	·Configurable Host I/O interface
Inactive Control	RESET_BAR	Input	F2	1	·Hard Reset Control, Active Low ·No Hardware State Retention ·Pin with Internal Pull Up Resistor
	STANDBY	Input	H3	1	·Hard Standby Control, Active High ·Hardware State Retention possible
Two Wire Address Definition	SADDR	Input	K3	1	·Selects device address for the two−wire slave serial interface ·When connected to GND the device ID is 0x90 ·When wired to 1V8/2V8/3V3_IO, the device ID is 0xBA
Host Output	PIXCLK	Output	M10	1	·Host pixel clock output
	FRAME_VALID	Output	L8	1	·Host frame valid output (synchronous to PIXCLK)
	LINE_VALID	Output	M8	1	·Host line valid output (synchronous to PIXCLK)
	META_LINE_VALID	Output	L10	1	·Line valid signal to indicate when Meta-data is valid ·There is an option to allow META_LINE_VALID to be reflected in LINE_VALID
	DOUT[23:0]	Output	K9, M9, K10, H10, K7, J10, G11, G10, F11, F10, E11, E10, D10, C10, B10, D11, B8, C12, C9, C7, C11, A10, A7, A9	24	·Host pixel data output (synchronous to PIXCLK)
	FRAME_SYNC	Output	K8	1	·Pass through to TRIGGER_OUT ·This signal should be connected to GND if not used
	TRIGGER_OUT	Output	L11	1	·Host Trigger signal to embedded image sensor
	FLASH	Output	H1	1	·External Flash Light Control Output

Table 3. PINOUT DESCRIPTION

Pinout Category	Pinout Name(s)	Pinout Direction	Correspondent Ball(s)	Ball(s) Total	Note(s)
Special Pins	NC	DO NOT CONNECT	B3, C2, C4, D1, D2, L1, M1 to M7, M11	14	·ON Internal Monitor Function Only
	Reserved	DO NOT CONNECT	G12	1	·ON Internal Debug Only
	PU_1	I/O	F1, G2	2	·Embedded Image Sensor Two−Wires Pins (for Stack Chip internal communication) ·Recommended 1.5 KOhm to 1V8_IO
	PD_1	I/O	B12, E1, E2, J3, L6, L9, L12	7	·Must be at Logic Low for proper Stack Chip Operation ·Recommended 10 KOhm to GND
	PD_2	I/O	H2, J1, K1, M12	4	·Pull down to GND for proper Stack Chip Operation ·Recommended 1 KOhm to GND

Table 4. AS0142AT REGULATOR MODE CONNECTION

Pinout Name	Internal Regulator Connection	External Supply Connection
REG_1V8	1.8 V Nominal	Tied to 1V8/2V8/3V3_IO
ENLDO	Tied to REG_1V8	Tied to GND
EXT_REG	GND	Tied to 1V8/2V8/3V3_IO
LDO_1V2	1.2 V nominal (Output)	Floating (No Connection)
VDD_1V2	Tied with LDO_1V2	External 1.2 V Nominal Supply

PUBLICATION ORDERING INFORMATION

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