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STK531U3xx series



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Application Note

1. Product synopsis

This application handbook is intended to provide practical guidelines for the **STK531U3xx series** use.

The **STK531U3xx series** is Intelligent Power Module (IPM) based upon ON's Insulated Metal Substrate Technology (IMST) for 3-phase motor drives which contain the main power circuitry and the supporting control circuitry. The key functions are outlined below:

- Highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single small SIP module.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal Boost diodes are provided for high side gate boost drive.
- Externally accessible embedded thermistor for substrate temperature measurement.
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- Single control power supply due to Internal bootstrap circuit for high side pre-driver circuit.
- Mounting points are available on SIP package

A simplified block diagram of a motor control system is shown in Figure 1.

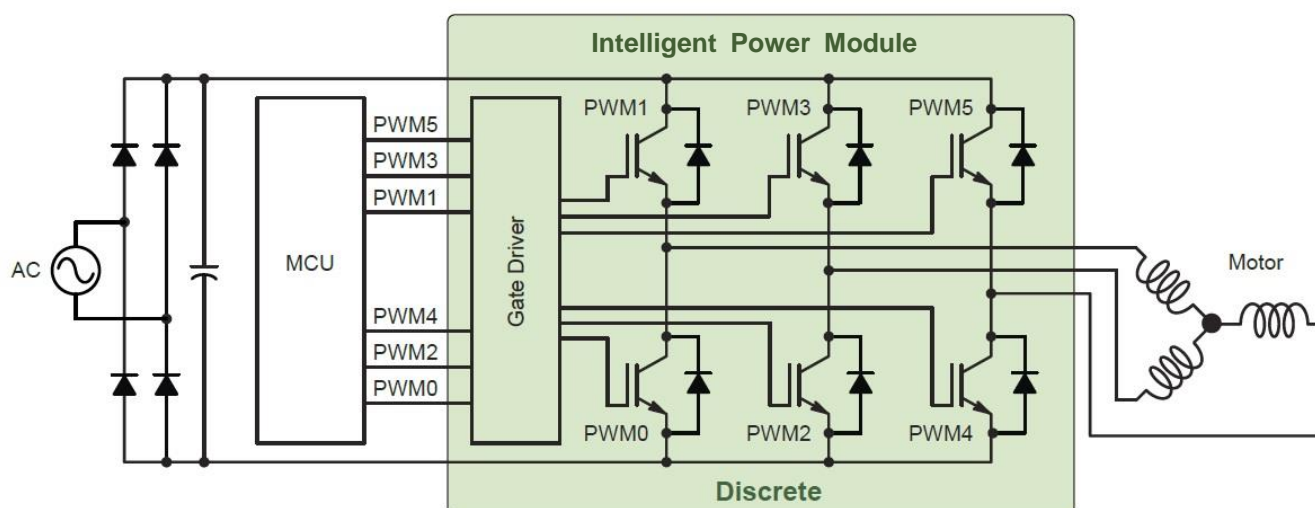


Figure 1. Motor Control System Block Diagram

2. Product description

Table1. gives an overview of the available devices, for a detailed description of the packages refer to Chapter 6.

Device	STK531U369A-E	STK531U394A-E
Feature	single shunt	
Package	SIP05 – horizontal pins	
Voltage (VCEmax.)	600V	
Current (Ic)	10A	15A
Peak current (Ic)	20A	30A
Isolation voltage	2000V	
Shunt resistance	33mΩ	25mΩ

Table 1. Device Overview

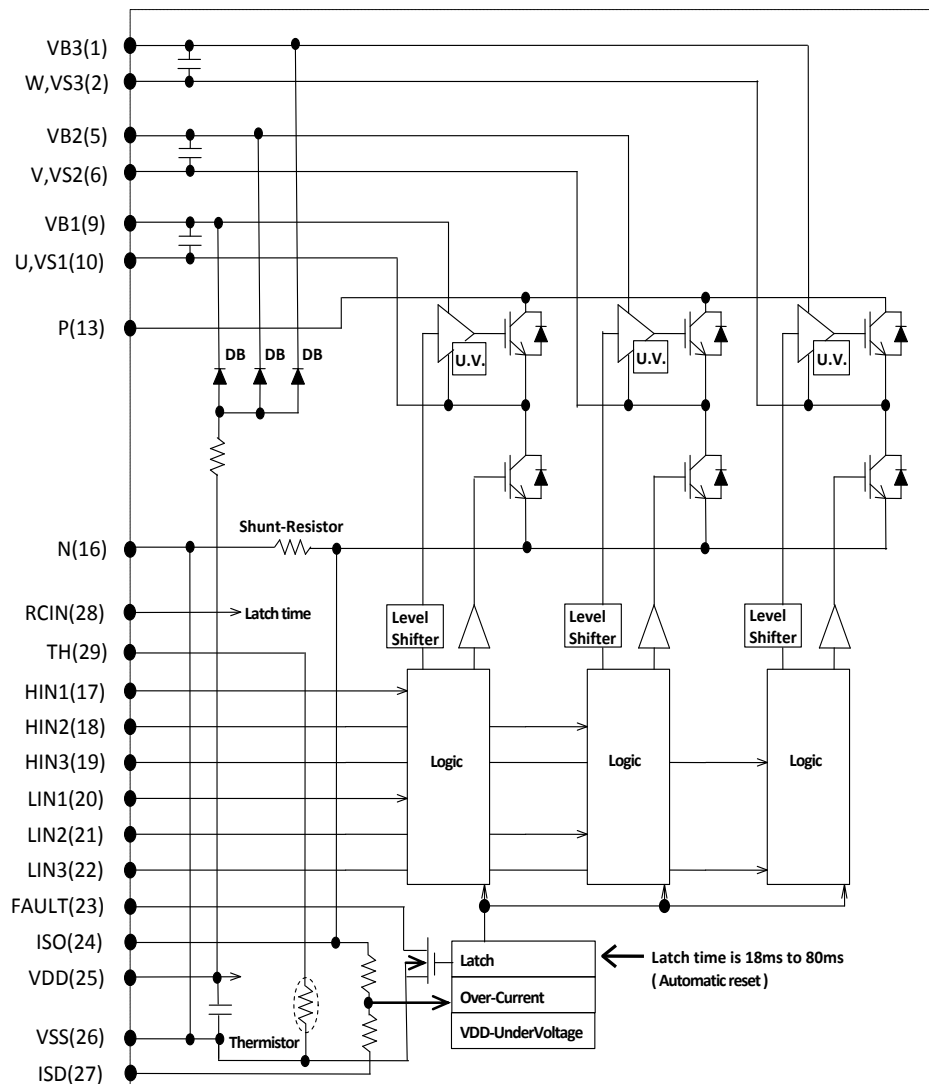


Figure 2. STK531U3xx series equivalent circuits

The high side drive is used with a bootstrap circuit to generate the higher voltage needed for gate drive. The Boost diodes are internal to the part and sourced from VDD (15V). There is an internal level shift circuit for the high side drive signals allowing all control signals to be driven directly from Vss levels common with the control circuit such as the microcontroller without requiring external level shift such as opto isolators.

3. Performance test guidelines

The following Chapter gives performance test method shown in Figures 3 to 7.

3.1. Switching time definition and performance test method

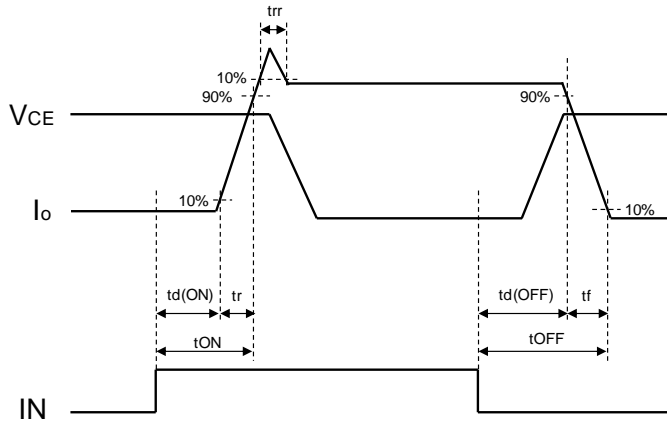


Figure 3. Switching time definition

Ex) Lower side U phase measurement

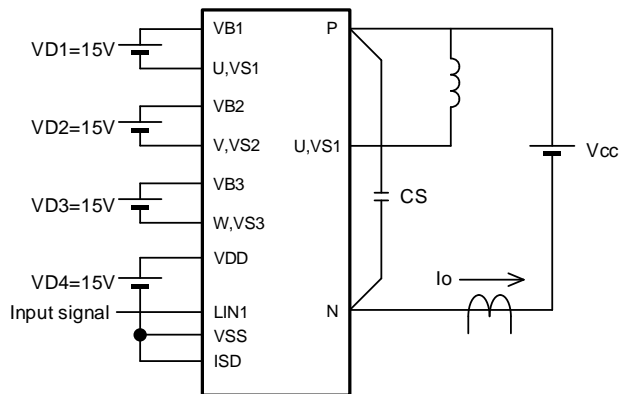


Figure 4. Evaluation circuit (Inductive load)

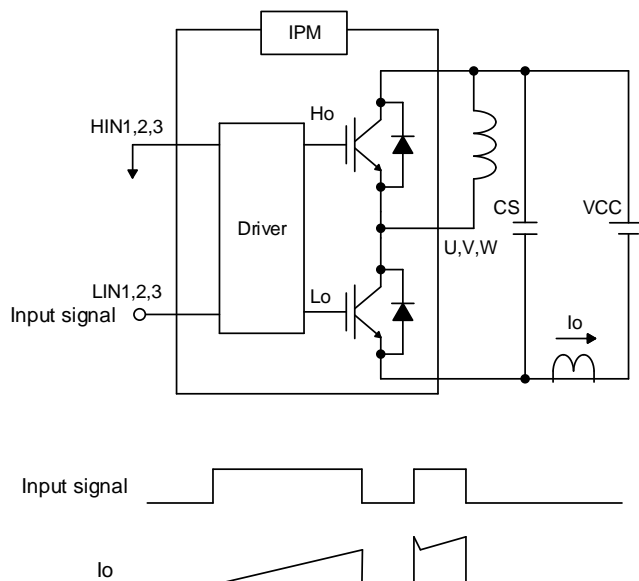


Figure 5. Switching loss circuit

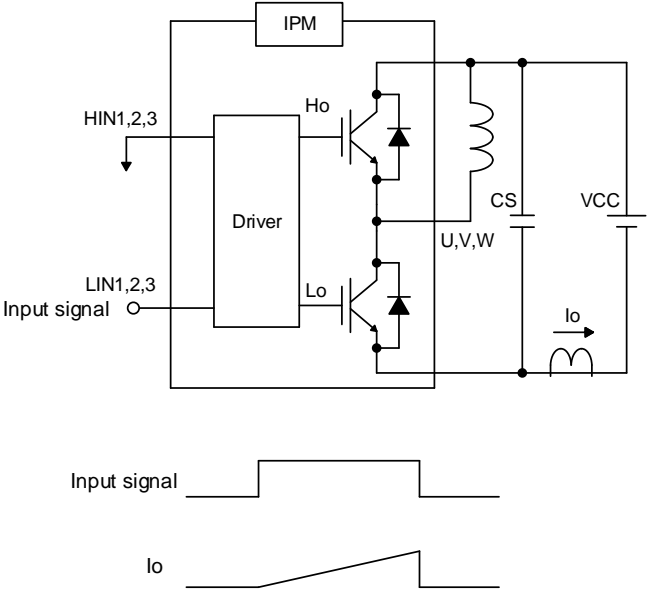


Figure 6. R.B.SOA circuit

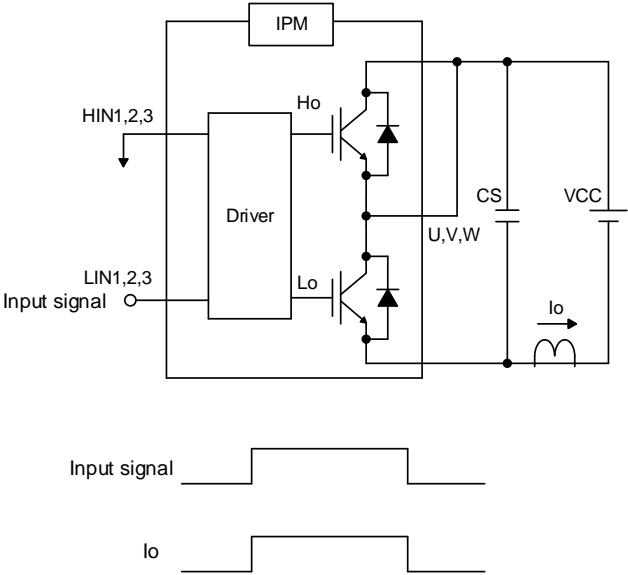


Figure 7. S.C.SOA circuit

3.2. Thermistor Characteristics

An integrated thermistor is used to sense the internal module temperature its electrical characteristic is outlined below.

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R ₂₅	T _c =25°C	99	100	101	kΩ
Resistance	R ₁₀₀	T _c =100°C	5.18	5.38	5.60	kΩ
B-Constant(25-50°C)	B		4208	4250	4293	K
Temperature Range			-40		+125	°C

Table 2. NTC Thermistor value

R₂₅ is the value of the integrated NTC thermistor at T_c=25°C. The resistance value is 100kΩ±1% and the value of the B-Constant (25-50°C) is 4250K±1%. The temperature depended value is calculated as shown in the formula.

$$R(t) = R_{25} \times e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

The resulting in the NTC values over temperatures

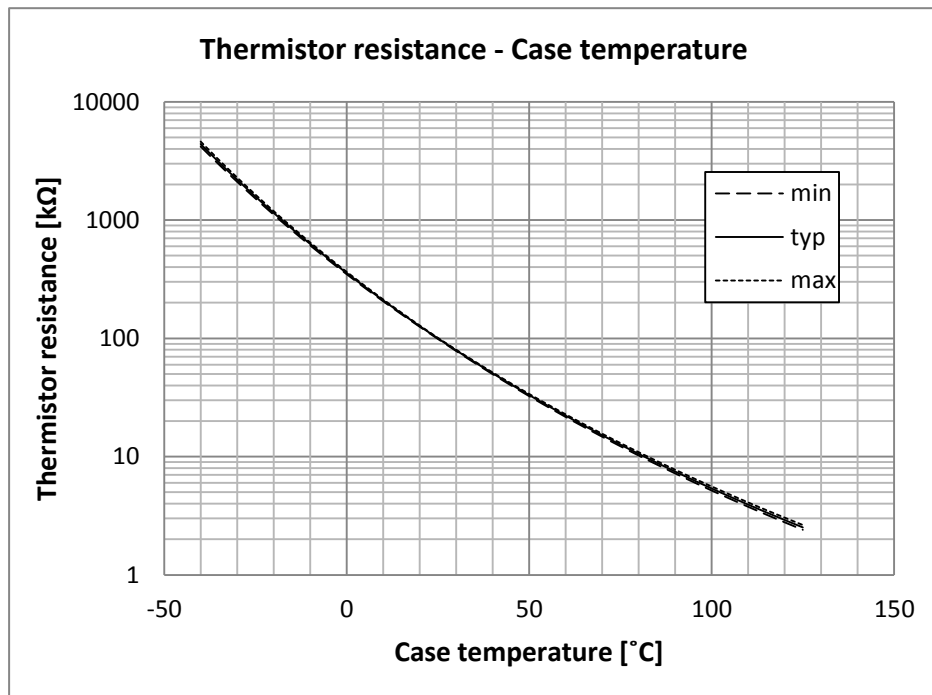


Figure 8. typical NTC value over temperature

4. Protective functions and Operation Sequence

This chapter describes the protection features.

- over current protection
- short circuit protection
- under Voltage Lockout (UVLO) protection
- cross conduction prevention

4.1. Over current protection

Over current protection is implemented by measuring the voltage across a shunt resistor to the negative supply terminal. In case of an OCP fault the gate drivers are shut down internally and the external Fault signal becomes active (low). The trip level of the over current protection current is programmable with an external resistance RSD between the ISD and VSS terminals as shown in over current protection Figure 9.

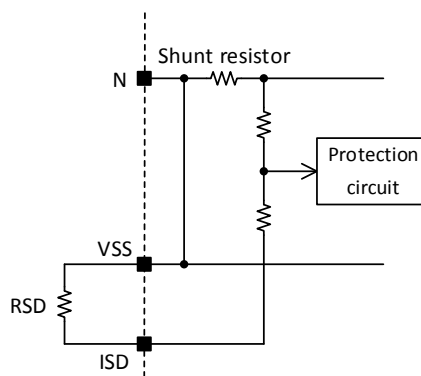


Figure 9. over current protection circuit

Once activated by a fault condition the FAULT signal output returns to inactive (and is pulled high by the external resistor) when the fault condition is over and the fault clear time (FLTCLR) has passed. This implies that the system microcontroller needs to disable all input signals to the module by driving them low upon detection of a fault condition.

The OCP trip level is programmed within the default or lower levels by an external resistor (RSD) between the ISD and VSD pins according to Figure 10 and 11. When the default level is used both terminals must be shorted e.g. by a 0Ω resistor.

Note 1: One should be aware that the “N” and the “VSS” pins are internally connected. Therefore an external short between these pins can cause the OCP level to be lower than desired.

Note 2: In order to prevent false OCP events due to switching noise and recovery current – a blanking time of some microseconds is implemented. This blanking time will also filter repetitive short high current pulses without tripping the OCP.

STK531U3xx series Application Note

External Resistance (RSD) [Ω]	Over Current Protection (ISD) [A]		
	min	typ	max
0	18.1	20.5	22.9
200	16.7	18.8	21.1
390	15.9	18.0	20.1
560	15.5	17.4	19.5
1000	14.8	16.6	18.6
2200	14.0	15.8	17.6
4700	13.6	15.3	17.0
10000	13.3	15.0	16.7
Open	13.1	14.7	16.4

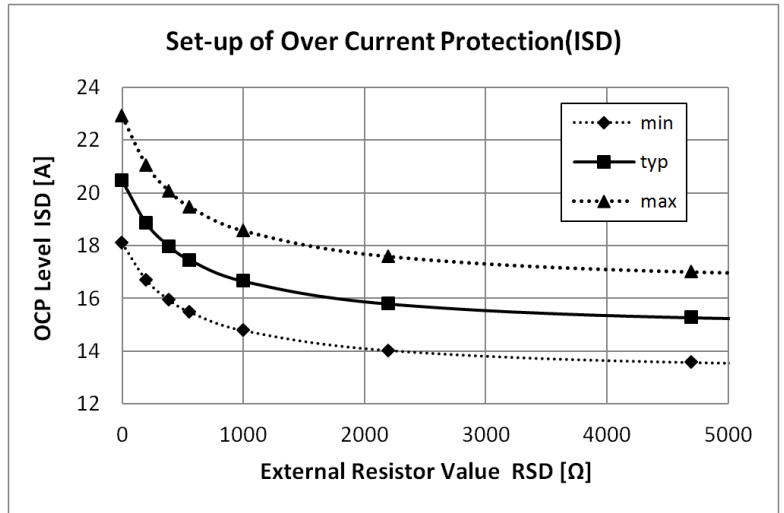


Figure 10. STK531U36xA-E RSD values and resulting ISD curve

External Resistance (RSD) [Ω]	Over Current Protection (ISD) [A]		
	min	typ	max
0	22.0	24.8	27.8
200	21.0	23.7	26.5
390	20.4	23.0	25.7
560	20.0	22.6	25.2
1000	19.4	21.8	24.3
2200	18.6	20.9	23.3
4700	18.1	20.3	22.6
10000	17.7	20.0	22.2
Open	17.4	19.6	21.8

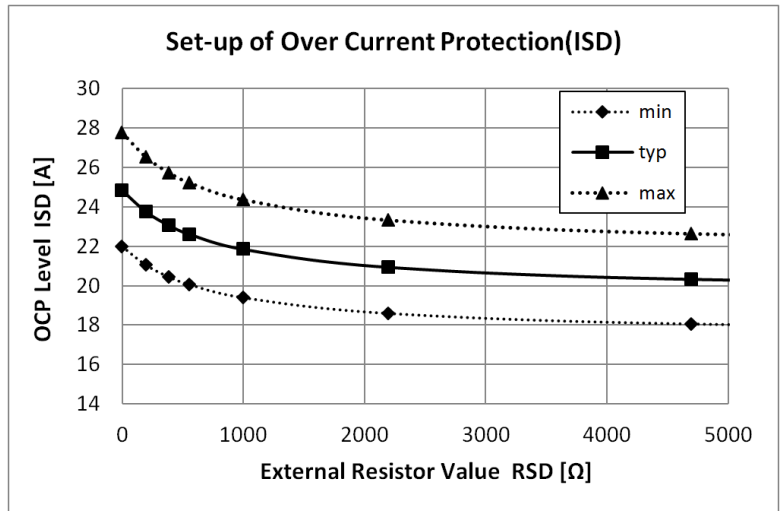


Figure 11. STK531U39xA-E RSD values and resulting ISD curve

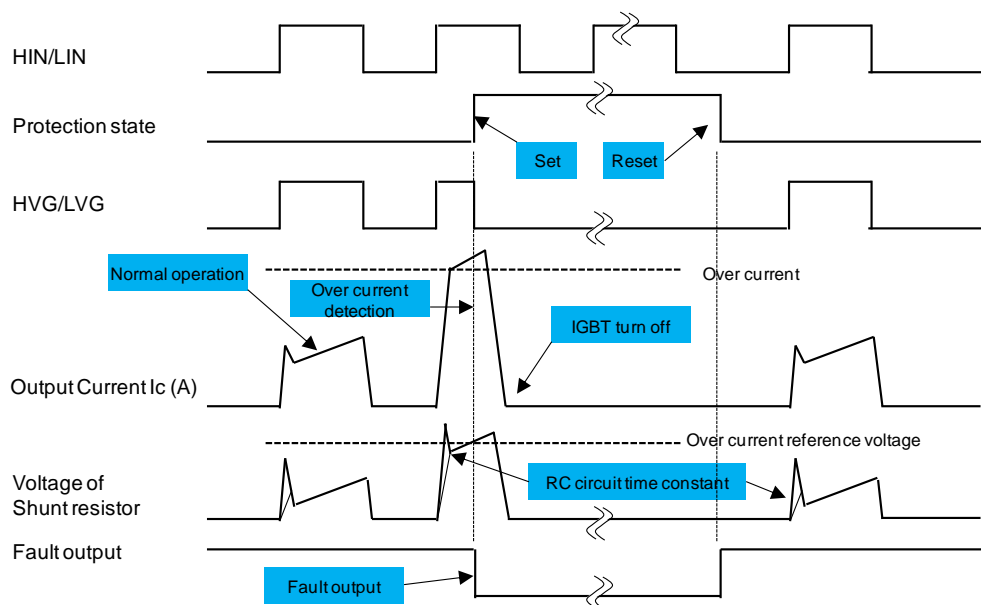


Figure 12. Over current protection Timing chart

4.2. Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 3. Both High-side and Low-side have UV protecting function. However the fault signal output only corresponds to the Low-side UVLO Protection. During the UVLO state the fault output is continuously driven (low).

VDD Voltage (typ. Value)	Operation behavior
< 12.5V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. rating is 20 V.

Table 3. Module operation according to control supply voltage

The sequence of events in case of a low side UVLO event (IGBTs turned off and active fault output) is shown in Figure 13. Figure 14 shows the same for a high side UVLO (IGBTs turned off and no fault output).

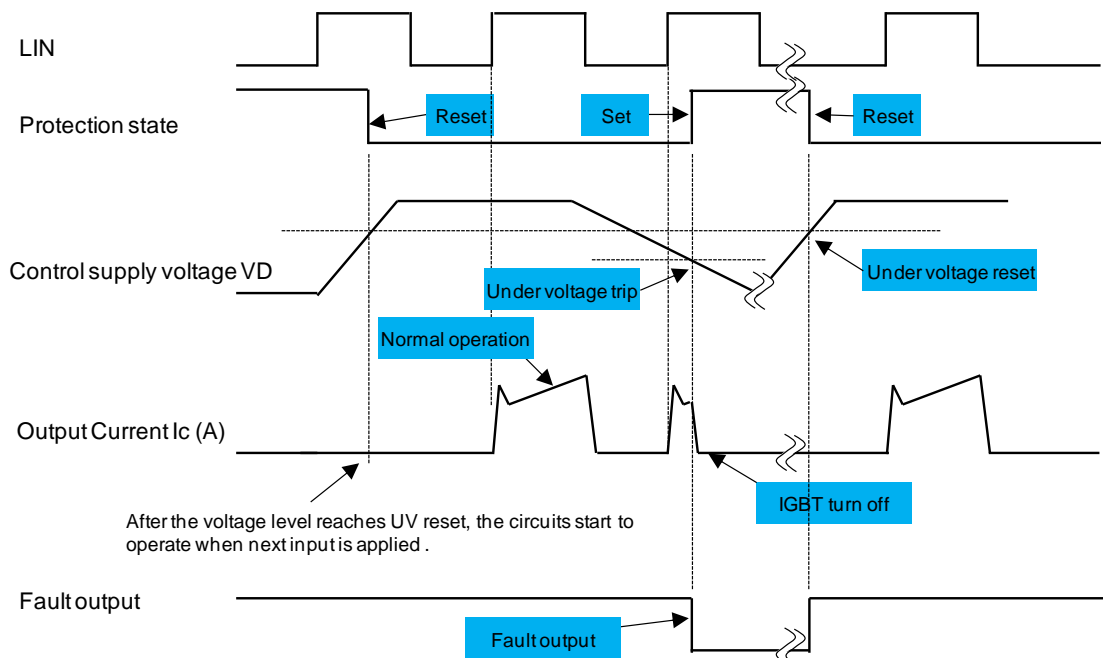


Figure 13. Low side UVLO timing chart

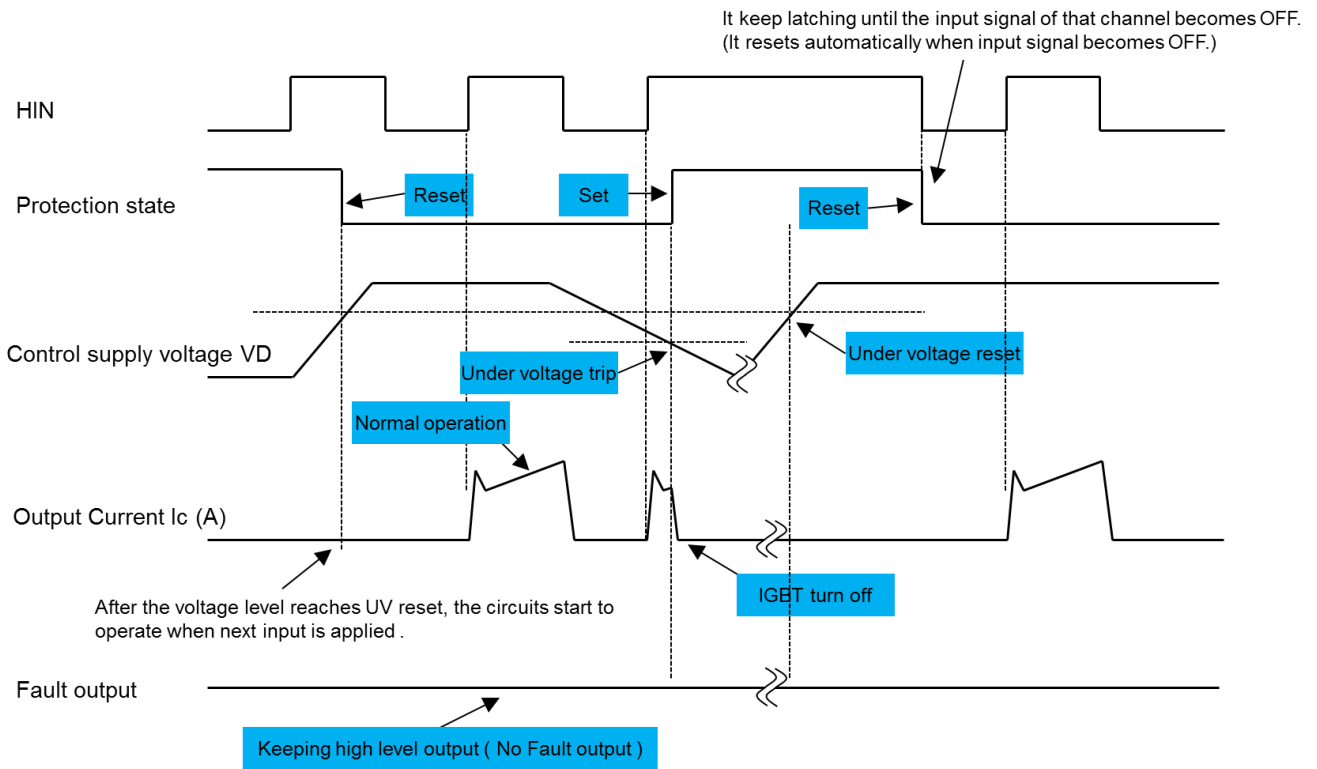


Figure 14. High side UVLO timing chart

4.3. Cross conduction prevention

The STK531U3xx series module implement a cross conduction prevention logic at the pre-driver to avoid simultaneous drive of the low- and high-side IGBTs as shown in Figure 15.

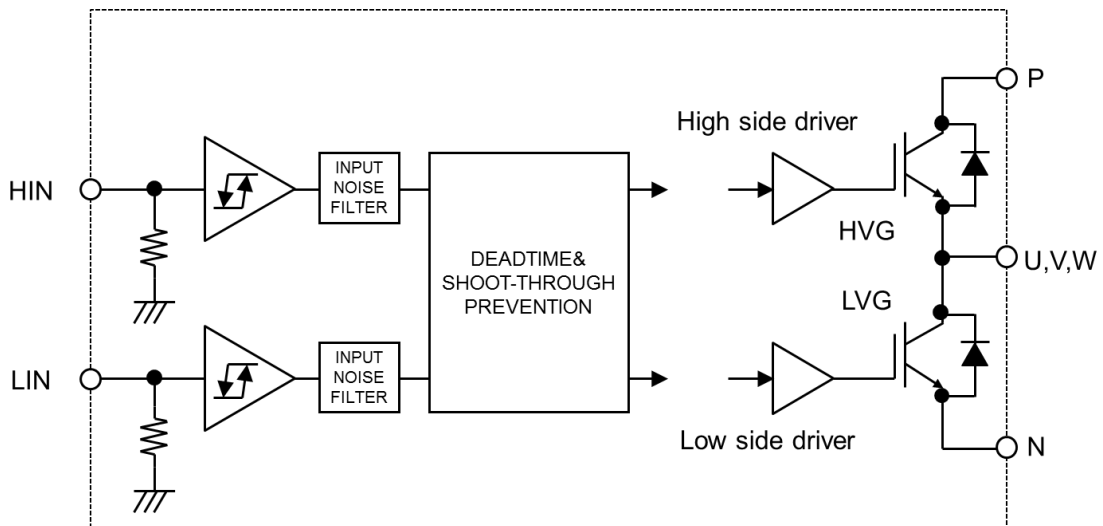


Figure 15. Cross Input Conduction Prevention

In case of both high and low side drive inputs are active (high) the logic prevents both gates from being driven – a corresponding timing diagram can be found in Figure 16 below.

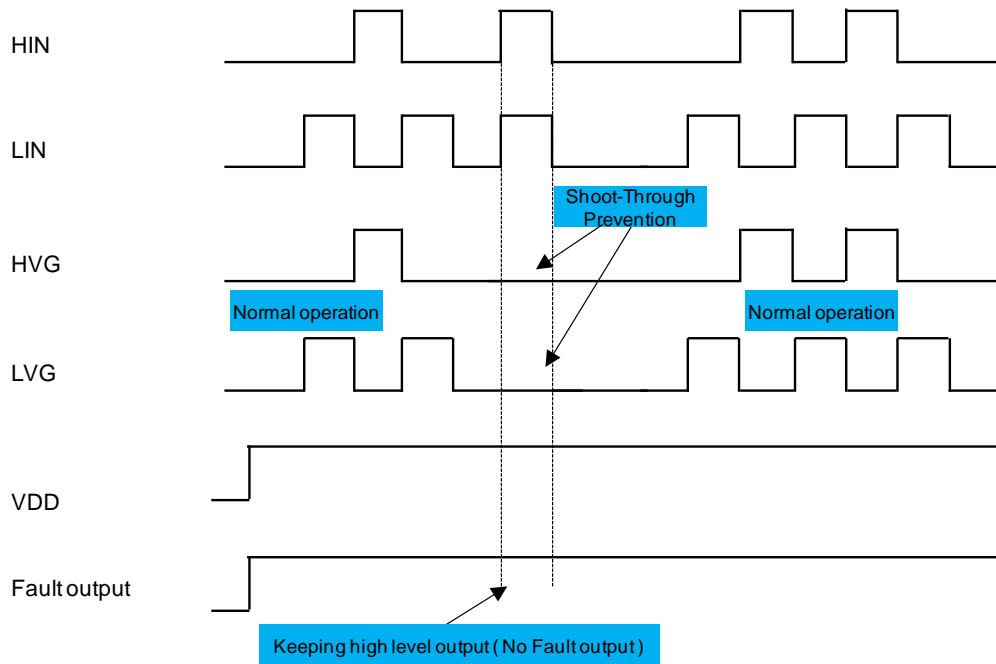


Figure 16. cross conduction prevention timing diagram

Even so cross conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs. Figure 17 shows the delay from the HIN-input via the internal HVG to high side IGBT, the similar path for the low side and the resulting minimum dead time which is equal to the potential shoot through period:

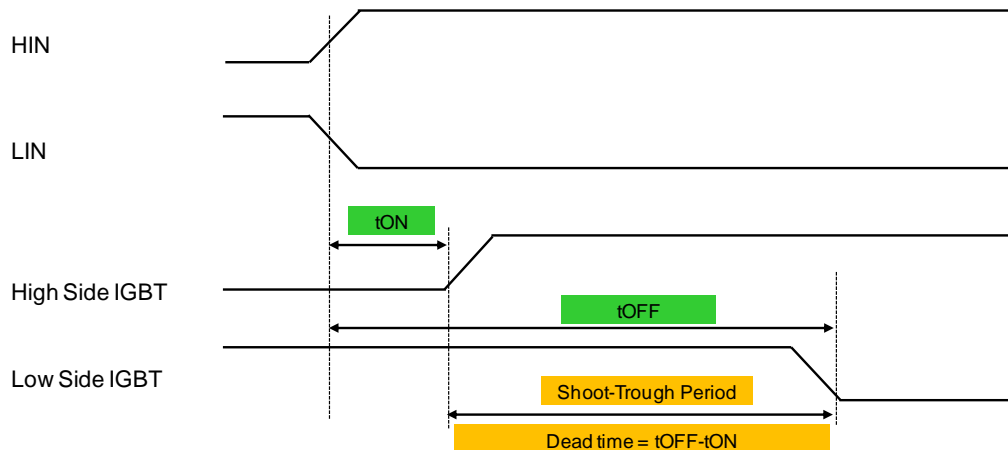


Figure 17. Shoot Trough Period

5. PCB design and mounting guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

5.1. Application (schematic) design

The following figures 18 gives an overview of the external circuitry's functionality when designing with the STK531U3xx series module.

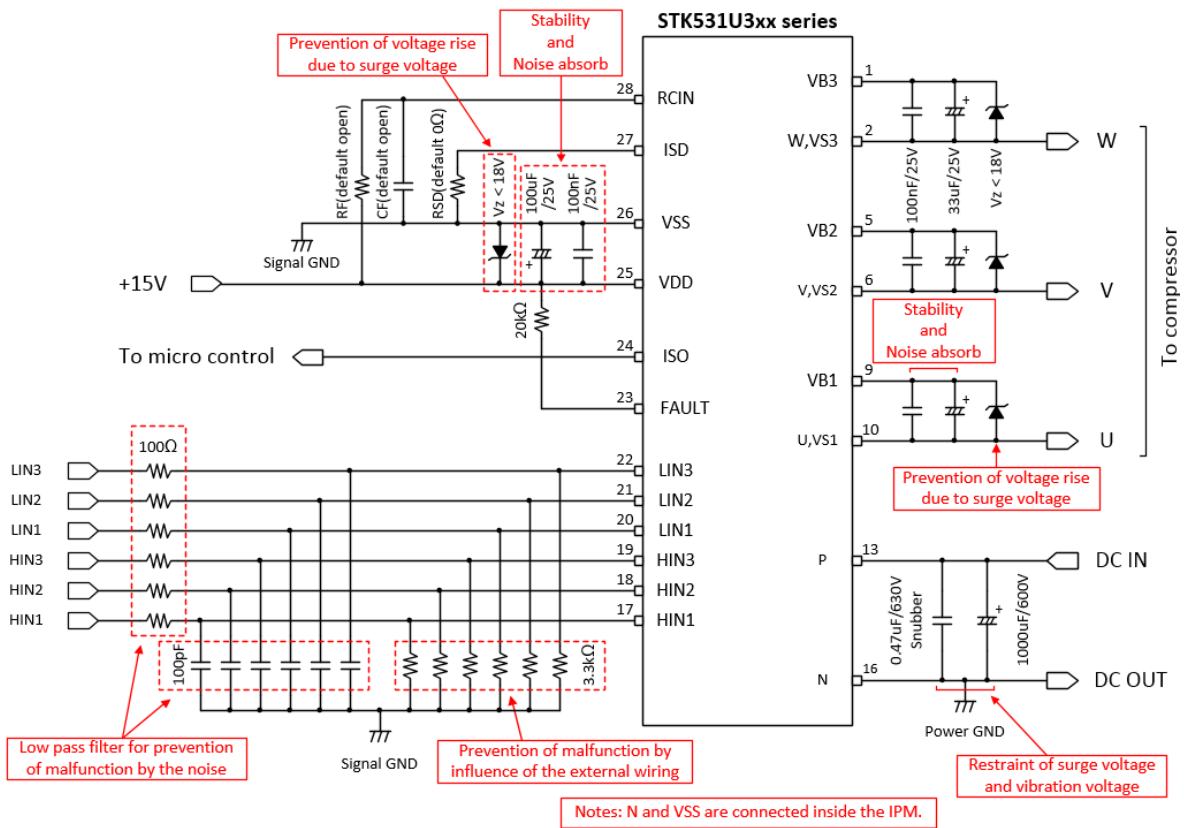


Figure 18. STK531U3xx series application circuit

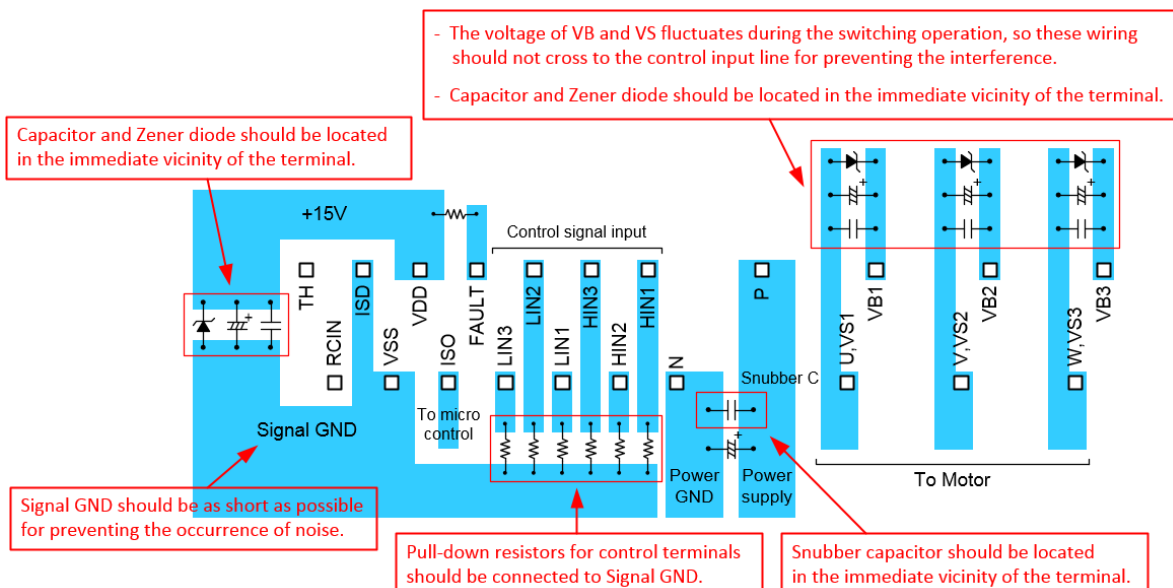


Figure 19. PCB design reference

5.2. Pin by pin design and usage notes

This section provides pin by pin PCB layout recommendations and usage notes. For a complete list of module pins refer to the datasheet or Chapter 6.

P, N These pins are connected with the main DC power supply. The applied voltage is up to the Vcc level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.

U, V, W These terminals are the output pins for connecting the 3-phase motor. They share the same GND potential with each of the high side control power supplies. Therefore they are also used to connect the GND of the of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD, VSS These pins connect with the circuitry of the internal protection and pre-drivers for the low -side power elements and also with the control power supply of the logic circuitry. Voltage to input these terminals is monitored by the under voltage protection circuit.

The VSS terminal is the reference voltage for the control inputs signals as well as Fault and ISO. VSS is connected with the “N” terminal internally. The main circuit does typically not draw current from VSS.

When the “N” and “VSS” pins are connected externally care must be taken to select a single connection point as close as possible to the IC. In case of multiple connections to these pins and longer traces being used, the overcurrent protection level may become low. Therefor this should be avoided.

VB1, VB2, VB3 The VBx pins are internally connected to the positive supply of the high-side drivers. The supply needs to be floating and electrically isolated. The boot-strap circuit shown in Figure 20 forms this power supply individually for every phase. Due to integrated boot resistor and diode (RB & DB) only an external boot capacitor (CB) is required.

CB is charged when the following two conditions are met.

- ① Low-side signal is input
- ② Motor terminal voltage is low level

The capacitor is discharged while the high-side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high side and the switching frequency into account.

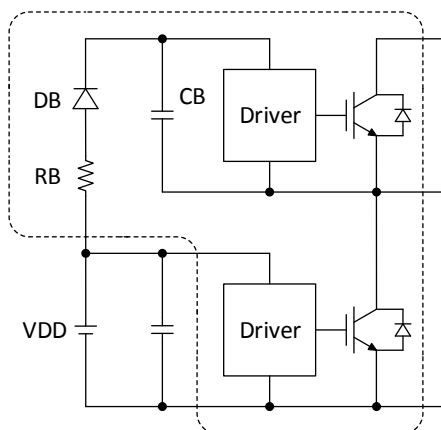


Figure 20. Boot Strap Circuit

The voltages on the high side drivers are individually monitored by the under voltage protection circuit. In case an UVP event is detected on a phase its operation is stopped.

Typically a CB value of less or equal 47uF ($\pm 20\%$) is used. In case the CB value needs to be higher an external resistor (of apx. 20 Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

HIN1, LIN1, HIN2, LIN2, HIN3, LIN3

These pins are the control inputs for the power stages. The inputs on HIN1/HIN2/HIN3 control the high-side transistors of U/V/W, and the inputs on LIN1/LIN2/LIN3 control the low-side transistors of U/V/W respectively. The input are active high and the input thresholds V_{IH} and V_{IL} are 5V compatible to allow direct control with a microcontroller system

Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead-time.

The equivalent input stage circuit is shown in Figure 21.

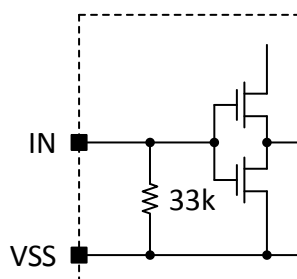


Figure 21. Internal Input Circuit

For fail safe operation the control inputs are internally tied to VSS via a 33k Ω (typ) resistor. To avoid switching captured by external wiring to influence the module behavior an additional external low-ohmic pull-down resistor with a value of 2.2k Ω -3.3k Ω should be used.

The output might not respond when the width of the input pulse is less than 1 μ s (both ON and OFF).

Fault

The Fault pin is an active low output (open-drain output). It is used to indicate an internal fault condition of the module. The structure is shown in Figure 22.

The sink current of I_{oSD} during an active fault is nominal 2mA @ 0.1V. Depending on the interface supply voltage the external pull-up resistor (RP) needs to be selected to set the low voltage below the VIL trip level.

For the commonly used supplies VP:

$VP = 15V \rightarrow RP \geq 20k\Omega$

$VP = 5V \rightarrow RP \geq 6.8k\Omega$

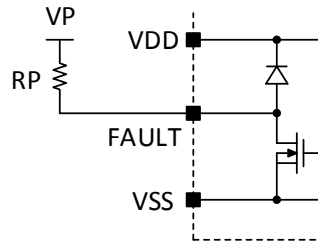


Figure 22. Fault Connection

For a detailed description of the fault operation refer to Chapter 4.

Note: The Fault signal does not latch permanently. After the protection event ended and the fault clear time(min. 18ms) passed, the module operation is automatically re-started. Therefore the input needs to be driven low externally activated as soon as a fault is detected.

ISO

The ISO pin allows monitoring the output voltage of the integrated current sense amplifier. This pin is usually left unconnected. Any external circuitry needs to have an impedance higher than 5.6kΩ.

Note: In case this pin is shorted to VSS – current sensing will not function.

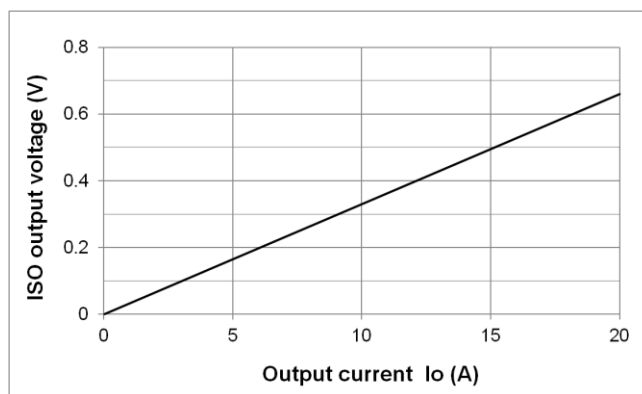


Figure 23. The output current (I_o) vs ISO characteristics (STK531U36xA-E)

TH

An internal thermistor to sense the substrate temperature is connected between TH and VSS. By connecting an external pull-up resistor to arbitrary voltage, the module temperature can be monitored. Please refer to heading 3.2 for details of the thermistor.

Note: This is the only means to monitor the substrate temperature indirectly.

RCIN

This pin is used to set the fault clear time. It is recommended to leave this pin open to select the default fault clear time of 18 ms.

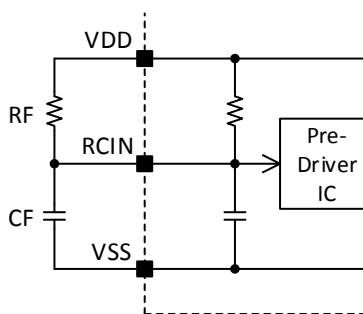


Figure 24. RCIN Circuit

To shorten the fault clear time, connect an external resistor R_F between VDD and RCIN. To lengthen the fault clear time, connect an external capacitor C_F between RCIN and VSS.

5.3. Heat sink mounting and torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately. This can lead to an inability of the device to provide its inherent performance, a serious reduction in reliability, or even destruction, burst and burn of the device due to overheating.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
 - There must be no burrs on aluminum or copper heat sinks.
 - Screw holes must be countersunk.
 - There must be no unevenness in the heat sink surface that contacts IPM.
 - There must be no contamination on the heat sink surface that contacts IPM.
2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount IPM on a heat sink. Upon re-mounting apply silicone grease(100um to 200um) again uniformly.
3. For an intimate contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack. The standard heat sink mounting condition of STK531U3xx series is as follows.

Item	Recommended Condition
Pitch	40.6 ± 0.1mm (Please refer to Package Outline Diagram)
Screw	diameter : M3 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D:7mm, d:3.2mm and t:0.5mm (Fig.2) JIS B 1256
Heat sink	Material : copper or Aluminum Warpage (the surface that contacts IPM) : -50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Final tightening : 0.6 to 0.9Nm Temporary tightening : 20 to 30 % of final tightening
Grease	Silicon grease Thickness : 100 to 200 μm Uniformly apply silicon grease to whole back. (Fig.3)

Table 4. heat sink mounting

Fig 1 : mount IPM on a Heat Sink

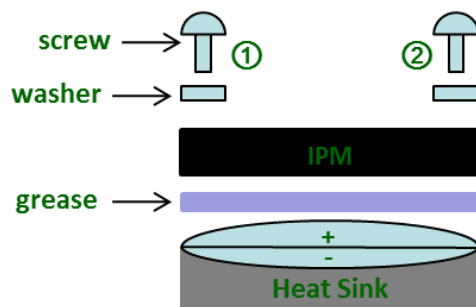


Fig 2 : size of washer

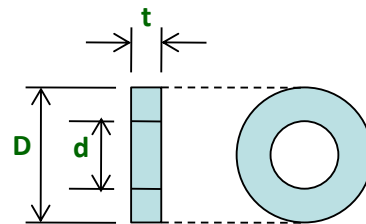
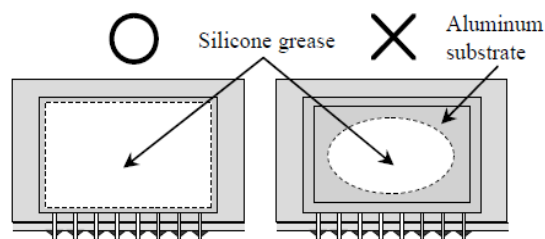


Fig 3 : About uniformly application



Steps to mount an IPM on a heat sink

1st: Temporarily tighten maintaining a left/right balance.

2nd : Finally tighten maintaining a left/right balance.

5.4. Mounting and PCB considerations

In designs in which the printed circuit board and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that a moving IPM is forcibly fixed to the heat sink with a screw.

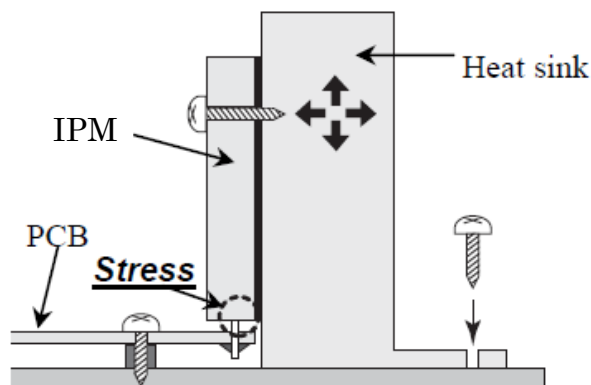
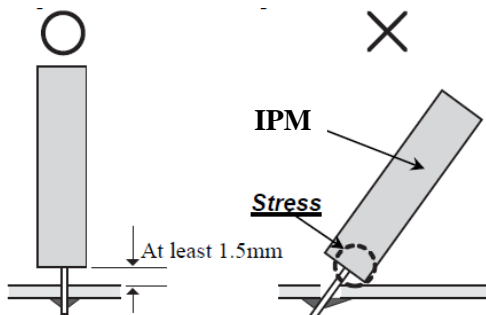


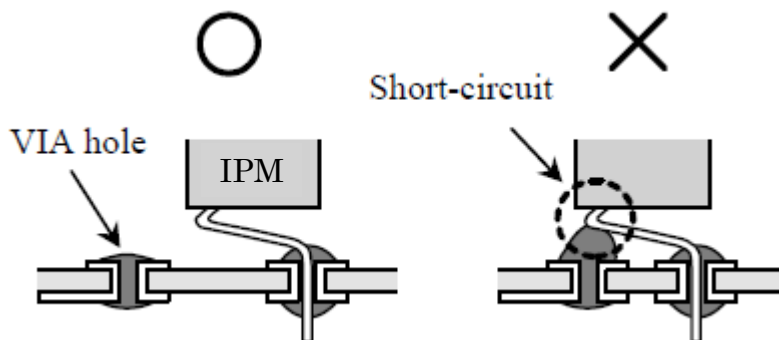
Figure 25. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the printed circuit board. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the printed circuit board.

Do not mount IPM with a tilted orientation. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the printed circuit board. Always mount the IPM vertically. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out. Be careful of this point.



When designing the PCB layout take care that the bent part portion of the lead frame pins does not short-circuit to VIA holes or tracks on the PCB.



Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

STK531U3xx series Application Note

IPMs are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the IPM should also be flame retardant.

Mounting on a Printed Circuit Board

1. Align the lead frame with the holes in the printed circuit board and do not use excessive force when inserting the pins into the printed circuit board. To avoid bending the lead frames, do not try to force pins into the printed circuit board unreasonably.
2. Do not insert IPM into printed circuit board with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPM may be destroyed, exploded, burned or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

5.5. Cleaning

IPM has a structure that is unable to withstand cleaning. As a basic policy, do not clean independent IPM or printed circuit boards on which an IPM is mounted.

6. Package Outline

STK531U3xx series is SIP05 package. (Single-inline-package)

Every second pin is bent forward to form two rows on the PCB see Figure 26.

6.1. Package outline and dimension

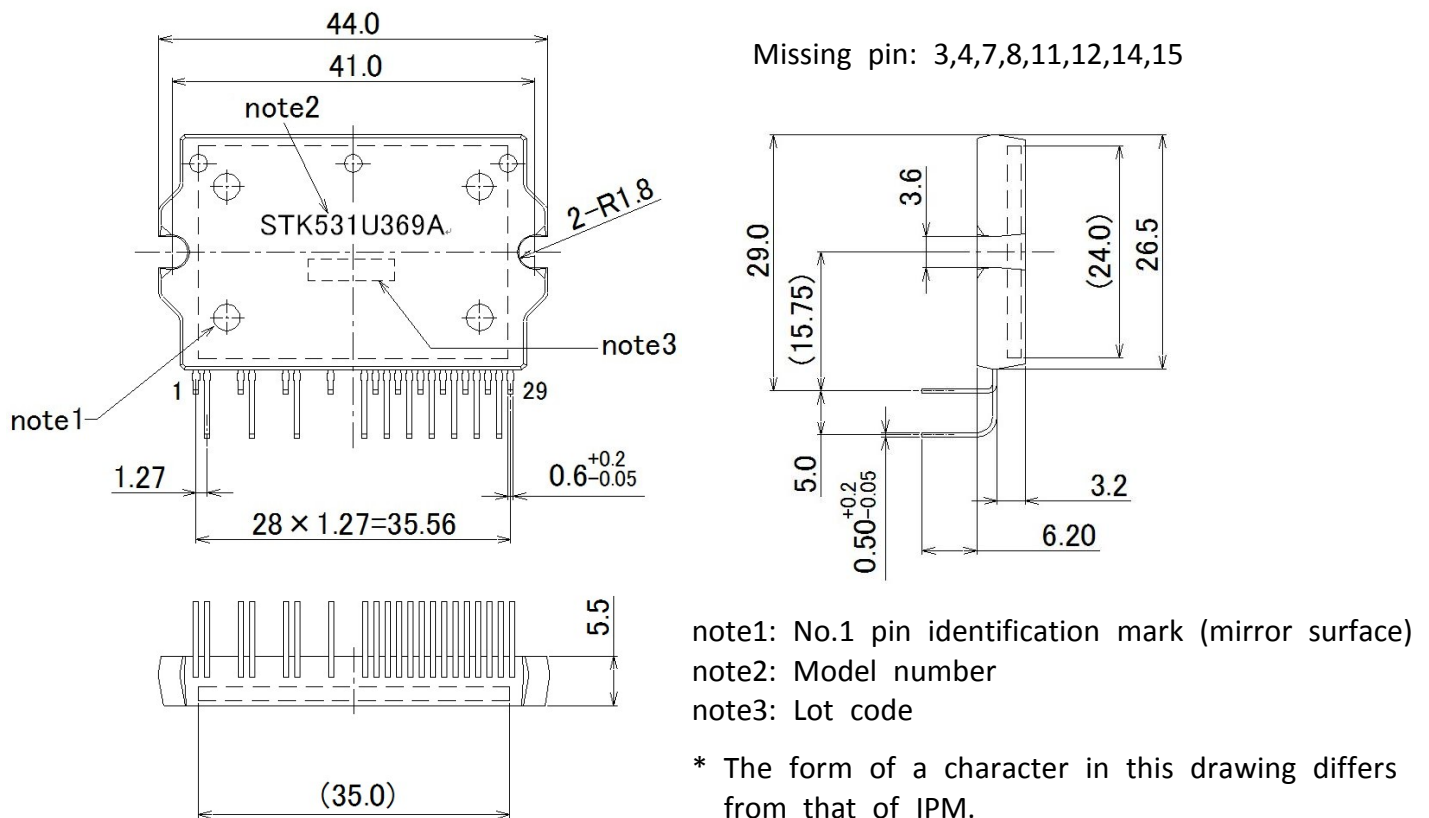


Figure 26. STK531U3xx series Package Outline

6.2. Pin Out Description

Pin	Name	Description
1	VB3	High Side Floating Supply Voltage 3
2	W, VS3	Output 3 - High Side Floating Supply Offset Voltage
3	NA	none
4	NA	none
5	VB2	High Side Floating Supply voltage 2
6	V,VS2	Output 2 - High Side Floating Supply Offset Voltage
7	NA	none
8	NA	none
9	VB1	High Side Floating Supply voltage 1
10	U,VS1	Output 1 - High Side Floating Supply Offset Voltage
11	NA	none
12	NA	none
13	P	Positive Bus Input Voltage
14	NA	none
15	NA	none
16	N	Negative Bus Input Voltage
17	HIN1	Logic Input High Side Gate Driver - Phase 1
18	HIN2	Logic Input High Side Gate Driver - Phase 2
19	HIN3	Logic Input High Side Gate Driver - Phase 3
20	LIN1	Logic Input Low Side Gate Driver - Phase 1
21	LIN2	Logic Input Low Side Gate Driver - Phase 2
22	LIN3	Logic Input Low Side Gate Driver - Phase 3
23	Fault	Fault Signal Output
24	ISO	Current Sensing Monitor
25	VDD	+15V Control Power Supply
26	VSS	Negative Control Power Supply
27	ISD	Over Current Protection Setting
28	RCIN	Fault Clear Time Setting
29	TH	Temperature Monitor

7. Demo Board

The demo board consists of the minimum required components such as snubber capacitor and bootstrap circuit elements of STK531U3xx series.

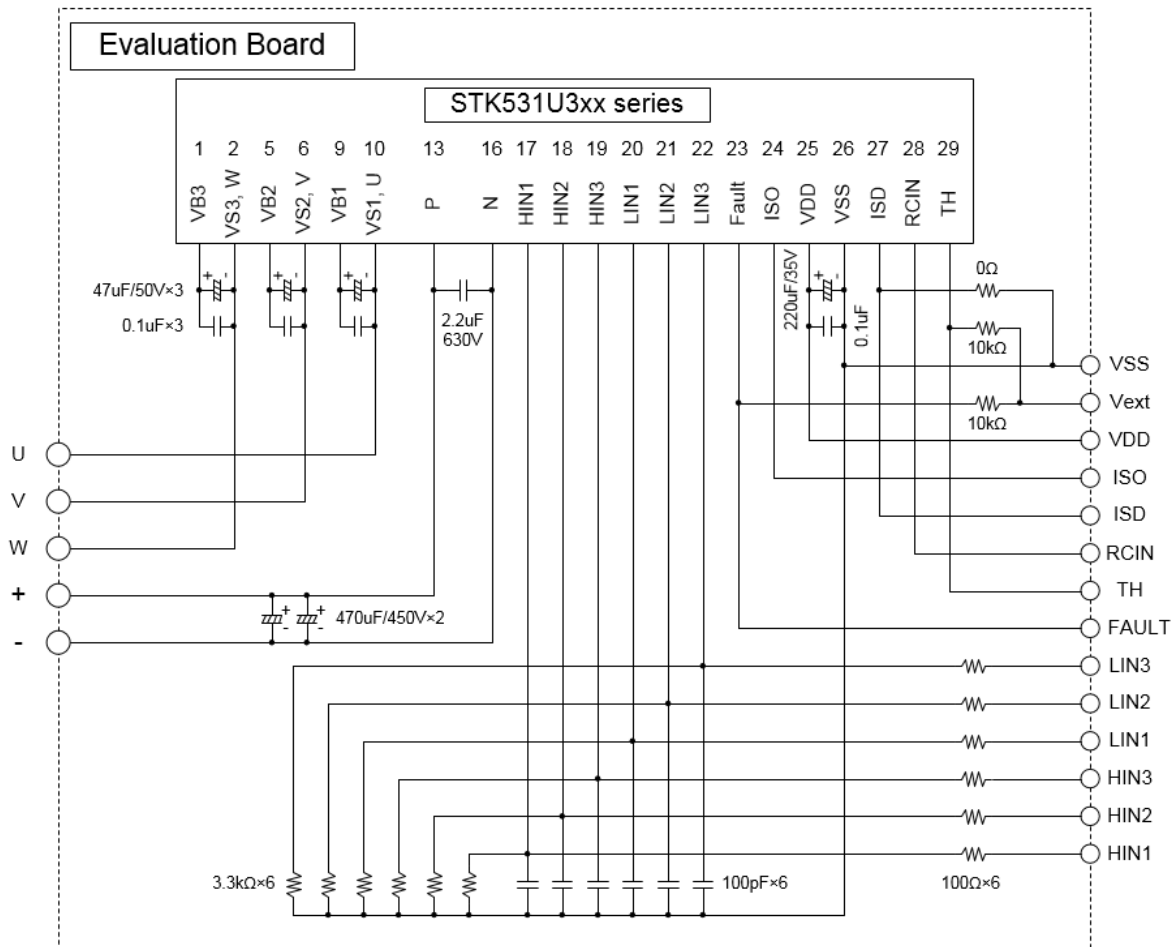


Figure 27. Evaluation board schematic

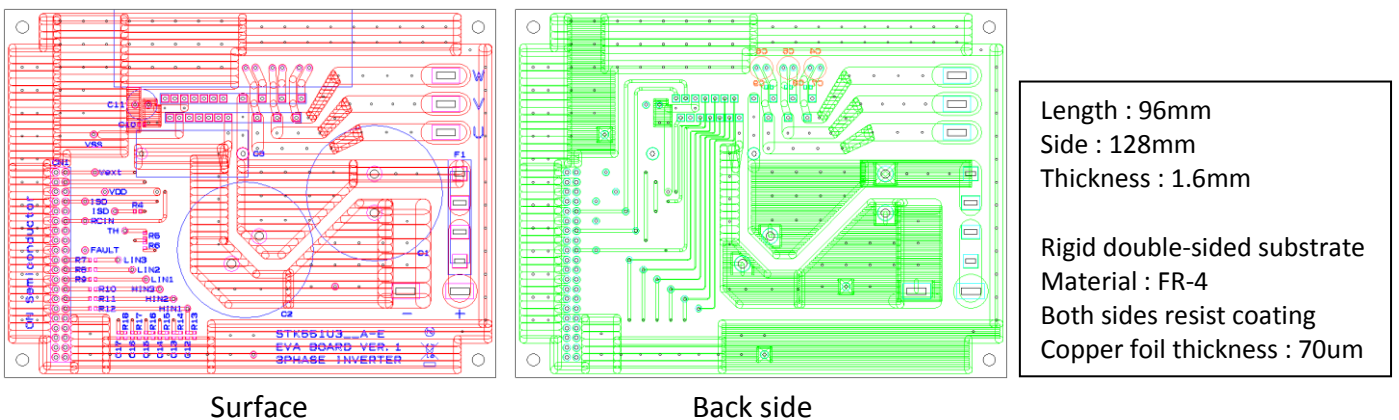


Figure 28. Evaluation board PCB layout (TOP view)

STK531U3xx series Application Note

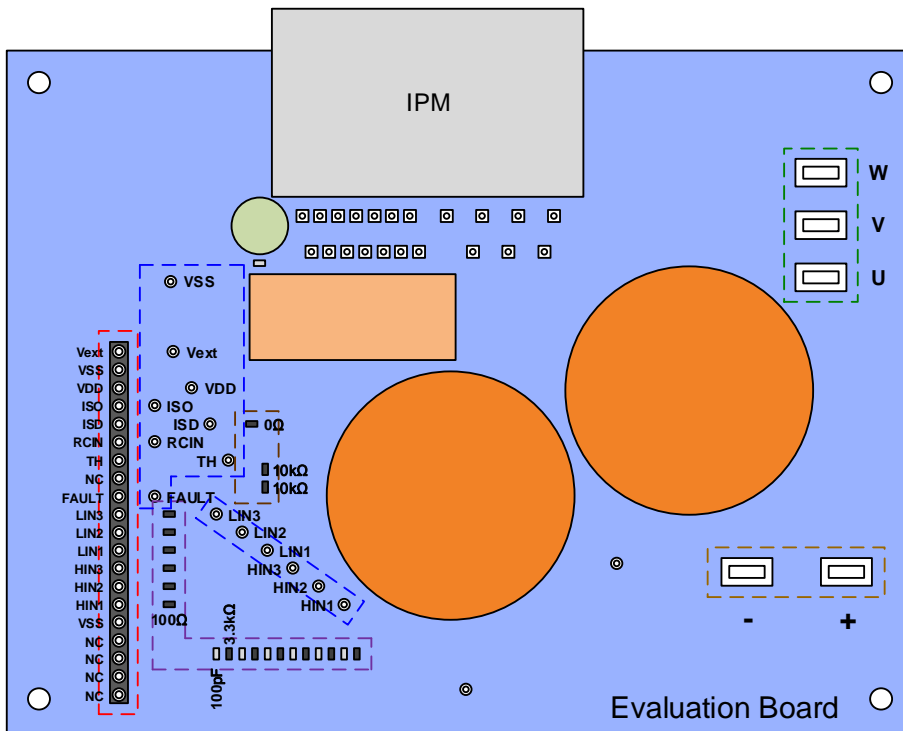


Figure 29. Description of each pin

Red frame: Connector

For the connection to the control part

Vext terminal is connected pull-up resistor from TH and fault. Please impress arbitrary voltage to this terminal.

Blue frame: Test pins

For monitoring each control signal

Purple frame: Low pass filter and pull-down resistor for control terminal

- Low pass filter is composed of resistor of 100Ω, and capacitor of 100pF.
- Pull-down resistor 3.3kΩ is for prevention of malfunction by external wiring.

Brown frame

ISD \rightarrow VSS Pull-down R(0Ω) for ISD

TH
Vext
Fault Pull-up R(10kΩ) for TH
Pull-up R(10kΩ) for Fault

Green frame: U,V,W terminal

Please connect to the motor.

Orange frame: +, - terminal

Please connect to DC power supply.

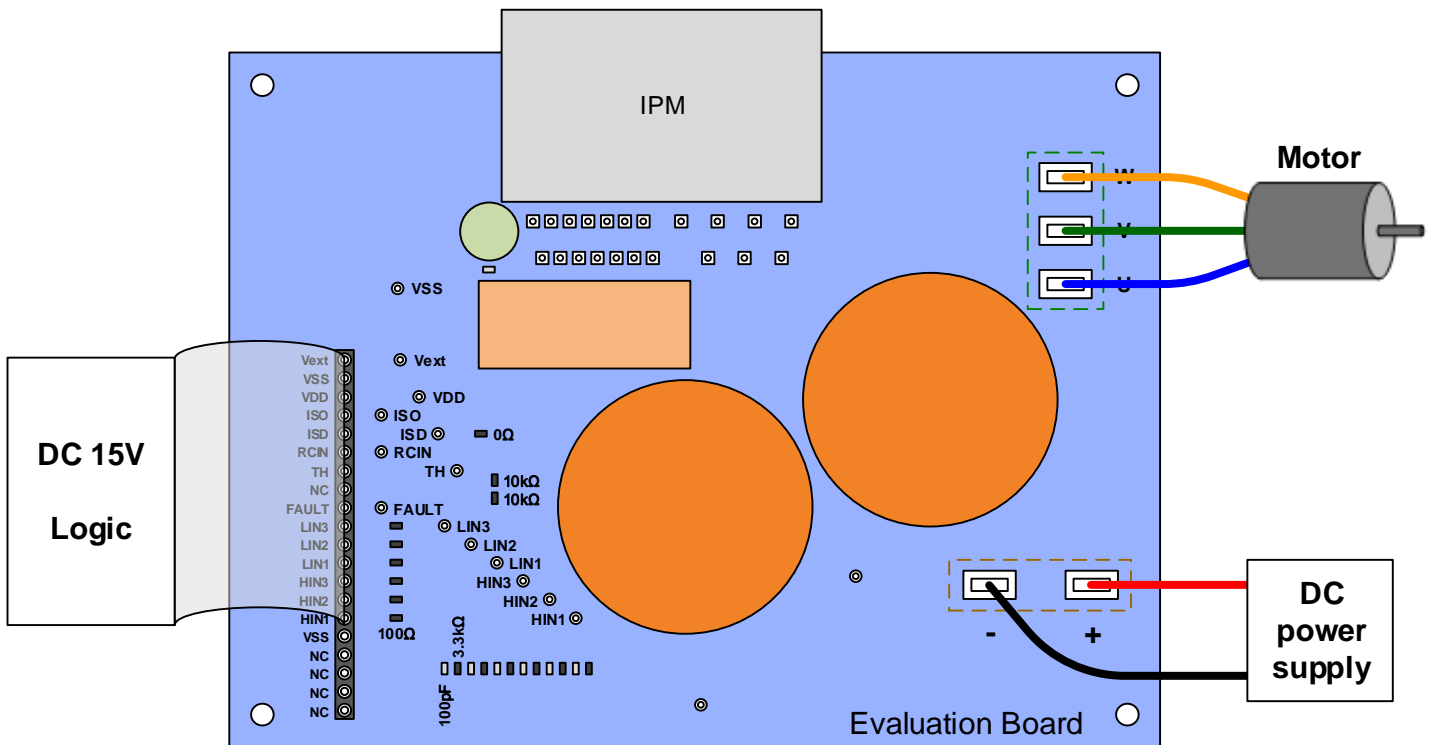


Figure 30. Evaluation board instructions

Operation procedure

- Step1:** Please connect IPM, each power supply, logic parts, and the motor to the evaluation board, and confirm that each power supply is OFF at this time.
- Step2:** Please impress the power supply of DC15V.
- Step3:** Please perform a voltage setup according to specifications, and impress the power supply between the "+" and the "-" terminal.
- Step4:** By inputting signal to the logic part, IPM control is started.
(Therefore, please set electric charge to the boot-strap capacitor of upper side to turn on lower side IGBT before running.)

* When turning off the power supply part and the logic part, please carry out in the reverse order to above steps.

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