ON Semiconductor

Is Now

To learn more about onsemi™, please visit our website at
www.onsemi.com

3-phase Inverter Power Module 1200 V SPM® 31 Series Application Note

AND9972/D

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

INTRODUCTION

This application note provides practical guidelines for designing with the SPM 31 Series power modules.

This series of Intelligent Power Modules (IPM) for 3−phase motor drives contains a three−phase inverter stage, gate drivers and a thermistor (Optional).

Design Concept

The SPM 31 design objective is to provide a minimized package and a low power consumption module with improved reliability. It is achieved by applying new gate−driving High−Voltage Integrated Circuit (HVIC), a new Insulated−Gate Bipolar Transistor (IGBT) of advanced silicon technology, and improved Direct Bonded Copper (DBC) substrate based on transfer mold package. The SPM 31 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as commercial air conditioners, general−purpose inverters and servo motors. The temperature sensing function of SPM 31 products are implemented in the LVIC to enhance the system reliability and isolated optional thermistor is available. The analog voltage proportional to the temperature of the LVIC and integrated thermistor temperature in module are provided for monitoring the module temperature and necessary protections against over−temperature situations. Figure 1 shows the package outline structure.

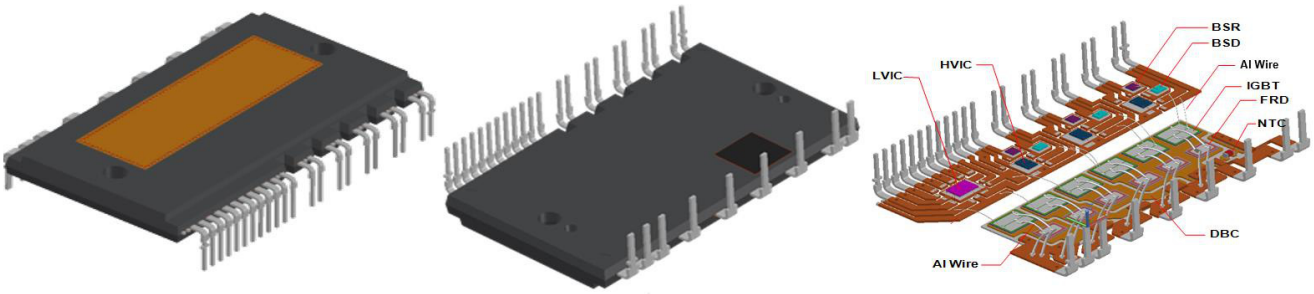


Figure 1. External View and Internal Structure of SPM 31

Key Features

- 1200 V / 5, 10, 20 A, three phase IGBT inverter including control ICs for gate driving and protections
- Very low thermal resistance by adopting DBC substrate
- Easy PCB layout thanks to built−in bootstrap circuits
- Open emitter configuration for easy monitoring of each phase current sensing
- Single−grounded power supply thanks to built−in HVICs and bootstrap operations
- Built−in temperature sensing function by LVIC and optional NTC
- Isolation Rating of 2500 Vrms / min

PRODUCT DESCRIPTION

Ordering Information

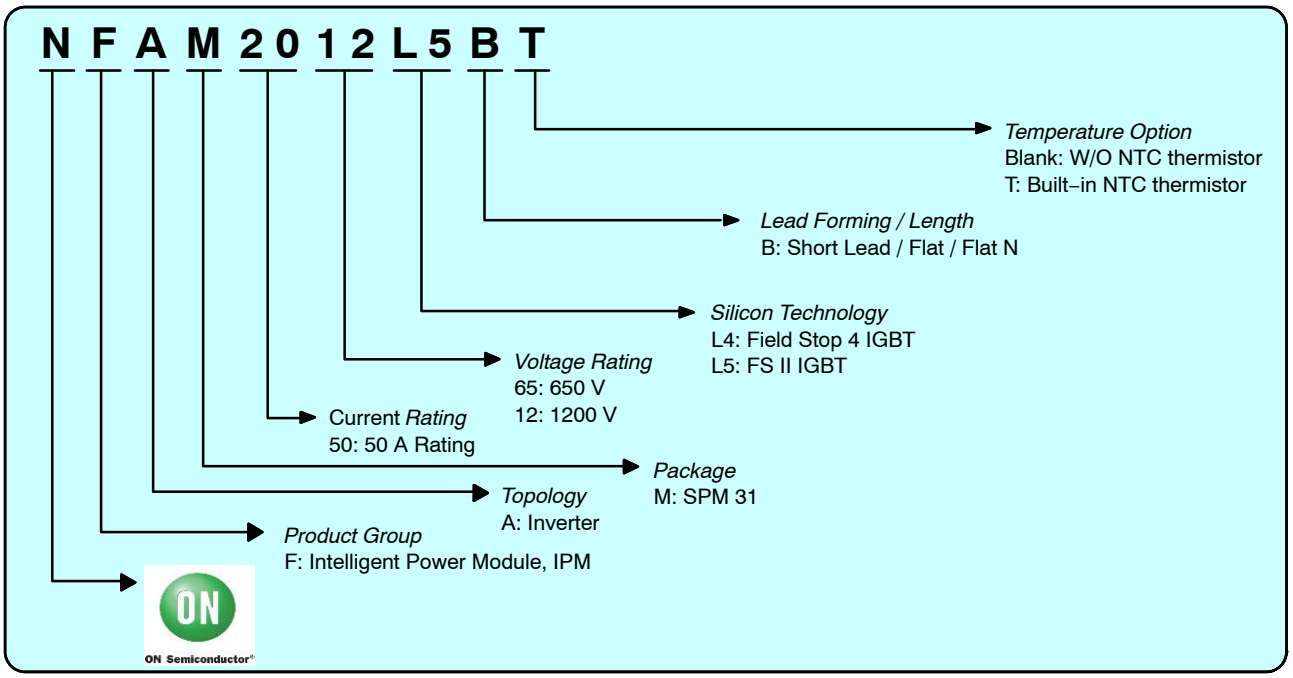


Figure 2. Ordering Information

Product Line−up

Table 1 shows the basic line up without package variations. Online loss and temperature simulation tool, Motion Control Design Tool is recommended to find out the right IPM product for the desired application. For package drawing, please refer to Chapter Package Outline.

Table 1. PRODUCT LINE−UP

Target Application	Device	IGBT Rating	Motor Rating (Note 1)	Isolation Voltage
Air Conditioners, Industrial Motor, General−purpose inverters, Servo motors	NFAM0512L5B(T)	5 A / 1200 V	0.75 kW	V_{ISO} = 2500 Vrms (Sine 60 Hz, 1−min All Shorted Pins Heat Sink)
	NFAM1012L5B(T)	10 A / 1200 V	1.5 kW	
	NFAM2012L5B(T)	20 A / 1200 V	2.2 kW	

1. These motor ratings are general ratings, so it can be changed by the operating conditions.

Internal Circuit Diagram

Three bootstrap circuits generate the voltage needed for driving the high−side IGBTs. The boost diodes are internal to the part and sourced from VDD (15 V). There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with opto−couplers.

Major differences between SPM 31 T version and normal version are shown on pins 38 and 39 of the internal circuit diagram as shown in Figure 3. The T version has built−in NTC that senses the temperature of the power chip. In normal version, NTC is not built in. Both T version and Normal version function as conventional functions LVIC temperature sensing signal is output from the VTS pin.

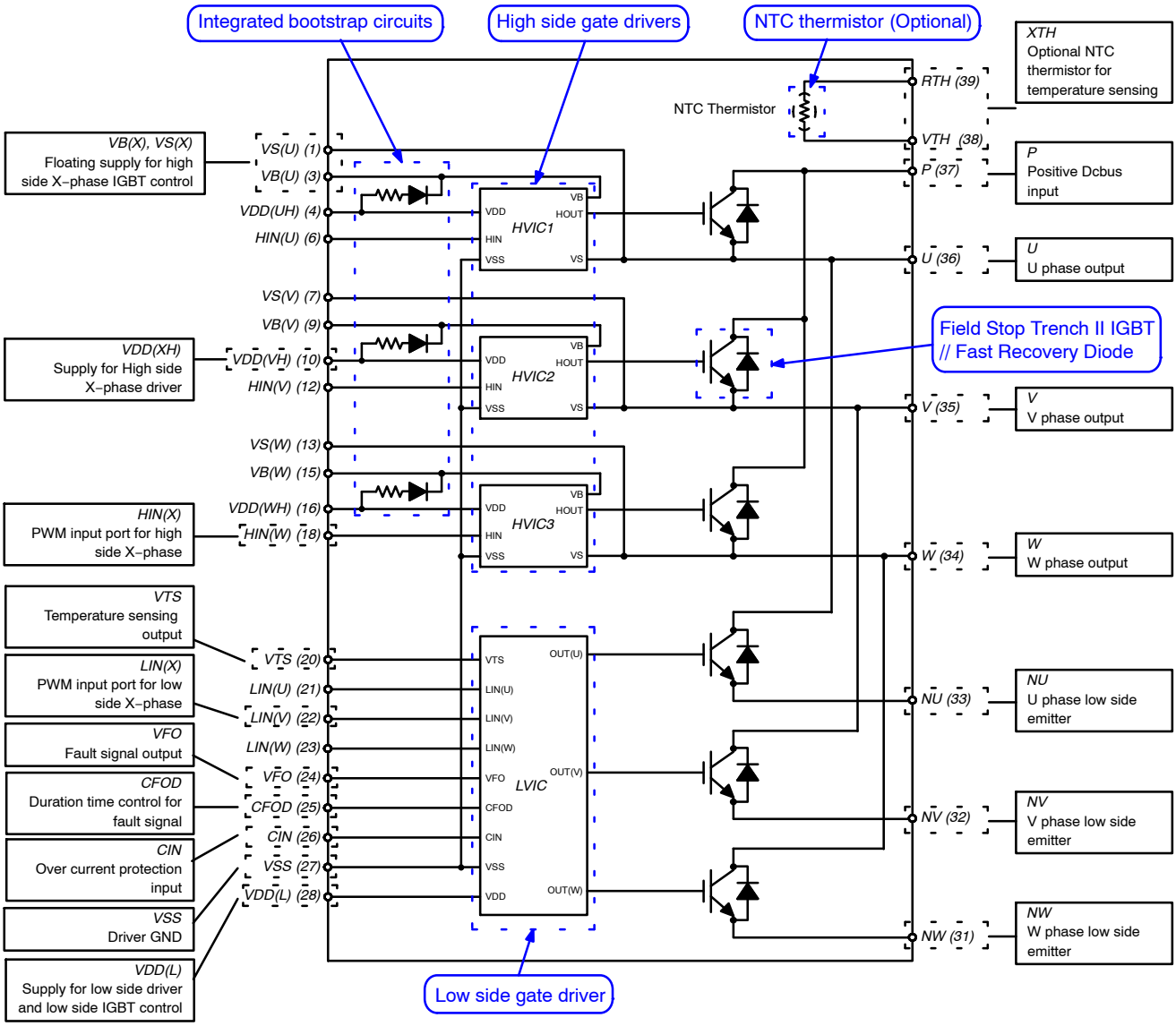


Figure 3. Internal Equivalent Circuit Diagram

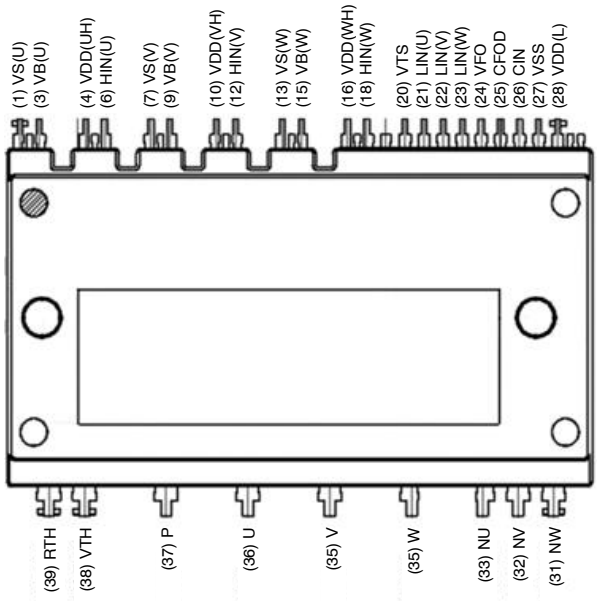


Figure 4. Package Top−View and Pin Assignment

Table 2. NUMBERS, NAMES AND DUMMY PINS

Pin Numbers	Names	Description
1	VS(U)	High−Side Bias Voltage GND for U Phase IGBT Driving
(2)	−	Dummy
3	VB(U)	High−Side Bias Voltage for U Phase IGBT Driving
4	VDD(UH)	High−Side Bias Voltage for U Phase IC
(5)	−	Dummy
6	HIN(U)	Signal Input for High−Side U Phase
7	VS(V)	High−Side Bias Voltage GND for V Phase IGBT Driving
(8)	−	Dummy
9	VB(V)	High−Side Bias Voltage for V Phase IGBT Driving
10	VDD(VH)	High−Side Bias Voltage for V Phase IC
(11)	−	Dummy
12	HIN(V)	Signal Input for High−Side V Phase
13	VS(W)	High−Side Bias Voltage GND for W Phase IGBT Driving
(14)	−	Dummy
15	VB(W)	High−Side Bias Voltage for W Phase IGBT Driving
16	VDD(WH)	High−Side Bias Voltage for W Phase IC
(17)	−	Dummy
18	HIN(W)	Signal Input for High−Side W Phase
(19)	−	Dummy
20	VTS	Voltage Output for LVIC Temperature Sensing Unit
21	LIN(U)	Signal Input for Low−Side U Phase
22	LIN(V)	Signal Input for Low−Side V Phase
23	LIN(W)	Signal Input for Low−Side W Phase
24	VFO	Fault Output

Table 2. NUMBERS, NAMES AND DUMMY PINS

Pin Numbers	Names	Description
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Over Current Protection
27	VSS	Low−Side Common Supply Ground
28	VDD(L)	Low−Side Bias Voltage for IC and IGBTs Driving
(29)	−	Dummy
(30)	−	Dummy
31	NW	Negative DC−Link Input for W Phase
32	NV	Negative DC−Link Input for V Phase
33	NU	Negative DC−Link Input for U Phase
34	W	Output for W Phase
35	V	Output for V Phase
36	U	Output for U Phase
37	P	Positive DC−Link Input
38	VTH	Thermistor Bias Voltage (T) / Not Connection
39	RTH	Series Resister for Thermistor (Temperature Detection) *Optional for T

2. Pins of ( ) are the dummy for internal connection. These pins should be no connection.

Detailed Pin Definition and Notification

Pins: VB(U) − VS(U), VB(V) − VS(V), VB(W) − VS(W)

- High−side bias voltage pins for driving the IGBT / high−side bias voltage ground pins for driving the IGBTs.
- VB(U), VB(V), VB(W) are integrated bootstrap diode cathode pins.
- These are drive power supply pins for providing gate drive power to the high−side IGBTs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high−side IGBTs. Each bootstrap capacitor is charged from the VDD supply during ON state of the corresponding low−side IGBT and Diode.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, a low−ESL filter capacitor should be mounted very close to these pins.

Pins: VDD(L), VDD(UH), VDD(VH), VDD(WH)

- Low−side bias voltage pins / high−side driver bias voltage pins.
- This is control supply pins for the built−in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a low−ESR, low−ESL filter capacitor should be mounted very close to these pins.

Pin: VSS

- Control signal ground pin.
- This is supply ground pin for the built−in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W)

- Signal input pins.
- These pins control the operation of the built−in IGBTs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt−trigger circuit composed of 5 V−class CMOS.
- The signal logic of these pins is active high. The IGBT associated with each of these pins is turned on.
- ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the SPM 31 against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 28 is recommended.

Pin: CIN

- Over−current and short−circuit detection input pin.
- The current sensing shunt resistor should be connected between the pin CIN and the low−side ground pin VSS to detect over or short circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.

Pin: VFO

- Fault output pin.
- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM 31.
- The alarm conditions are: Short−Circuit Current Protection (SCP), and low−side bias Under−Voltage Lock Out (UVLO).
- The VFO output is open drain configured. The VFO signal line should be pulled to the 5 V logic power supply with approximately 10 kΩ resistance.

Pin: CFOD

- Fault output duration time control pin.
- The fault−out pulse width time depends on the capacitance value of CFOD.

Pin: VTH, RTH (Optional for T type)

- For case temperature (Tc) detection, this pin should be connected to an external series resistor.
- The external series resistor should be selected to meet the detection range matched for the specification of each application (for details, refer to Figure 22).

Pin: VTS

- Analog temperature sensing output pin.
- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the IGBTs will increase the temperature of the LVIC.
- VTS versus temperature characteristics is illustrated in Figure 17.

Pin: P

- Positive DC−link pin.
- This is the DC−link positive power supply pin of the inverter.
- It is internally connected to the collectors of the high−side IGBTs.
- To suppress surge voltage caused by the DC−link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

Pins: NU, NV, NW

- Negative DC−link pins.
- These are the DC−link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low−side IGBT emitters of each phase.
- These pins are used to one shunt or three shunt resistor.

Pins: U, V, W

- Inverter power output pins.
- Inverter output pins for connecting to the inverter load (e.g. motor).

PACKAGE

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade−off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In SPM 31, technology was developed with DBC substrate that resulted in excellent heat dissipation characteristics. Power chips are attached directly to the DBC substrate. This technology is applied SPM 31, achieving improved reliability and heat dissipation.

Figure 5 and Figure 6 show the package outline and the cross−sections of the SPM 31 package.

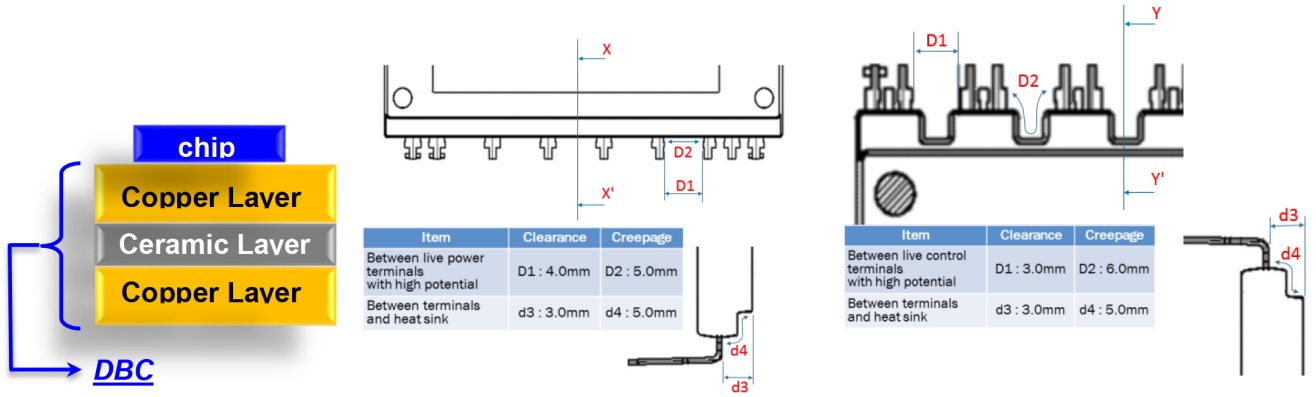


Figure 5. Vertical Structure for Heat Dissipation and Distance for Isolation

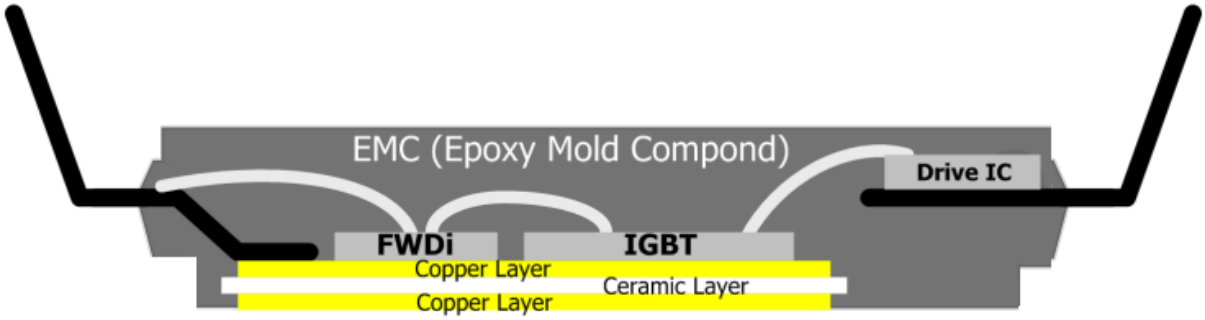
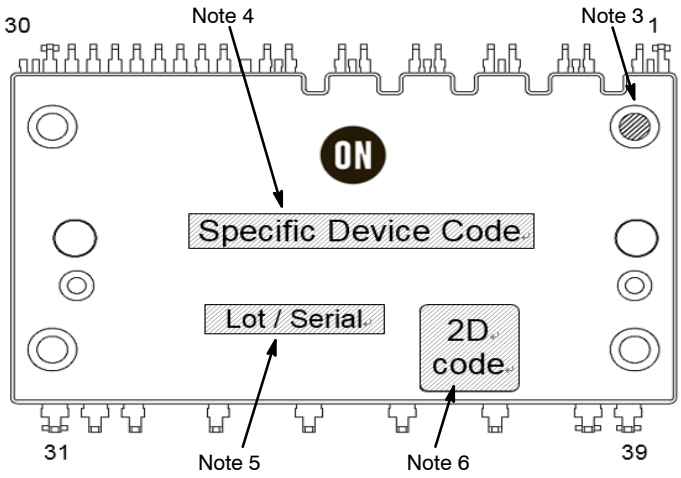


Figure 6. Package Structure and Cross Section for SPM 31

Marking Specification Base on NFAMxx12L5BT

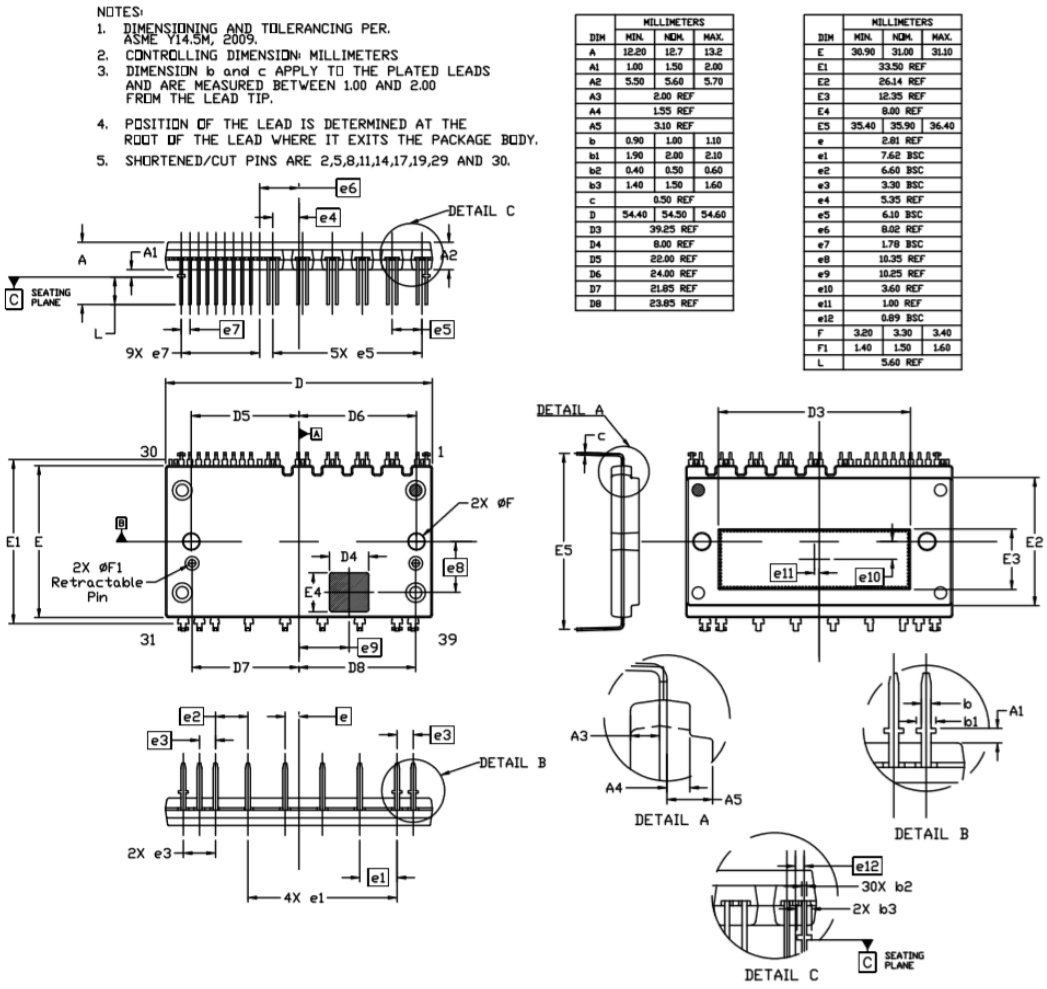


NOTES:
3. No.1 pin identification mark
4. Specific Device code
5. Lot / Serial
6. 2D code

Figure 7. Marking Specification Base on NFAMxx12L5BT

Package Outline

Unit: mm



DIM	MILLIMETERS MIN.	NOM.	MAX.
A	12.20	12.7	13.2
A1	1.00	1.50	2.00
A2	5.50	5.60	5.70
A3		2.00 REF	
A4		1.55 REF	
A5		3.10 REF	
b	0.90	1.00	1.10
b1	1.90	2.00	2.10
b2	0.40	0.50	0.60
b3	1.40	1.50	1.60
c		0.50 REF	
D	54.40	54.50	54.60
D3		39.25 REF	
D4		8.00 REF	
D5		22.00 REF	
D6		24.00 REF	
D7		21.85 REF	
D8		23.85 REF	

DIM	MILLIMETERS MIN.	NOM.	MAX.
E	30.90	31.00	31.10
E1		33.50 REF	
E2		26.14 REF	
E3		12.35 REF	
E4		8.00 REF	
E5	35.40	35.90	36.40
e		2.81 REF	
e1		7.62 BSC	
e2		6.60 BSC	
e3		3.30 BSC	
e4		5.35 REF	
e5		6.10 BSC	
e6		8.02 REF	
e7		1.78 BSC	
e8		10.35 REF	
e9		10.25 REF	
e10		3.60 REF	
e11		1.00 REF	
e12		0.89 BSC	
F	3.20	3.30	3.40
F1	1.40	1.50	1.60
L		5.60 REF	

Figure 8. NFAM2012L5BT

Unit: mm

DIM	MILLIMETERS			DIM	MILLIMETERS		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	12.20	12.7	13.2	E	30.90	31.00	31.10
A1	1.00	1.50	2.00	E1	33.50 REF		
A2	5.50	5.60	5.70	E2	26.14 REF		
A3	2.00 REF			E3	12.35 REF		
A4	1.55 REF			E4	8.00 REF		
A5	3.10 REF			E5	35.40	35.90	36.40
b	0.90	1.00	1.10	e	2.81 REF		
b1	1.90	2.00	2.10	e1	7.62 BSC		
b2	0.40	0.50	0.60	e2	6.60 BSC		
b3	1.40	1.50	1.60	e3	3.30 BSC		
c	0.50 REF			e4	5.35 REF		
D	54.40	54.50	54.60	e5	6.10 BSC		
D3	39.25 REF			e6	8.02 REF		
D4	8.00 REF			e7	1.78 BSC		
D5	22.00 REF			e8	10.35 REF		
D6	24.00 REF			e9	10.25 REF		
D7	21.85 REF			e10	3.60 REF		
D8	23.85 REF			e11	1.00 REF		
				e12	0.89 BSC		
				F	3.20	3.30	3.40
				F1	1.40	1.50	1.60
				L	5.60 REF		

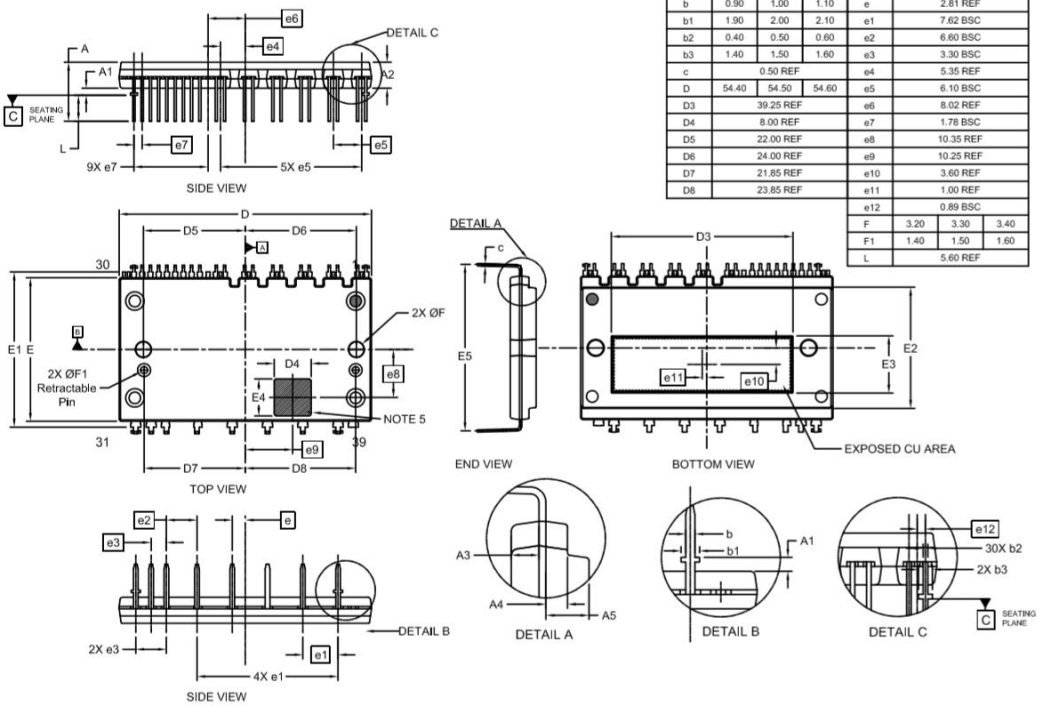


Figure 9. NFAM2012L5B

PRODUCT SYNOPSIS

This section discusses electrical specification, characteristics and mechanical characteristics.

Absolute Maximum Rating

(Tc = 25°C, unless otherwise specified)

ABSOLUTE MAXIMUM RATING (Tc = 25°C, unless otherwise specified)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART (BASE ON NFAM2012L5BT)				
VPN	Supply Voltage	Applied between P − NU, NV, NW	900	V
VPN(surge)	Supply Voltage (Surge)	Applied between P − NU, NV, NW	1000	
Vces	Collector − Emitter Voltage		1200	
±Ic	Each IGBT Collector Current	Tc = 25°C, Tj ≤ 150°C (Note 7)	20	A
±Icp	Each IGBT Collector Current (Peak)	Tc = 25°C, Tj ≤ 150°C, Under 1 ms Pulse Width	40	
Pc	Collector Dissipation	Tc = 25°C per One Chip	125	W
T_J	Operating Junction Temperature (Note 7)		−40~150	°C
CONTROL PART				
VDD	Control Supply Voltage	Applied between VDD(XX) − VSS	20	V
VBS	High−Side Control Bias Voltage	Applied between VB(X) − VS(X)	20	
VIN	Input Signal Voltage	Applied between HIN(X), LIN(X) − VSS	−0.3~VDD	
VFO	Fault Output Supply Voltage	Applied between VFO − VSS	−0.3~VDD	
IFO	Fault Output Current	Sink Current at VFO Pin	2	mA
VCIN	Current Sensing Input Voltage	Applied between CIN − VSS	−0.3~VDD	V
BOOTSTRAP DIODE PART				
VRRM	Maximum Repetitive Reverse Voltage		1200	V
CBOOT	Allowable Max. Bootstrap Capacitor	Tj ≤ 150°C	470	μF
TOTAL SYSTEM				
VPN(PROT)	Self−Protection Supply Voltage Limit (Short−Circuit Protection Capability)	VDD(XX), VB(X) = 13.5~16.5 V, Tj = 150°C, (Non−Repetitive, <2 μs)	800	V
Tc	Module Case Operation Temperature	See Figure 10	−40~125	°C
Tstg	Storage Temperature		−40~125	
Viso	Isolation Voltage	60 Hz, Sinusoidal, 1−Minute, Connect Pins to Heat Sink	2500	Vrms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

7. These values had been made on acquisition by the calculation considered to design factor. The maximum junction temperature rating of power chips integrated within the SPM 31 products are 150°C.

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rth(j−c)Q	Junction to Case Thermal Resistance (Note 8)	Inverter IGBT Part (per 1/6 Module)	−	−	1.0	°C/W
Rth(j−c)F		Inverter FWDi Part (per 1/6 Module)	−	−	1.2	

8. For the measurement point of case temperature (T_C), please refer Figure 10.

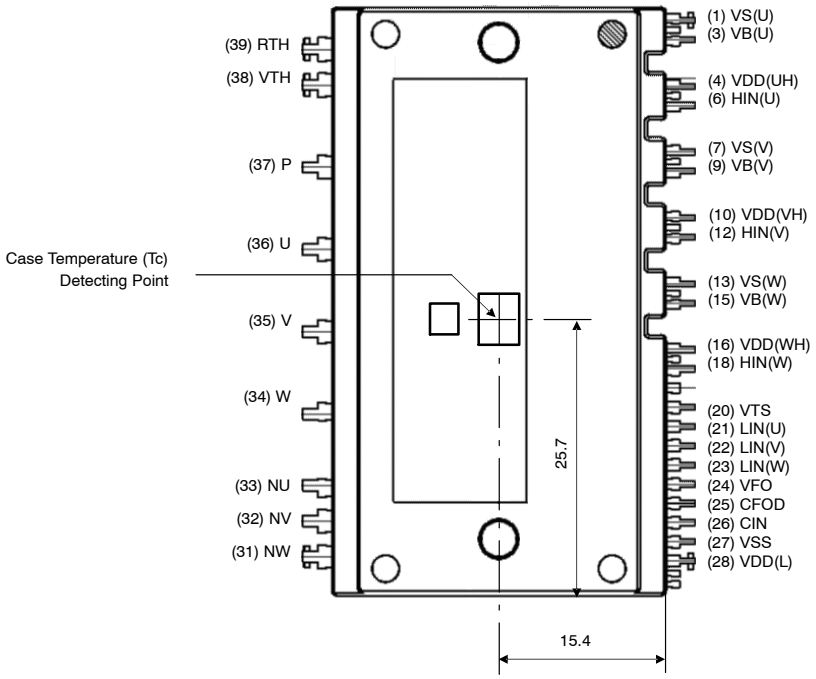


Figure 10. Case Temperature (Tc) Detecting Point

Electrical Characteristic

(Tc = 25°C, unless otherwise specified)

ELECTRICAL CHARACTERISTIC (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
INVERTER PART (BASE ON NFAM2012L5BT)							
VCE(sat)	Collector–Emitter Saturation Voltage	VDD, VBS = 15 V, yIN(X) = 5 V	Ic = 20 A, Tj = 25°C	–	1.85	2.5	V
VF	FWDi Forward Voltage	yIN(X) = 0 V	If = 20 A, Tj = 25°C	–	1.9	2.5	
ton	Switching Times (High Side) (Note 9)	VPN = 600 V, VDD = 15 V, VBS = 15 V, Ic = 20 A, Tj = 25°C, IN = 0 V ↔ 5 V, Inductive Load See Figure 11		0.80	1.40	2.00	μs
tc(on)				–	0.30	0.60	
toff				–	1.90	2.70	
tc(off)				–	0.20	0.60	
trr				–	0.40	–	
ton	Switching Times (Low Side) (Note 9)			0.90	1.50	2.10	
tc(on)				–	0.30	0.60	
toff				–	2.00	2.80	
tc(off)				–	0.20	0.60	
trr				–	0.40	–	
Ices	Collector – Emitter Leakage Current	Vce = Vces, Tj = 25°C		–	–	1	mA
BOOTSTRAP CIRCUIT PART							
VF	Forward Voltage	If = 0.1 A, Tj = 25°C		3.4	4.6	5.8	V
RBOOT	Bootstrap Resistor	If = 0.1 A, Tj = 25°C		30	38	46	Ω

ELECTRICAL CHARACTERISTIC (T_C = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
CONTROL PART							
IQDDH	Quiescent VDD Supply Current	VDD(xH) = 15 V, HIN(X), LIN(X) = 0 V	VDD(xH) – VSS	–	–	0.30	mA
IQDDL	Quiescent VDD Supply Current	VDD(L) = 15 V, HIN(X), LIN(X) = 0 V	VDD(L) – VSS	–	–	3.50	
IQBS	Quiescent VBS Supply Current of Each Phase	VB(X) – VS(X) = 15 V, HIN (X) = 0 V		–	–	0.30	
VFOH	Fault Output Voltage	CIN = 0 V, Pulled up to 5 V by 10 kΩ		4.9	–	–	V
VFOL		CIN = 1 V, Pulled up to 5 V by 10 kΩ		–	–	0.95	
VCIN(ref)	Short–Circuit Trip Level	VDD = 15 V	CIN – VSS	0.46	0.48	0.50	
UVDDD	Supply Circuit, Under–Voltage Protection	Detection Level		10.3	–	12.5	
UVDDR		Reset Level		10.8	–	13.0	
UVBSD		Detection Level		10.0	–	12.0	
UVBSR		Reset Level		10.5	–	12.5	
tFOD	Fault–Out Pulse Width	CFOD = 22 nF		1.6	2.4	–	ms
VTS	Temperature output	VDD(L) = 15 V, VTS – VSS = 10 nF, TLVIC = 25°C		0.905	1.030	1.155	V
$VIN(ON)_{)}$	ON Threshold Voltage	Applied between HIN(X), LIN(X) – VSS		–	–	2.6	
VIN(OFF)	OFF Threshold Voltage			0.8	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

9. ton and toff include the propagation delay time of the internal drive IC. tc(on) and tc(off) are the switching time of IGBT itself under the given gate driving condition internally. For the detail information, please see and Figure 11.
10. Short–circuit current protection is functioning only at low side.

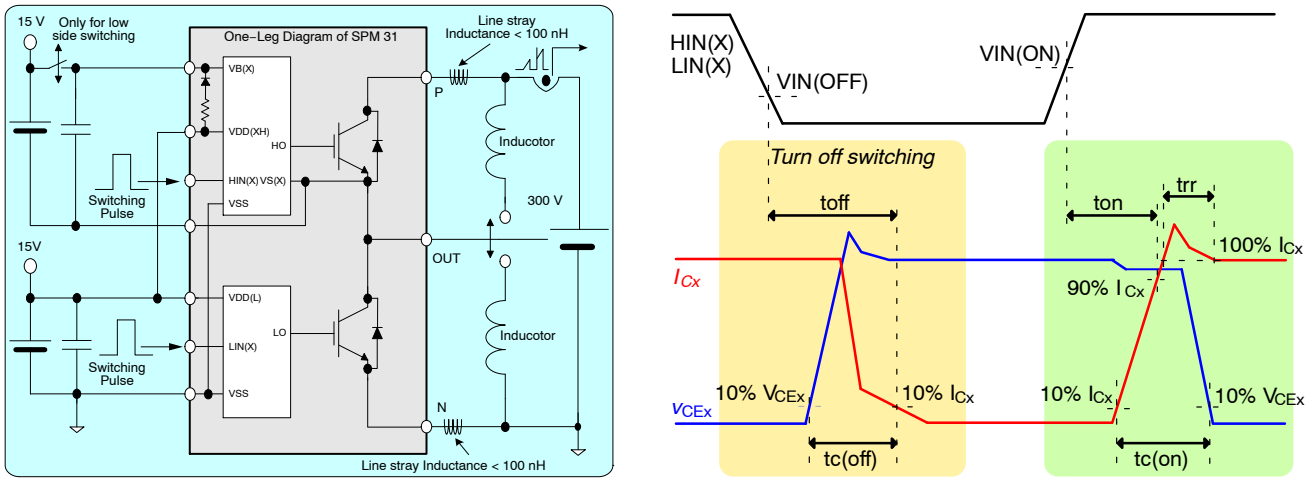


Figure 11. Switching Evaluation Circuit and Switching Time Definition

Recommended Operating Conditions

(Base on NFAM2012L5B(T))

RECOMMENDED OPERATING CONDITIONS (Base on NFAM2012L5B(T))

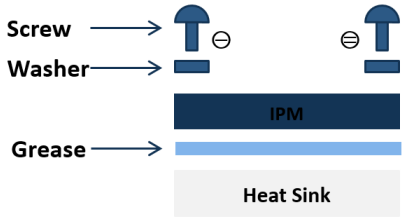
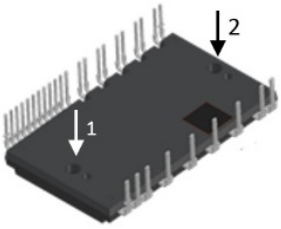
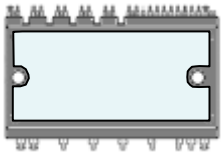
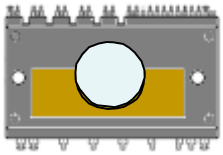
Symbol	Parameter	Condition		Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P – N_x		–	600	800	V
VDD	Gate Driver Supply Voltages	Applied between VDD(XH) – VSS		13.5	15.0	16.5	
VBS		Applied between VB(X) – VS(X)		13.0	15.0	18.5	
dVDD/dt, dVBS/dt	Control Supply Variation			–1	–	1	V/μs
DT	Dead Time	Turn–off to Turn–on (external)		3	–	–	μs
fPWM	PWM Input Signal	–		1	–	20	kHz
Io	Allowable r.m.s Current	400 V ≤ VPN ≤ 800 V, 13.5 V ≤ VDD ≤ 16.5 V, 13.0 V ≤ VBS ≤ 18.5 V –40°C ≤ Tc ≤ 150°C	f_{PWM} = 5 kHz	–	–	18.1	Arms
			f_{PWM} = 15 kHz	–	–	9.4	
PWIN (on)	Allowable Input Pulse Width	VPN ≤ 800 V, 13.5 V ≤ VDD ≤ 16.5 V 13.0 V ≤ VBS ≤ 18.5 V, –40°C ≤ Tc ≤ 125°C		2.0	–	–	μs
PWIN (off)				2.5	–	–	
	Package Mounting Torque	M3 type screw		0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. This product might not make response if input pulse with is lee than the recommended value.

Mechanical Characteristics

MECHANICAL CHARACTERISTICS

Item	Recommended Condition
Pitch	46.0 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions D = 7 mm, d = 3.2 mm and t = 0.5 mm JIS B 1256  * JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): -50 to 100 μm No contamination on the heat sink surface that contacts IPM.
Torque	Pre. tightening: 0.2~0.3 Nm on first screw Pre. tightening: 0.2~0.3 Nm on second screw Final tightening: 0.6~0.9 Nm on first screw Final tightening: 0.6~0.9 Nm on second screw   Pre - Screwing : 1 → 2 Final Screwing : 1 → 2
Grease	Silicone grease. Thickness: 100 to 200 μm Uniformly apply silicon grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.  Recommend  Not Recommend

OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 1200 V SPM 31 uses external shunt resistor for the short circuit current detection, as shown in Figure 12. LVIC has a built−in short−circuit current protection function. This protection function senses the voltage to the CIN pin. If this voltage (VCIN) exceeds the VCIN(ref) (the threshold voltage trip level of over current protection) specified in the device datasheets (VCIN(ref), typ. is 0.48 V), a fault signal is asserted and the all low side IGBTs are turned off.

Typically, the maximum short−circuit current magnitude is gate−voltage dependent: higher gate voltage (VDD and VBS) results in larger short−circuit current. To avoid potential problems, the maximum short−circuit trip level is set below 1.5 times the nominal rated collector current. The LVIC over current protection−timing chart is shown in Figure 12.

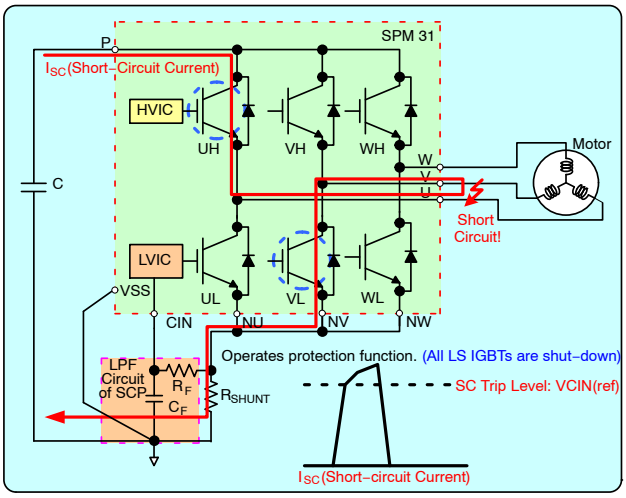
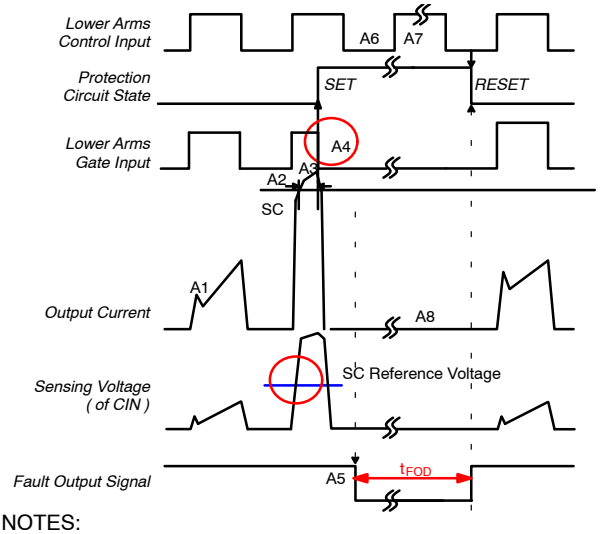


Figure 12. Operation of Short−Circuit Protection



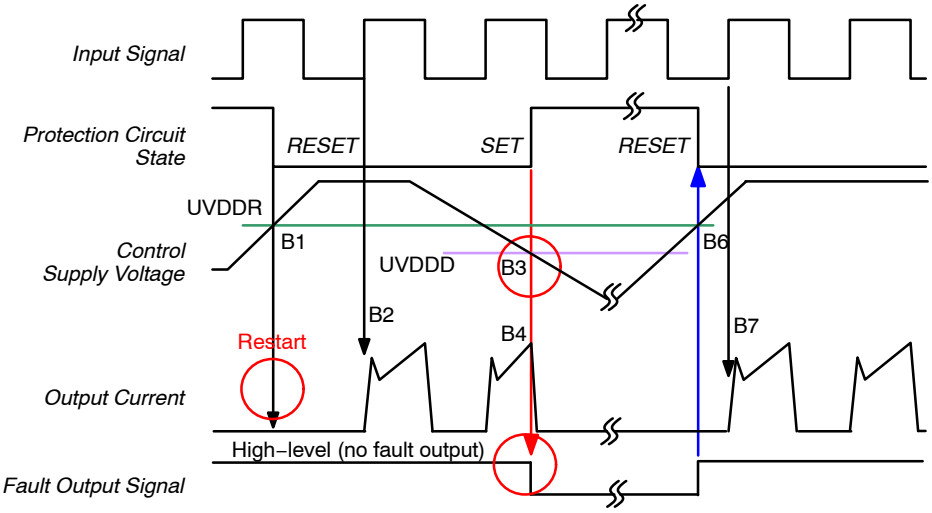
NOTES:

12. A1: normal operation: IGBT turn on and carrying current.
13. A2: short−circuit current detection (SC trigger).
14. A3: hard IGBT gate interrupt.
15. A4: IGBT turns off.
16. A5: fault output timer operation starts with internal delay (typ. 2.4 ms, CFOD = 22 nF), Fault−out duration time is controlled by CIN.
17. A6: input “L”: IGBT turn off state.
18. A7: input “H”: IGBT turn on state, but during the active period of fault output the IGBT doesn’t turn on.
19. A8: IGBT keeps turn off state

Figure 13. Timing Chart of Short−Circuit Protection Function

Under−Voltage Lock Out Protection

The LVIC has an Under−Voltage Lock Out protection (UVLO) function to protect the low−side IGBTs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 14.

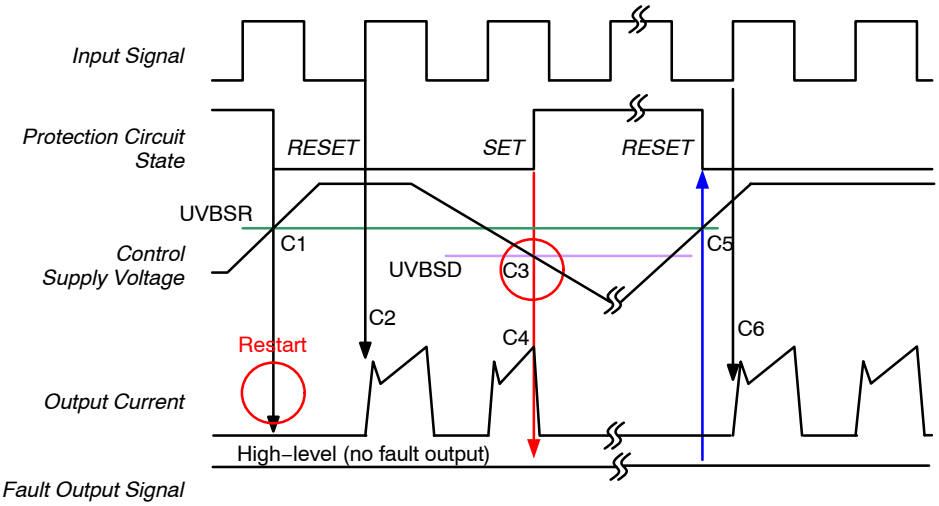


NOTES: *(Low−Side Protection Sequence)*

20. B1: control supply voltage rise: after the voltage rises UVDDD, the circuits start to operate when the next input is applied.
21. B2: normal operation: IGBT turn on and carrying current.
22. B3: under−voltage detection UVDDD.
23. B4: IGBT turn off in spite of control input is alive.
24. B5: fault output signal starts.
25. B6: under−voltage reset UVDDR.
26. B7: normal operation: IGBT turn on and carrying current. If fault−out duration (tFOD) by external capacitor at CIN pin is longer than UVDDD timing, fault output and IGBT state are cleared after tFOD.

Figure 14. Timing Chart of Low−side Under−Voltage Protection Function

The HVIC has an under−voltage lockout function to protect the high−side IGBT from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 15. A fault−out (VFO) alarm is not given for low HVIC bias conditions.



NOTES: (High−Side Protection Sequence)

27. C1: control supply voltage rises: after the voltage reaches UVBSR, the circuit starts when the next input is applied.
28. C2: normal operation: IGBT turn on and carrying current.
29. C3: under−voltage detection (UVBSD).
30. C4: IGBT turn off in spite of control input is alive, but there is no fault output signal.
31. C5: under−voltage reset (UVBSR).
32. C6: normal operation: IGBT turn on and carrying current

Figure 15. Timing Chart of High-Side Under-Voltage Protection Function

KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 1200 V SPM 31 series.

Thermal Sensor Output (VTS) and NTC Thermistor

The junction temperature of power devices should not exceed the maximum junction temperature. Even though there is some margin between the Tj_{MAX} specified on the datasheet and the actual Tj_{MAX} at which power devices get destroyed, caution should be given to make sure the junction temperature stays well below the Tj_{MAX}. One of the inconveniences in using previous versions of SPM 31 series products was lack of temperature monitoring. An NTC had to be mounted on the heat sink or very close to the module if over−temperature protection is required in the application.

Circuit of VTS

The Thermal Sensing Unit analog voltage output reflects the temperature of the LVIC in 1200 V SPM 31 version 6 series products. The relationship between VTS voltage output and LVIC temperature is shown in Figure 17. It does not have any self−protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from IGBT temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot−through event. Even though VTS has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 16 shows the LVIC location of SPM 31 series and Figure 17 shows that the relationship between VTS voltage and LVIC temperature. It can be expressed as the following equation.

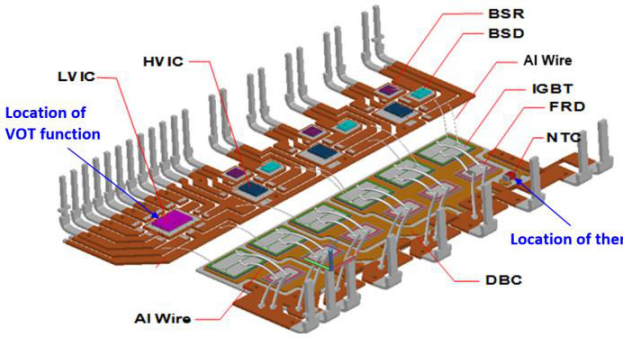


Figure 16. Location of VTS Function (LVIC) and NTC

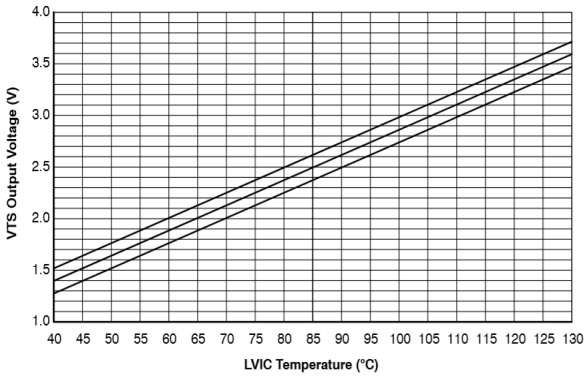


Figure 17. Temperature vs. VTS

Figure 18 shows the equivalent circuit diagram of VTS inside IC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V, an external Zener diode should be inserted between an A/D input pin and the analog ground pin of MCU. An amplifier can be used to change the range of voltage input to the Analog to Digital converter to have better resolution of the temperature. It is recommended to add a ceramic capacitor of 10 nF or more between VTS and VSS (Signal Ground) to make the VTS more stable.

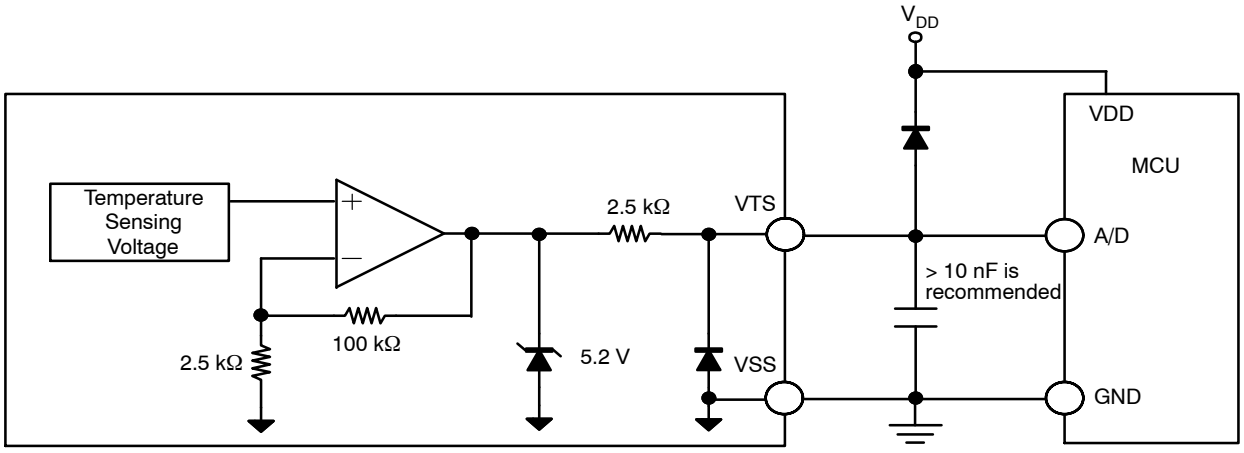


Figure 18. Internal Block Diagram and Interface Circuit of VTS

$VTS_{,min} = 0.0243 \times T_{LVIC} + 0.3015$ [V]
$VTS_{,typ} = 0.0243 \times T_{LVIC} + 0.4225$ [V]
$VTS_{,max} = 0.0243 \times T_{LVIC} + 0.5435$ [V]

The maximum variation of VTS is 0.121 V, and the minimum variation of VTS is 0.121 V due to process variation which is equivalent ±5°C approximately. This is regardless of the temperature because the slopes of three lines are identical. If the ambient temperature information is available. For example, through NTC in the system, VTS can be measured to adjust the offset before the motor starts to operate. As temperature decreases further below 0°C, VTS decreases linearly until it reaches zero volts. If the temperature of LVIC increases above 150°C, which is above the maximum operating temperature, VTS would increase theoretically up to 5.2 V until it gets clamped by the internal zener diode.

Circuit of NTC Thermistor (Monitoring of Tc)

The Motion SPM 31 series includes a Negative Temperature Coefficient (NTC) thermistor for module case temperature (Tc) sensing. This thermistor is located in DBC substrate with the power chip (IGBT//FWDi).

Therefore, the thermistor can accurately reflect the temperature of the power chip (see Figure 19).

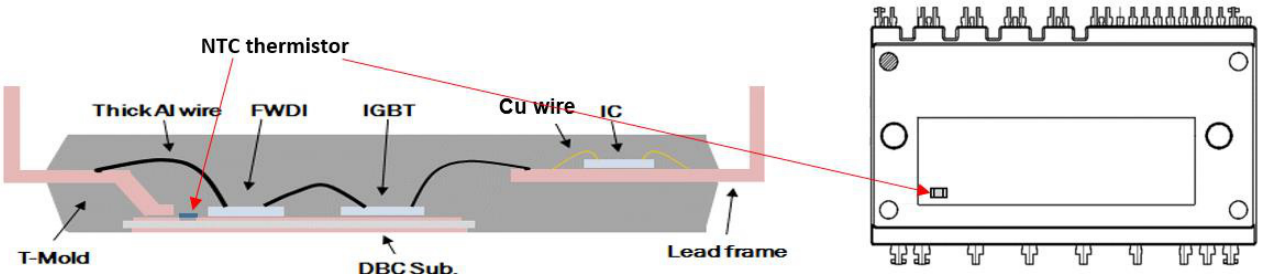


Figure 19. Location of NTC Thermistor in SPM 31 Package

Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog−Digital Converter (ADC). The other is circuit by comparator. Figure 20 shows examples of application circuits with an NTC thermistor.

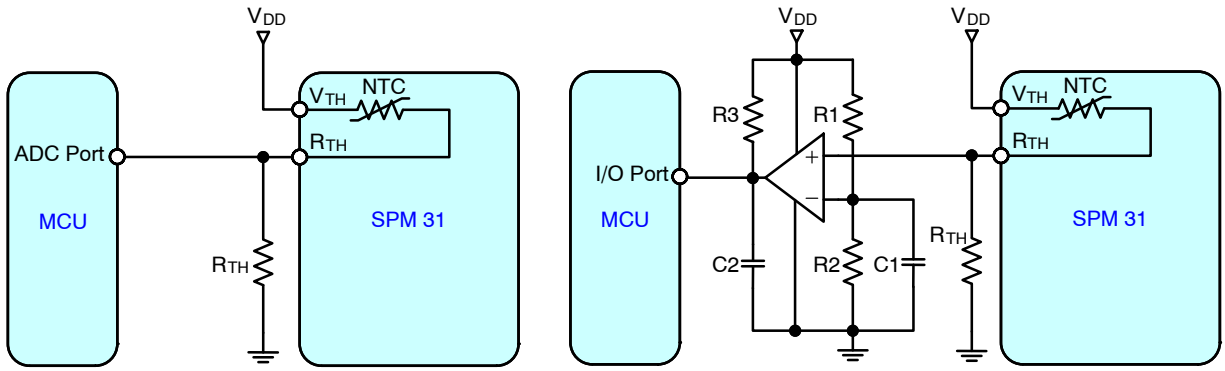


Figure 20. Over Temperature Protection Circuit by MCU and Comparator

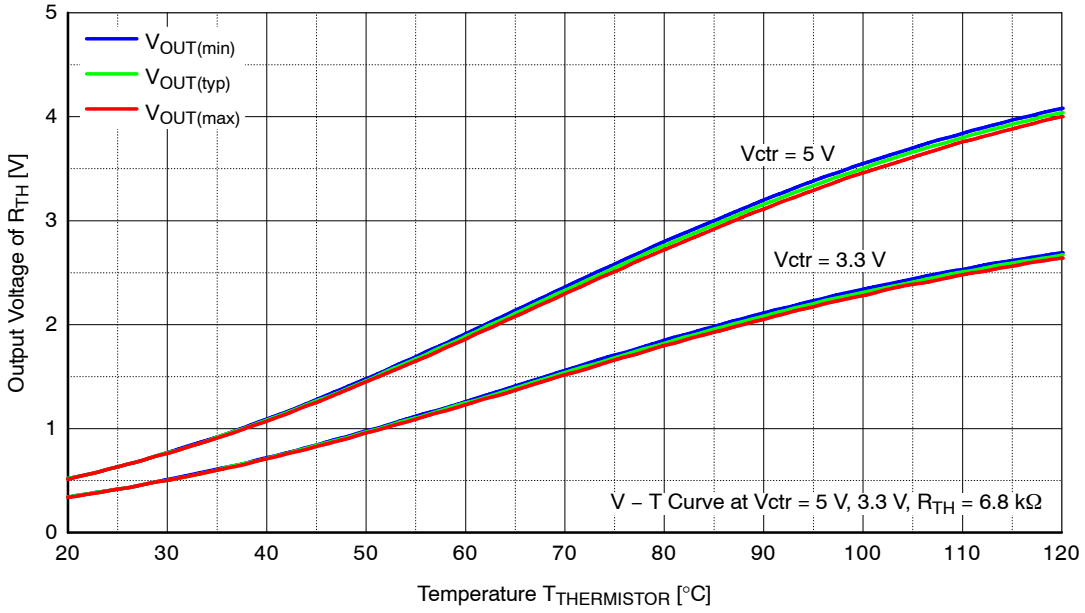


Figure 21. V – T Curve of Figure 20

Table 3. THERMISTOR CHARACTERISTICS (BUILT−IN ONLY IN T TYPE)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{25}	Resistance	Tc = 25°C	46.530	47	47.47	kΩ
R_{125}	Resistance	Tc = 125°C	1.344	1.406	1.471	kΩ
–	B−Constant (25 – 50°C)	B	4009.5	4050	4090.5	K
–	Temperature range	–	−40	–	+125	°C

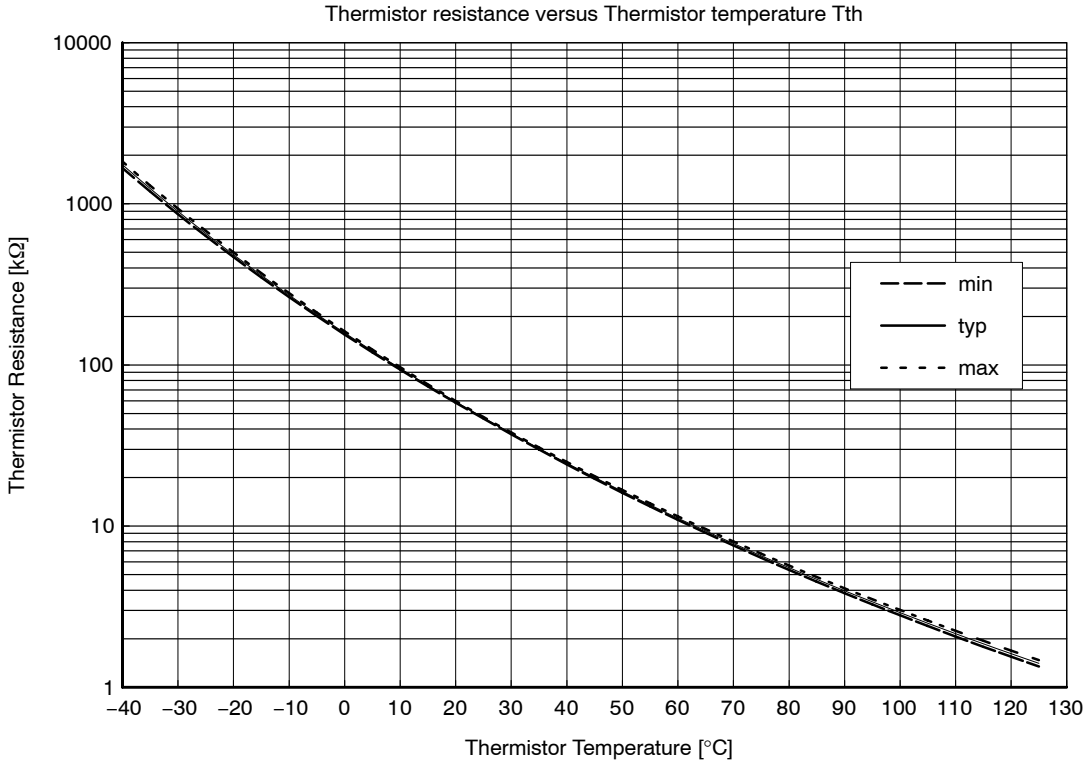


Figure 22. Thermistor Resistance vs. Temperature

Table 4. R−T TABLE OF NTC THERMISTOR

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
0	154.7426	158.2144	161.748	42	22.257	22.6466	23.0406	84	4.674	4.8299	4.9904
1	146.9466	150.1651	153.4388	43	21.3574	21.7401	22.1275	85	4.5213	4.6736	4.8305
2	139.5891	142.5725	145.6051	44	20.4988	20.8746	21.2551	86	4.3737	4.5226	4.676
3	132.643	135.4081	138.217	45	19.679	20.0478	20.4216	87	4.2317	4.3771	4.5271
4	126.0829	128.6453	131.2466	46	18.8961	19.258	19.6249	88	4.0948	4.2369	4.3835
5	119.8852	122.2594	124.6681	47	18.1482	18.5032	18.8633	89	3.963	4.1019	4.2452
6	114.028	116.2273	118.4573	48	17.4337	17.7818	18.135	90	3.8361	3.9717	4.1118
7	108.4905	110.5275	112.5914	49	16.7508	17.0921	17.4385	91	3.7137	3.8463	3.9832
8	103.2537	105.1398	107.0496	50	16.0981	16.4325	16.7721	92	3.5958	3.7253	3.8592
9	98.2995	100.0454	101.8121	51	15.474	15.8016	16.1346	93	3.4821	3.6087	3.7396
10	93.6111	95.2267	96.8605	52	14.8772	15.1981	15.5243	94	3.3725	3.4963	3.6242
11	89.1728	90.6673	92.1776	53	14.3063	14.6205	14.9402	95	3.2668	3.3878	3.5128
12	84.9699	86.3519	87.7475	54	13.7601	14.0677	14.3808	96	3.1654	3.2836	3.4058
13	80.9887	82.2661	83.5552	55	13.2374	13.5385	13.8452	97	3.0675	3.183	3.3026
14	77.2163	78.3963	79.5865	56	12.737	13.0318	13.332	98	2.973	3.086	3.2029
15	73.6406	74.7302	75.8283	57	12.258	12.5465	12.8404	99	2.8819	2.9923	3.1066
16	70.2503	71.2558	72.2684	58	11.7993	12.0815	12.3693	100	2.794	2.9019	3.0137
17	67.0347	67.962	68.8953	59	11.36	11.6361	11.9176	101	2.7091	2.8146	2.9239
18	63.9841	64.8386	65.6981	60	10.9391	11.2091	11.4847	102	2.6272	2.7303	2.8372
19	61.0889	61.8759	62.6667	61	10.5366	10.8007	11.0703	103	2.5481	2.6489	2.7535
20	58.3406	59.0647	59.7918	62	10.1508	10.4091	10.6729	104	2.4717	2.5703	2.6725
21	55.7305	56.3961	57.064	63	9.781	10.0336	10.2916	105	2.3979	2.4943	2.5943
22	53.2515	53.8628	54.4756	64	9.4265	9.6734	9.9258	106	2.3264	2.4206	2.5184
23	50.8962	51.4569	52.0186	65	9.0865	9.3279	9.5747	107	2.2572	2.3493	2.445
24	48.6579	49.1715	49.6857	66	8.7603	8.9963	9.2378	108	2.1904	2.2805	2.3741
25	46.53	47	47.47	67	8.4475	8.6782	8.9143	109	2.1258	2.2139	2.3054
26	44.4667	44.936	45.4058	68	8.1472	8.3727	8.6036	110	2.0634	2.1496	2.2391
27	42.5059	42.9737	43.4423	69	7.8591	8.0795	8.3053	111	2.0034	2.0877	2.1753
28	40.642	41.1075	41.5742	70	7.5825	7.7979	8.0186	112	1.9454	2.0278	2.1135
29	38.8697	39.3323	39.7964	71	7.3163	7.5268	7.7426	113	1.8893	1.9699	2.0538
30	37.184	37.6431	38.104	72	7.0606	7.2663	7.4773	114	1.8351	1.9139	1.996
31	35.5801	36.0351	36.4923	73	6.815	7.016	7.2223	115	1.7827	1.8598	1.94
32	34.0537	34.5041	34.9571	74	6.5791	6.7755	6.9771	116	1.7322	1.8076	1.8862
33	32.6007	33.0462	33.4944	75	6.3524	6.5443	6.7414	117	1.6834	1.7572	1.834
34	31.2171	31.6573	32.1005	76	6.1352	6.3227	6.5153	118	1.6361	1.7083	1.7836
35	29.8994	30.3339	30.7717	77	5.9263	6.1096	6.2979	119	1.5904	1.6611	1.7347
36	28.6447	29.0734	29.5055	78	5.7256	5.9046	6.0887	120	1.5461	1.6153	1.6874
37	27.4492	27.8717	28.2979	79	5.5325	5.7075	5.8874	121	1.5031	1.5707	1.6413
38	26.3098	26.726	27.146	80	5.3468	5.5178	5.6936	122	1.4613	1.5276	1.5966
39	25.2235	25.6332	26.047	81	5.1688	5.3358	5.5077	123	1.421	1.4858	1.5534
40	24.1876	24.5907	24.9981	82	4.9975	5.1607	5.3287	124	1.3819	1.4453	1.5114
41	23.1996	23.596	23.9967	83	4.8326	4.9921	5.1564	125	1.344	1.406	1.4708

Selection of Shunt Resistor

Figure 23 shows an example circuit of the SC protection using 1−shunt resistor. The line current on the N side DC−ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the SC reference level, all the gates of the N−side three−phase IGBTs are switched to the off state and the VFO fault signal is transmitted to MCU. Since SC protection is non−repetitive, IGBT operation should be immediately halted when the VFO fault signal is given.

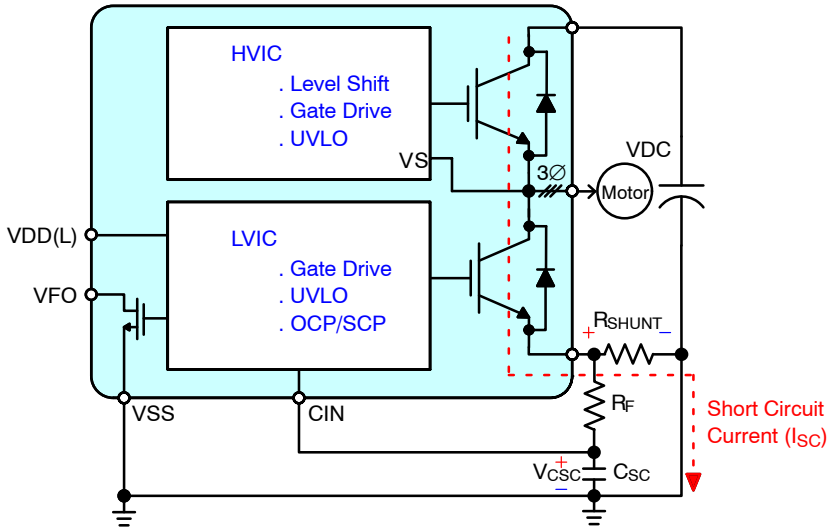


Figure 23. Short Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistor is calculated by the following equation.
Recommended SC current trip level: $I_{SC(max)}$ = 1.5 x Ic (rated current)
SC trip referenced voltage: VCIN(ref) = min. 0.46 V, typ. 0.48 V, max. 0.5 V
Shunt resistance: $I_{SC(max)}$ = $VCIN(ref)_{\_max}$ / $R_{SHUNT(min)}$ → $R_{SHUNT(min)}$ = $V_{SC(max)}$ / $I_{SC(max)}$
If the deviation of shunt resistor should is limited below ±5%,
$R_{SHUNT(typ)}$ = $R_{SHUNT(min)}$ / 0.95, $R_{SHUNT(max)}$ = $R_{SHUNT(typ)}$ x 1.05
Actual SC trip current level becomes:
$I_{SC(typ)}$ = $VCIN(ref)_{\_typ}$ / $R_{SHUNT(min)}$, $I_{SC(min)}$ = $V_{SC(min)}$ / $R_{SHUNT(max)}$
Inverter output power:
P_{OUT} = √3 x VO,LL x $I_{O(RMS)}$ x PF
Where:
VO,LL = (√3 / √2) x MI x (V_{DC} / 2)
I(O)RMS = Maximum load current of inverter; and
MI = Modulation Index;
VDC = DC link voltage;
PF = Power Factor
Average DC Current
I_{DC_AVG} = V_{DC_Link} / (P_{out} x Eff)
Where:
Eff = Inverter Efficiency
The power rating of shunt resistor is calculated by the following equation.
P_{SHUNT} = (I^2_{RMS} x R_{SHUNT} x Margin) / De−rating Ratio
Where:
Shunt resistor typical value at Tc = 25°C (R_{SHUNT})
De−rating ratio of shunt resistor at T_{SHUNT} = 100°C (From datasheet of shunt resistor)
Safety margin (Determine by customer)

The value of shunt resistor calculation examples:
DUT: NFAM2012L5B(T)
Tolerance of shunt resistor: ±5%
SC Trip Reference Voltage, VCIN(ref):
$VCIN(ref)_{\_min}$ = 0.46 V, $VCIN(ref)_{\_typ}$ = 0.48 V, $VCIN(ref)_{\_max}$ = 0.5 V
Maximum Load Current of Inverter (I_{RMS}): 14 A_{rms}
Maximum Peak Load Current of Inverter ($I_{C(max)}$): 30 A
Modulation Index (MI): 0.9
DC Link Voltage (V_{DC_Link}): 600 V
Power Factor (PF): 0.8
Inverter Efficiency (Eff): 0.95
Shunt Resistor Value at Tc = 25°C (R_{SHUNT}): 16 mΩ
De−rating Ration of Shunt Resistor at T_{SHUNT} = 100°C: 70% (refer to Figure 24)
Safety Margin: 20 %

Calculation results:
$I_{SC(max)}$: 1.5 x $I_{C(max)}$ = 1.5 x 20 A = 30 A
$R_{SHUNT(typ)}$: $VCIN(ref)_{\_typ}$ / $I_{SC(max)}$ = 0.48 V / 30 A = 16.0 mΩ
$R_{SHUNT(max)}$: $R_{SHUNT(max)}$ x 1.05 = 16.0 mΩ x 1.05A = 16.8 mΩ
$R_{SHUNT(min)}$: $R_{SHUNT(min)}$ x 0.95 = 16.0 mΩ x 0.95 A = 15.2 mΩ
$I_{SC(min)}$: $VCIN(ref)_{\_min}$ / $R_{SHUNT(max)}$ = 0.46 V / 16.8 mΩ = 27.38 A
$I_{SC(max)}$: $VCIN(ref)_{\_max}$ / $R_{SHUNT(min)}$ = 0.5 V / 15.2 mΩ = 32.89 A
P_{OUT} = √3 x ((√3 / √2) x MI x (V_{DC} / 2)) x $I_{(O)RMS}$ x PF = (3 / √2) x 0.9 x (600 / 2) x 14 x 0.8 = 6415 W
I_{DC_AVG} = (P_{OUT} / Eff) / V_{DC_Link} = 11.25 A
P_{SHUNT} = ($I^2_{DC\_AVG}$ x R_{SHUNT} x Margin) / De−rating Ratio = (11.25^2 x 0.016 x 1.2) / 0.7 = 3.47 W (therefore, the proper power rating of shunt resistor is over 3.5 W).

When over−current events are detected, the 1200 V Motion SPM 31 series shuts down all low−side IGBTs and sends out the fault−out (VFO) signal. FAULT output timer operation start with internal delay (typ. 2.4 ms, CFOD = 22 nF), Fault−out duration time is controlled by CFOD.

To prevent malfunction, it is recommended that an RC filter be inserted at the CIN pin. To shut down IGBTs within 3 μs when over−current situation occurs, a time constant of 0.75~1.25 μs is recommended.

Table 5 shows the shunt resistance and typical short−circuit protection current

Table 5. OVER−CURRENT (OC) PROTECTION TRIP LEVEL

Device	R_{SHUNT}	OC Trip Level	Remark
NFAM0512L5B(T)	64.0 mΩ	7.5 A	It is typical value
NFAM1012L5B(T)	32.0 mΩ	15 A	
NFAM2012L5B(T)	16.0 mΩ	30 A	

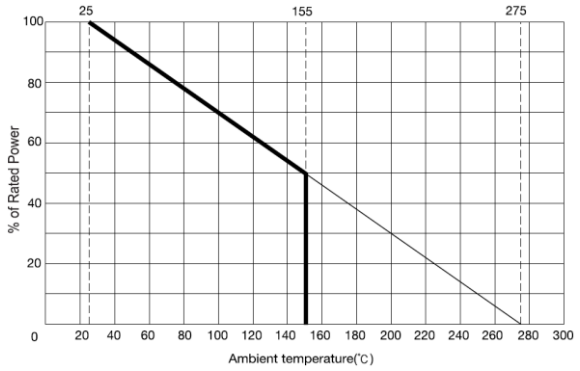


Figure 24. De−rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter is prevents noise−related over and short circuit current protection (OCP, SCP) circuit malfunction. The RC time constant is determined by the applied noise time and the Short−Circuit withstanding time (SCWT) of SPM 31 version series. When the R_{shunt} voltage exceeds the VCIN(ref) level, this is applied to the CIN pin via the RC filter. The RC filter delay is the time required for the CIN pin voltage to rise to the referenced SCP level. The LVIC has an internal filter time (logic filter time for noise elimination: around 0.85 μs). Consider this filter time when designing the RC filter of VCIN. Figure 25 shows actual real time at over and short circuit current protection. Each time sections have a distribution, so it is necessary to consider a distribution.

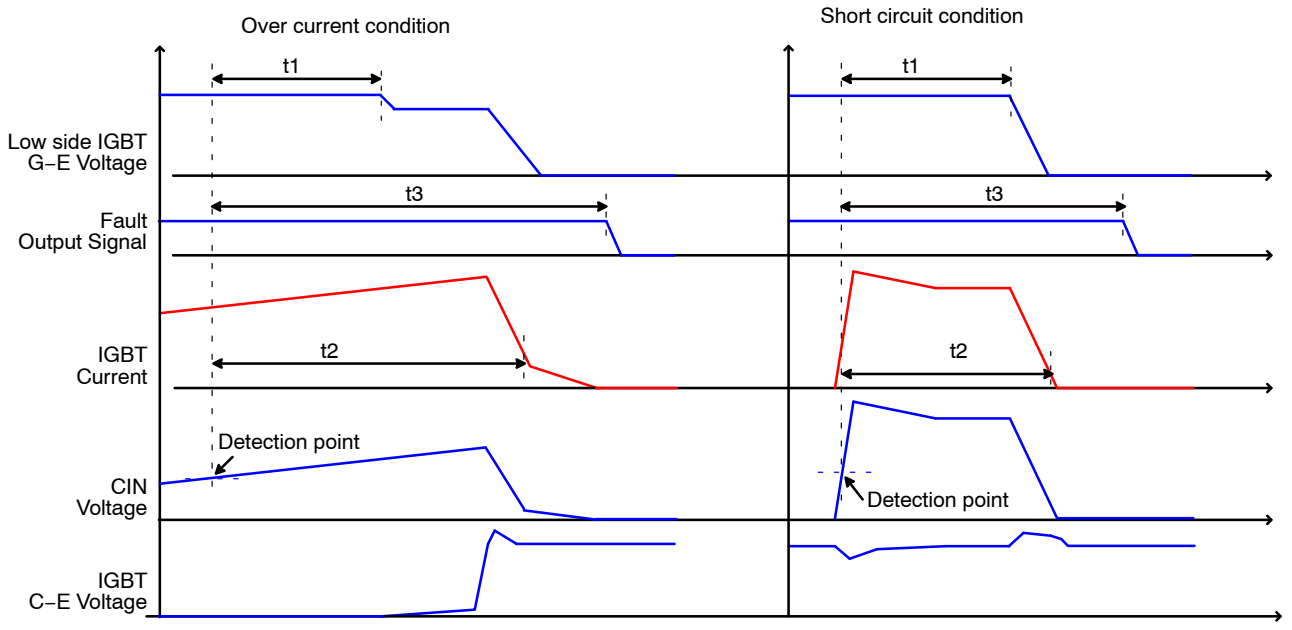


Figure 25. Timing Diagram of Over and Short Circuit Protection

Table 6. TIME TABLE OF OVER AND SHORT CIRCUIT CONDITIONS; VCIN(REF) TO LOW SIDE GATE, COLLECTOR CURRENT AND VFO

Ref. Condition VPN = 600 V, VDD = 15 V		Over Current Condition. 2 * I Rating						Short Circuit Condition					
		t1 [μs]		t2 [μs]		t3 [μs]		t1 [μs]		t2 [μs]		t3 [μs]	
Device	**T_J [°C]**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**	**Typ**	**Max**
NFAM0512L5B(T)	*25*	1.05	1.30	1.9	2.2	4.0	5.0	1.05	1.30	1.4	1.7	4.0	5.0
	150	1.0	1.25	1.8	2.1	3.2	4.2	1.0	1.25	1.2	1.5	3.2	4.2
NFAM1012L5B(T)	*25*	1.05	1.30	1.7	2.0	4.0	5.0	1.05	1.30	1.1	1.3	4.0	5.0
	150	1.0	1.25	1.65	1.9	3.2	4.2	1.0	1.25	0.9	1.2	3.2	4.2
NFAM2012L5B(T)	*25*	1.05	1.30	1.8	2.1	4.0	5.0	1.05	1.30	1.3	1.6	4.0	5.0
	150	1.0	1.25	1.75	2.05	3.2	4.2	1.0	1.25	1.1	1.4	3.2	4.2

33. To guarantee safe short−circuit protection under all operating conditions, CIN should be triggered within 1.0 μs after short−circuit occurs. (Recommendation: SCWT < 3.0 μs, Conditions: VDC = 800 V, VDD = 16.5 V, Tj = 150°C).

It is recommended that delay from short−circuit to CIN triggering should be minimized.

NOTES:

1. t1: from CIN detection to gate driver LO shut down
2. t2: from CIN detection to collector current 10 %
3. t3: from CIN detection to fault out signal activation

Fault Output Circuit

Because VFO terminal is an open−drain type, it should be pulled up via a pull−up resistor.

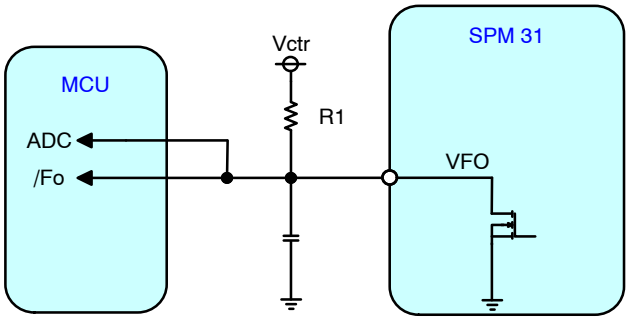


Figure 26. Voltage−Current Characteristics of VFO Terminal

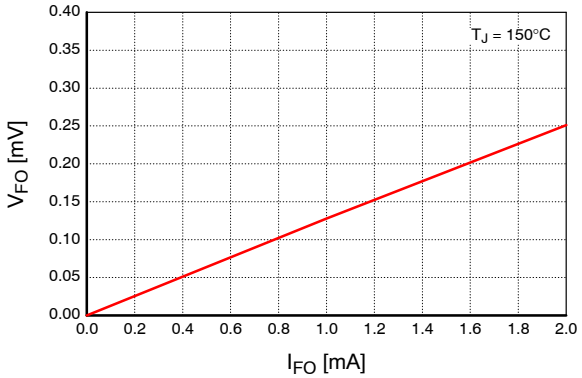


Figure 27. Voltage−Current Characteristics of VFO Terminal

Circuit of Input Signal (HINx, LINx)

Figure 28 shows recommended I/O interface circuit between the MCU and SPM 31. Because SPM 31 input logic is active HIGH and there are built−in pull−down resistors, external pull−down resistors are not needed.

Since the fault output is open drain and its rating is VDD + 0.3 V, 15 V supply interface is possible.

However, it is recommended that the fault output be configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the decoupling capacitors be placed at both the MCU and Motion SPM 31 ends of the VFO signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 28) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the Motion SPM 31 series integrates a 5 kΩ (typical) pull−down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 31 input, attention should be given to the signal voltage drop at the Motion SPM 31 input terminals to satisfy the turn−on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in Figure 28.

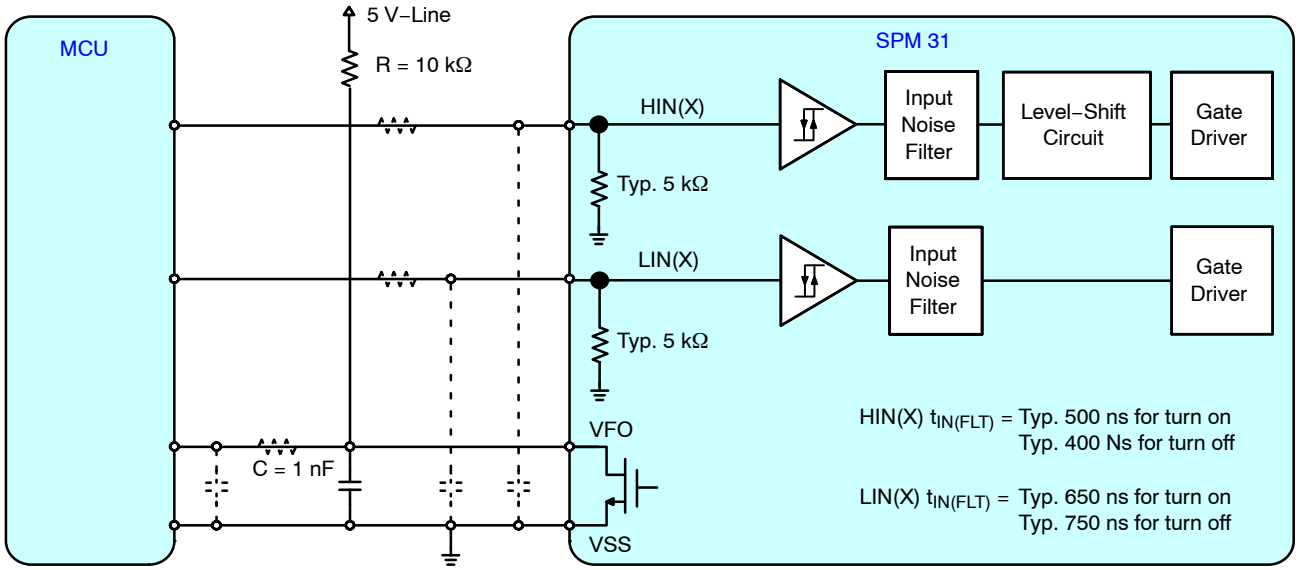


Figure 28. Recommended MCU I/O Interface Circuit

Bootstrap Circuit Design

Operation of Bootstrap Circuit

The VBS voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), provides the supply to the HVIC within the 1200 V SPM 31 series. This supply must be in the range of 13.0 V~18.5 V to ensure that the HVIC can fully drive the high−side IGBT. The SPM 31 series includes an under−voltage lock out protection function for the VBS to ensure that the HVIC does not drive the high−side IGBT, if the VBS voltage drops below a specified voltage. This function prevents the IGBT from operating in a high dissipation mode. There are a number of ways in which the VBS floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 29). This method has the advantage of being simples and inexpensive. However, the duty cycle and on−time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low−side or the load), the bootstrap capacitor (C_{BOOT}) is charged through the bootstrap diode (D_{BOOT}) and the resistor (R_{BOOT}) from the VDD supply

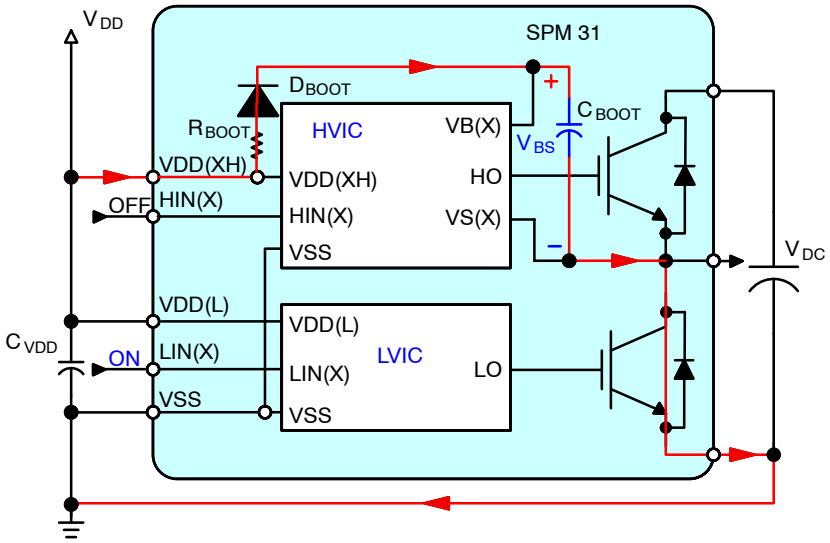


Figure 29. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on−time of the low−side IGBT to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BOOT} \times R_{Boot} \times \frac{1}{\delta} \times \ln \frac{VDD}{VDD - VBS(min.) - VF - VLS} \quad \text{(eq. 1)}$$

Where:

VF = Forward voltage drop across the bootstrap diode;

VBS(min.) = The minimum value of the bootstrap capacitor;

VLS = Voltage drop across the low−side IGBT or load; and

Δ = Duty ratio of PWM.

When the bootstrap capacitor is charged initially; VDD drop voltage is generated based on initial charging method, VDD line SMPS output current, VDD source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UVDDD level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce VDD voltage drop at initial charging, a large VDD source capacitor and selection of optimized low−side turn−on method are recommended. Adequate on−time duration of the low−side IGBT to fully charge the bootstrap capacitor is initially required before normal operation of PWM starts.

Figure 30 shows an example of initial bootstrap charging sequence. Once VDD establishes, VBS needs to be charged by turning on the low−side IGBTs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high−side PWM signals. The capacitance of VDD should be sufficient to supply necessary charge to VBS capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high−side IGBTs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over−current protection level.

Therefore, initial charging time for bootstrap capacitors need to be separated, as shown in Figure 31 if amount of initial current during short time should be minimized. The effect of the bootstrap capacitance factor and charging method (low−side IGBT driving method) is shown in Figure 32.

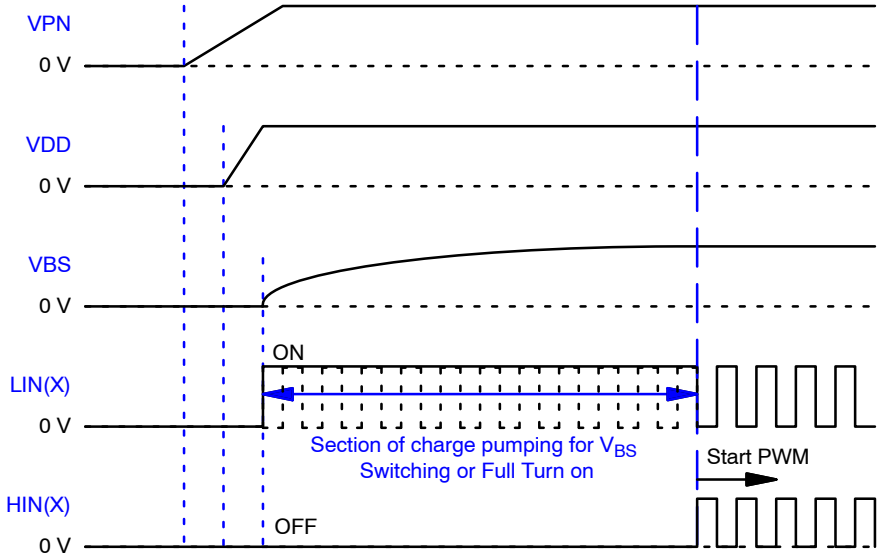


Figure 30. Timing Chart of Initial Bootstrap Charging

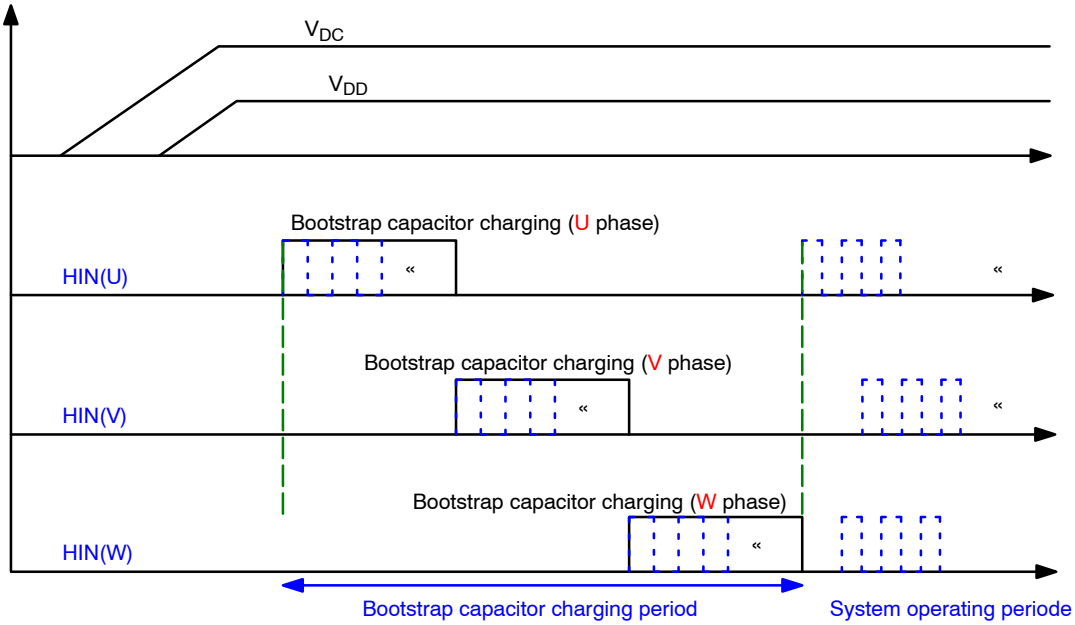


Figure 31. Recommended Initial Bootstrap Capacitors Charging Sequence

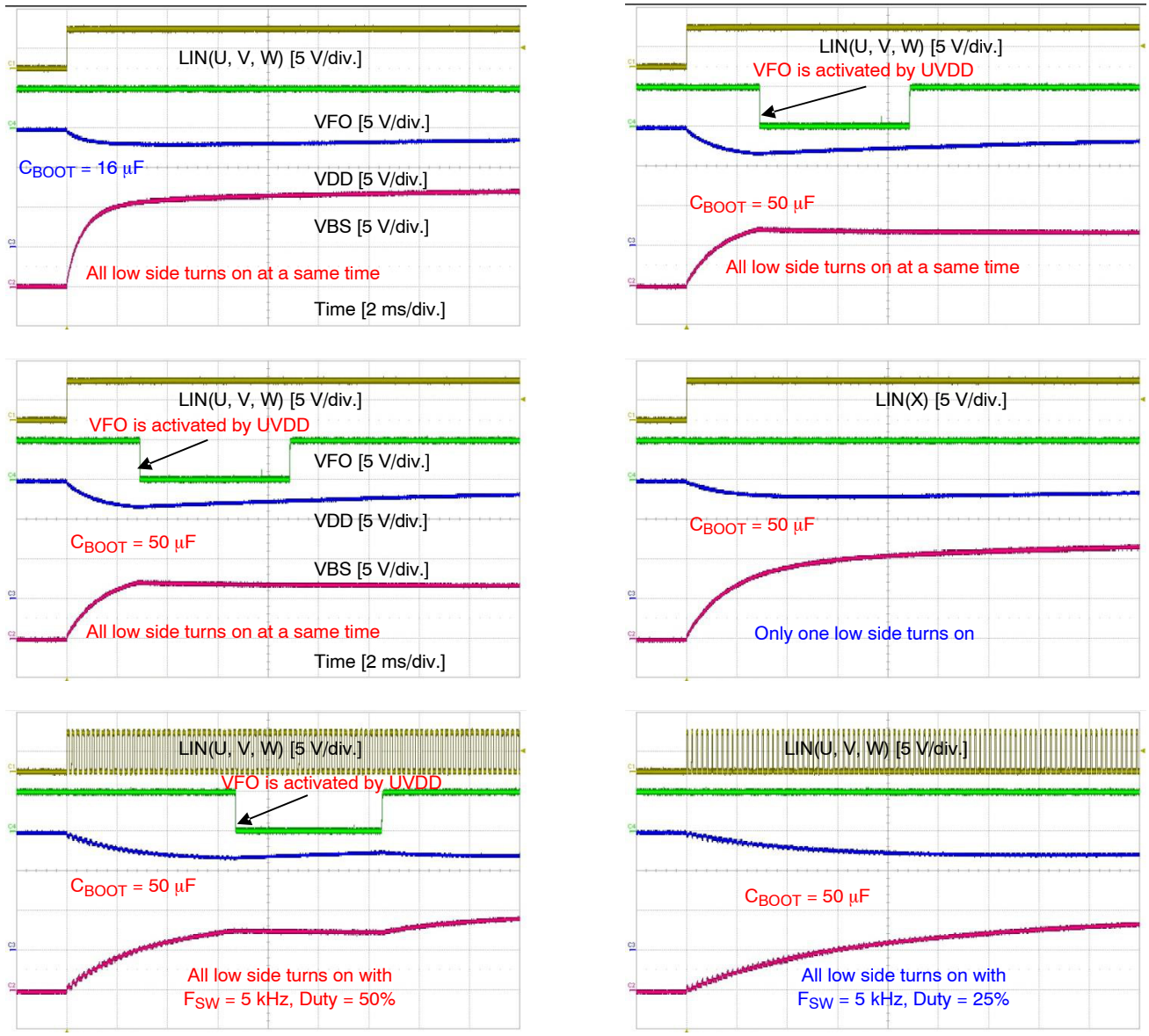


Figure 32. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: VDD = 15 V / 300 mA, VDD Capacitor = 220 μF, C_{BOOT} = 100 μF, R_{BOOT} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BOOT} = \frac{I_{leak} \times \Delta t}{\Delta VBS} \quad \text{(eq. 2)}$$

Where:

Δt: maximum on pulse width of high−side IGBT;

ΔVBS: the allowable discharge voltage of the C_{BOOT} (voltage ripple); and

ILeak: maximum discharge current of the C_{BOOT}.

Mainly via the following mechanisms:

Gate charge for turning the high−side IGBT on.

Quiescent current to the high−side circuit in HVIC.

Level−shift charge required by level−shifters in HVIC.

Leakage current in the bootstrap circuit.

C_{BOOT} capacitor leakage current (ignored for non−electrolytic capacitors).

Bootstrap diode reverse recovery charge.

Practically, 4.5 mA of I Leak is recommended for the 1200 V SPM 31 series. By considering dispersion and reliability, the capacitance is generally selected to be 2~3 times the calculated one. The C_{BOOT} is only charged when the high−side IGBT is off and the VS(x) voltage is pulled down to ground.

The on−time of the low−side IGBT must be sufficient to for the charge drawn from the C_{BOOT} capacitor to be fully replenished. This creates an inherent minimum on−time of the low−side IGBT (or off−time of the high−side IGBT).

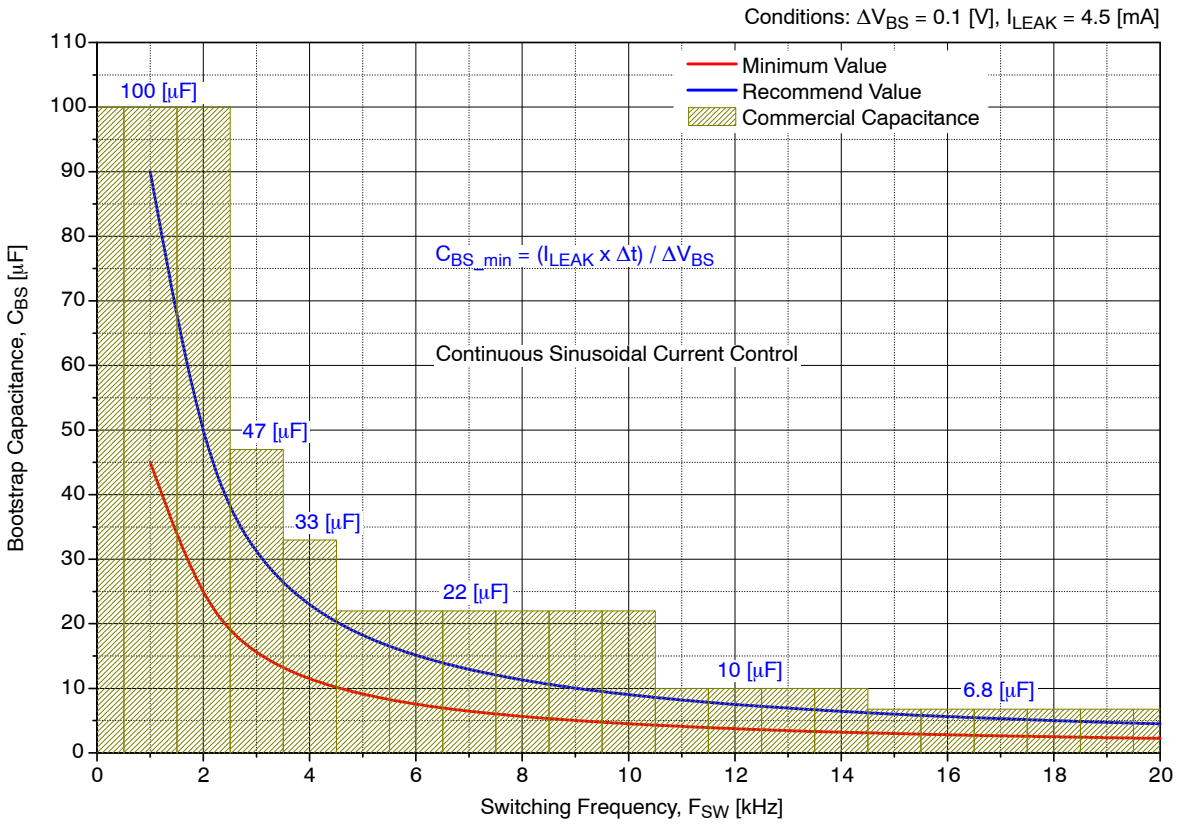


Figure 33. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔVBS.

I_{Leak}: circuit current = 4.5 mA (recommended value)

ΔVBS: discharged voltage = 1.0 V (recommended value)

Δt: maximum on pulse width of high−side IGBT = 0.2 ms (depends on application)

$C_{BOOT\_min} = ((I_{leak} \times \Delta t) / \Delta V_{BS}) = ((4.5\ mA \times 0.2\ ms) / 1.0\ V) = 9 \times 10^{-6}$

→ More than 2 times → 18 μF. (22 μF STD value)

NOTE: The capacitance value can be changed according to the switching frequency, the capacitor selected, and the recommended VBS voltage of 13.0~18.5 V (from datasheet). The above result is just a calculation example. This value can be changed according to the actual control method and lifetime of the component.

Built−in Bootstrap Circuit

When the low−side IGBT or diode conducts, the bootstrap diode (D_{BOOT}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 1200 V is recommended. It is important that this diode has a fast recovery (recovery time <100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the VDD supply. The bootstrap resistor (R_{BOOT}) is to slow down the dVBS/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BOOT}), bootstrap resistor (R_{BOOT}), and bootstrap capacitor (C_{BOOT}). As shown in Figure 34, the built−in bootstrap circuit of SPM 31 product has series resistor to be used without additional bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built−in bootstrap diode in the SPM 31 products are:

Fast recovery diode: more than 1200 V / 2 A

Resistive characteristic: equivalent resistor of approximately 38 Ω

Table 7 shows the specification of bootstrap circuit. Figure 34 shows forward voltage drop and reverse recovery characteristic of the bootstrap diode.

Table 7. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VF	Forward−Drop Voltage	If = 0.1 A, Tc = 25°C	3.4	4.6	5.8	V
RBOOT	Built−in Limiting Resistance		30	38	46	Ω

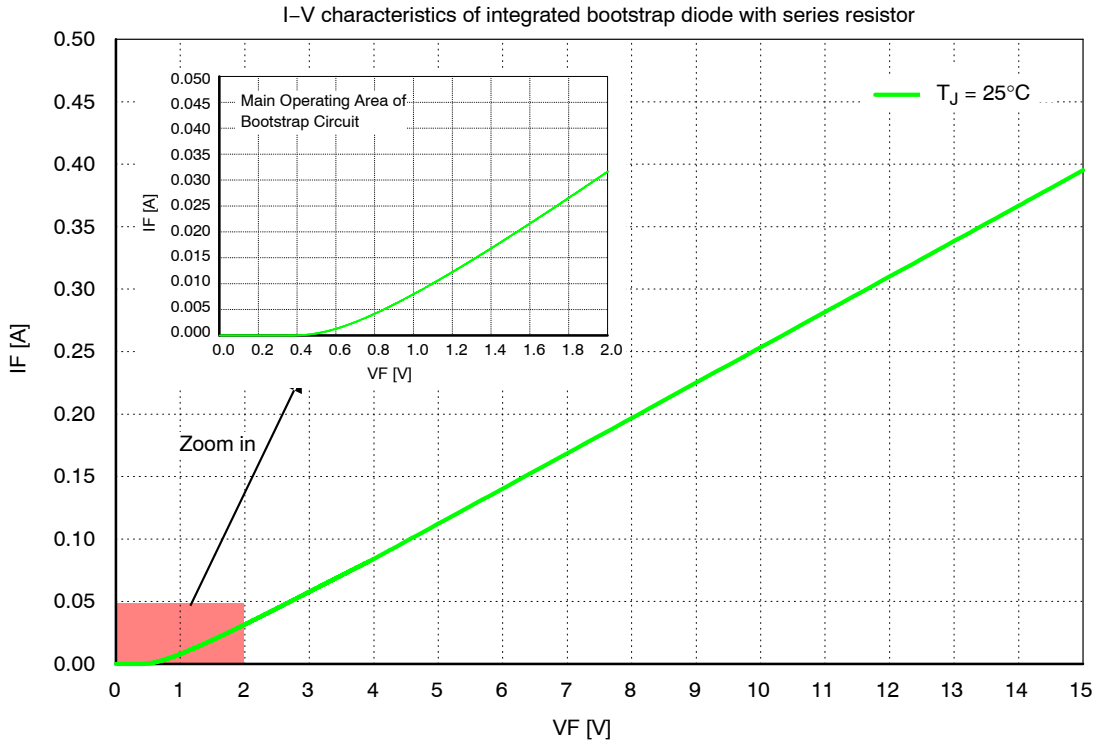


Figure 34. V−I characteristics of Bootstrap Circuit in SPM 31 Series Products

PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 35 shows a general application circuitry of interface schematic with control signals connected directly to a MCU. Figure 36 shows guidance of PCB layout for the 1200 V SPM 31 series.

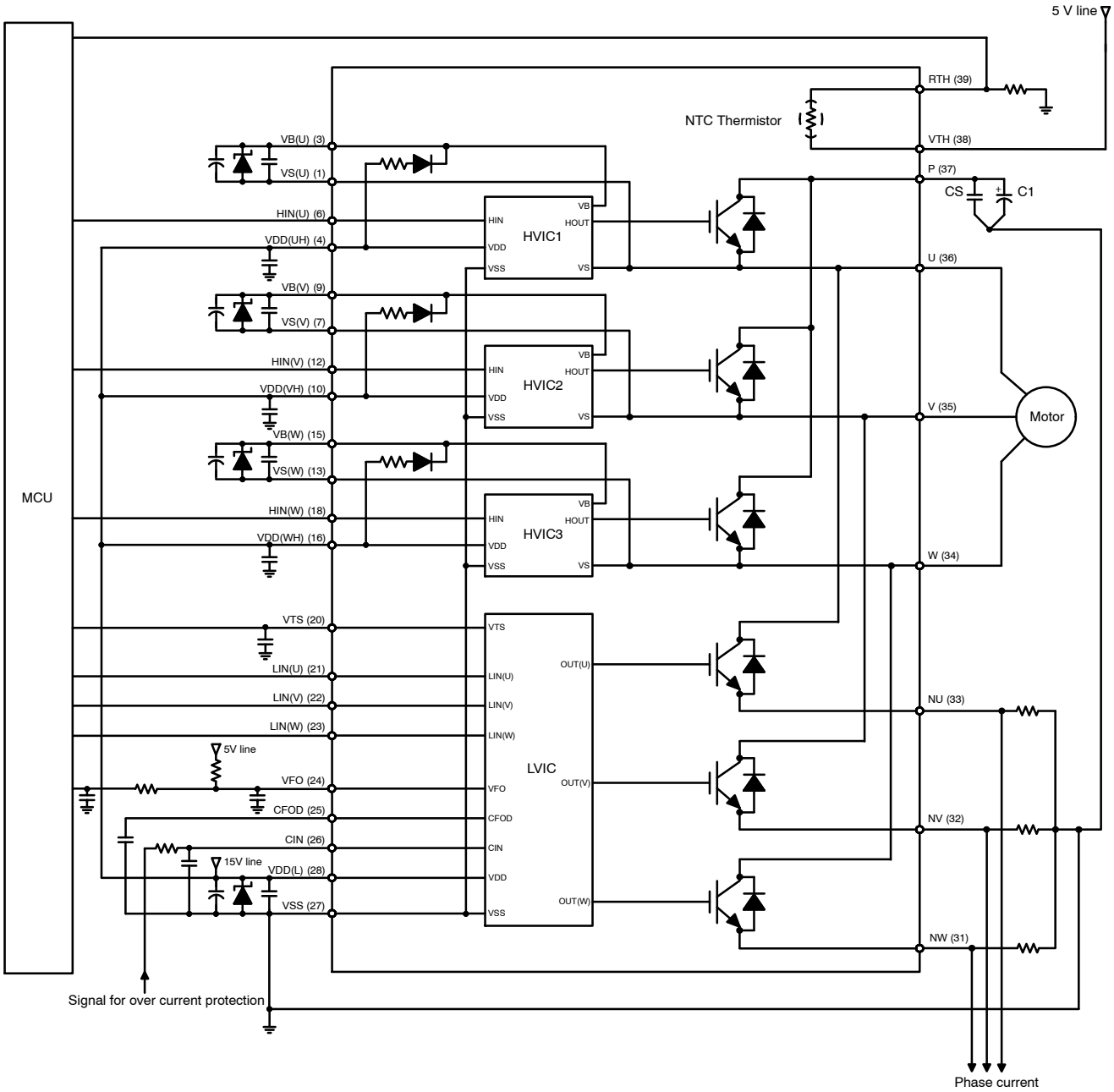


Figure 35. General Application Circuitry for 1200 V Motion SPM 31

PCB Layout Guidance

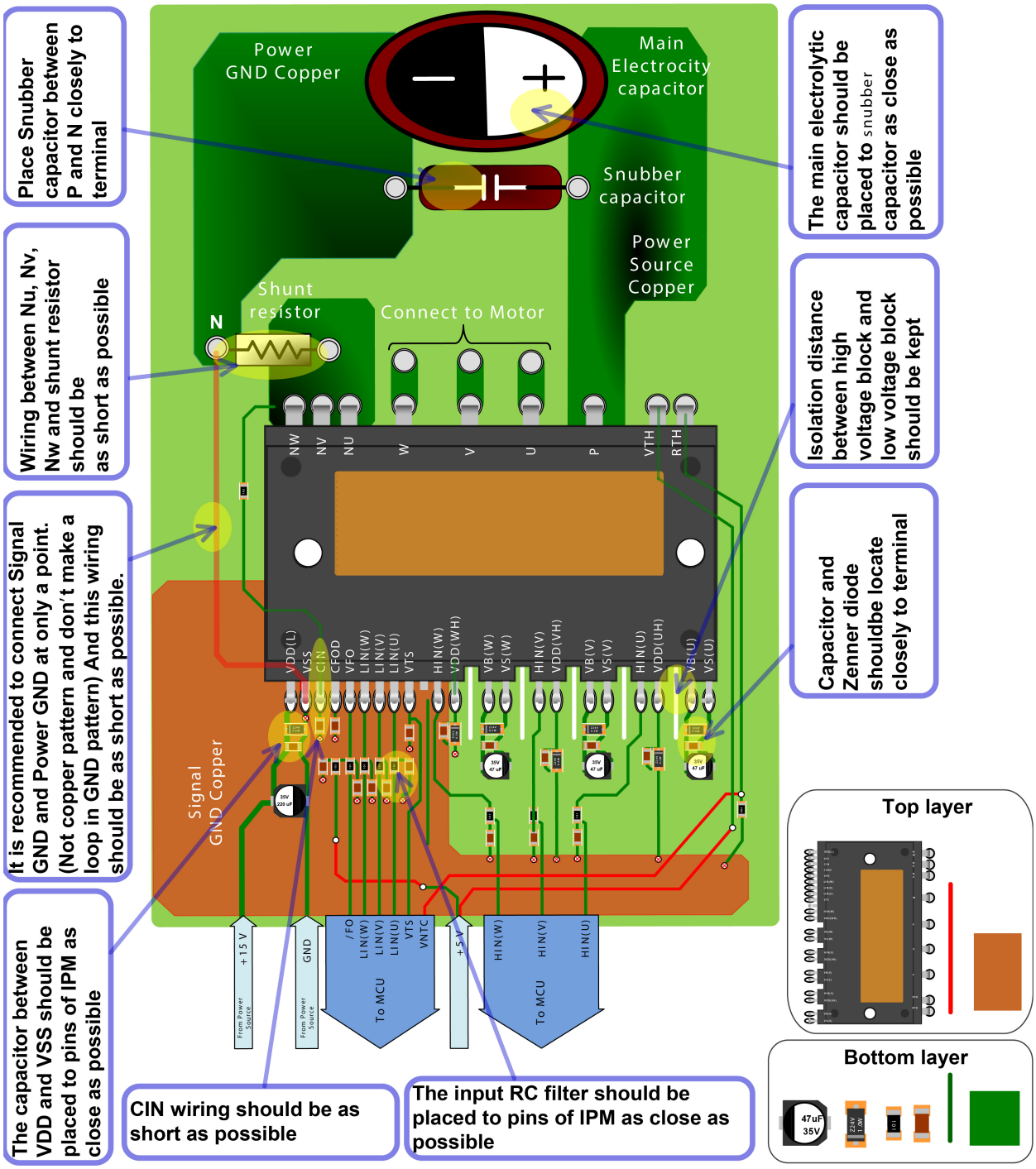


Figure 36. Print Circuit Board (PCB) Layout Guidance for SPM 31 Series

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊