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AND9910/D

3-Phase Inverter Power Module Application Note for the STK544UC63K-E

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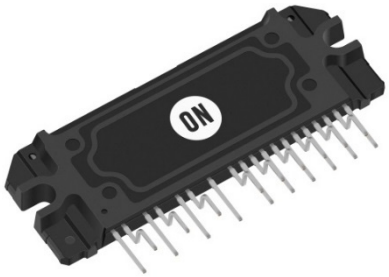
APPLICATION NOTE



Introduction

This application note provides practical guidelines for designing with the STK544UC63K−E power modules.

The STK544UC63K−E is an Intelligent Power Module (IPM) for 3−phase motor drives containing a three−phase inverter stage, gate drivers for the inverter stages and a thermistor. It uses ON Semiconductor Insulated Metal Substrate (IMS) Technology.

Key Functions

- Highly integrated device containing all High Voltage (HV) control from HV−DC to 3−phase outputs in a single small SIP module
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over−current Protection (OCP). Internal bootstrap diodes are provided for the high−side drivers
- Separate pins for each of the three low−side emitter terminals
- Thermistor for substrate temperature measurement
- All control inputs and status outputs have voltage levels compatible with microcontrollers
- Single V_{DD} power supply due to internal bootstrap circuit for high−side gate driver circuit
- Mounting holes for easy assembly of heat sink with screws

A simplified block diagram of a motor control system is shown in Figure 1.

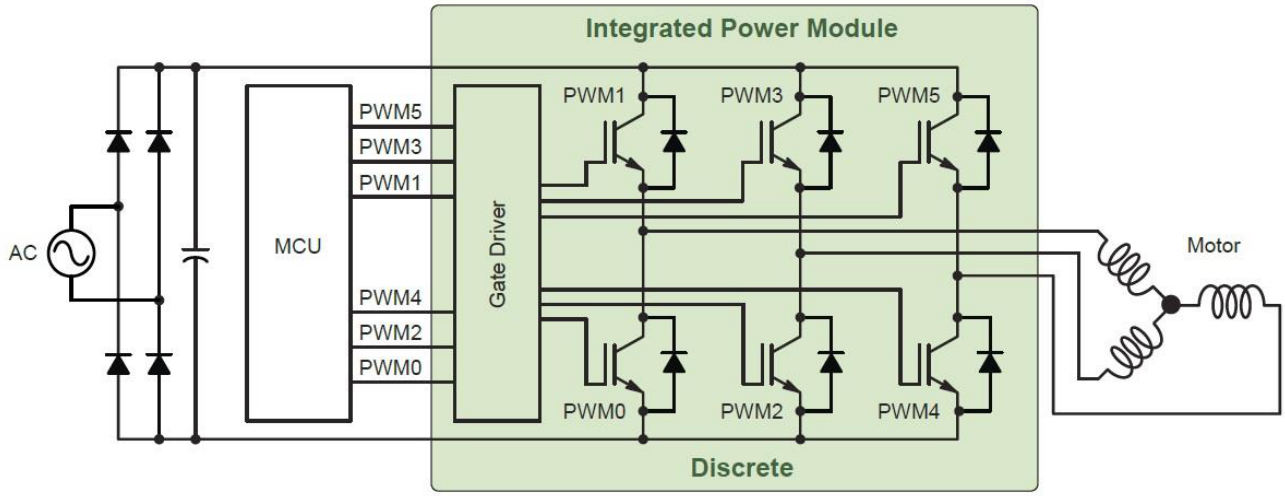


Figure 1. Motor Control System Block Diagram

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Product Description

Table 1 gives an overview of the available devices in the STK544UC63K−E series. For package drawing, please refer to Package Outline chapter.

Table 1. DEVICE OVERVIEW

Device	STK544UC63K−E
Package	SIP23 62x21.8FP−4– Vertical pins
Voltage (VCEmax.)	600 V
Current (Ic)	10 A
Peak current (Ic)	20 A
Isolation voltage	2000 V
Input logic	Low−active
Shunt resistance	triple shunts / external

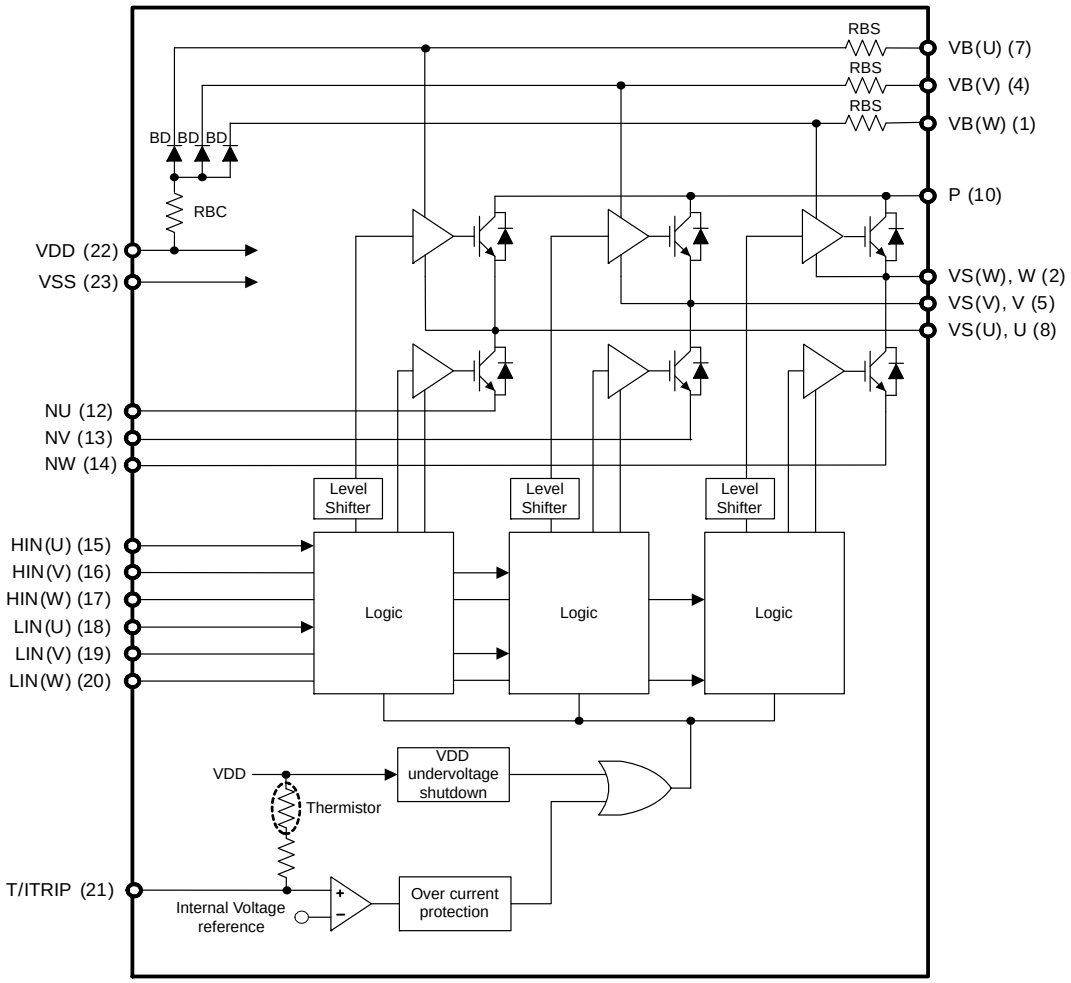


Figure 2. STK544UC63K−E Series Internal Diagram

Three bootstrap circuits generate the voltage needed for driving the high−side IGBTs. The boost diodes are internal to the part and sourced from VDD (15V). There is an internal level shift circuit for the high−side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with photo couplers.

Performance Test Guidelines

The methods used to test some datasheet parameters are shown in Figures 3 to 7.

Switching Time Definition and Performance Test Method

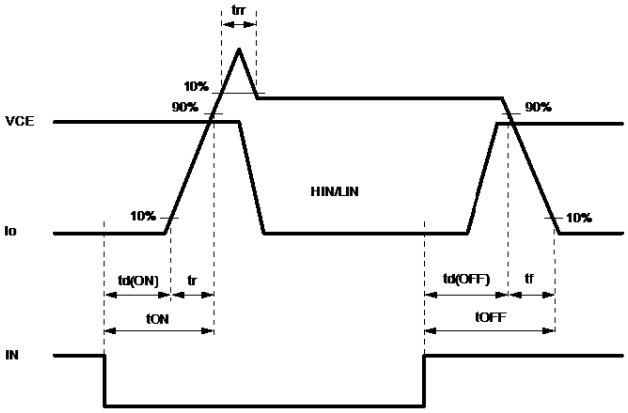


Figure 3. Switching Time Definition

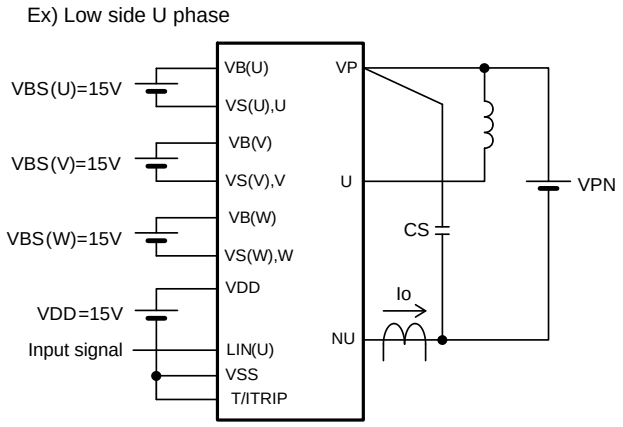


Figure 4. Evaluation Circuit (Inductive load)

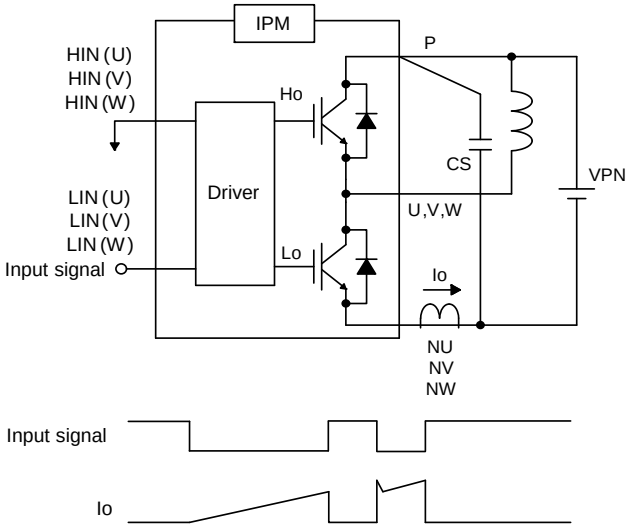


Figure 5. Switching Loss Measurement Circuit

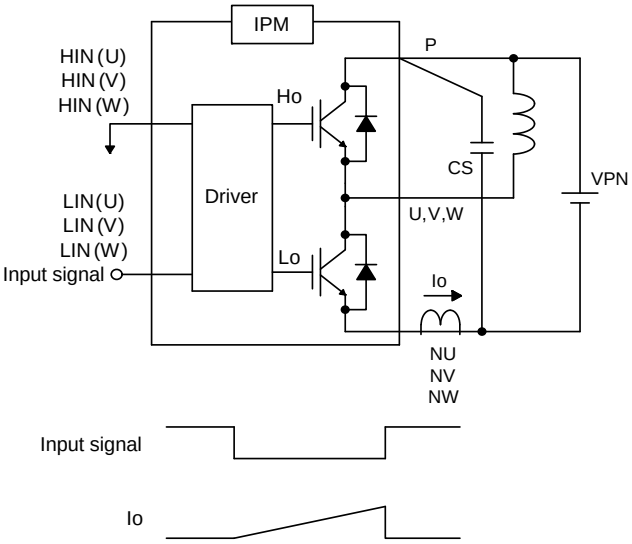


Figure 6. Reverse Bias Safe Operating Area Measurement Circuit

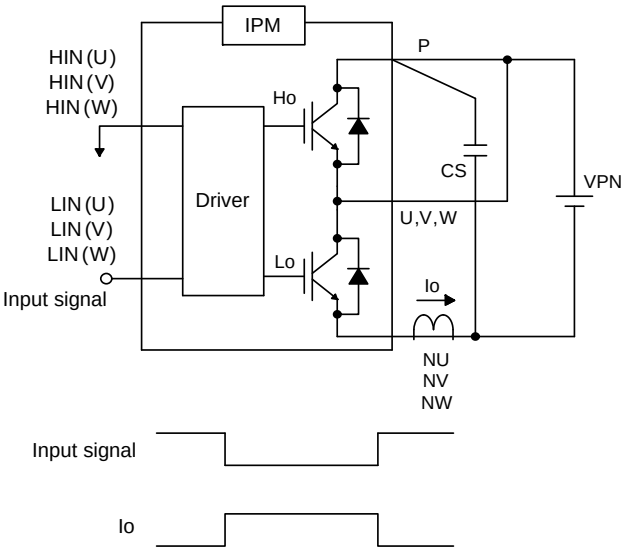


Figure 7. Short Circuit Safe Operating Area Measurement Circuit

Thermistor Characteristics

The T/ITRIP pin are connected to a thermistor mounted on the module substrate. The thermistor is used to sense the internal substrate temperature. It has the following characteristics.

Table 2. NTC THERMISTOR SPECIFICATION

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25°C	99	100	101	kΩ
Resistance	R_{125}	Tc = 125°C	2.40	2.52	2.65	kΩ
B−Constant (25 to 50°C)	B		4207	4250	4293	K
Temperature Range			−40		+125	°C

R_{25} is the value of the integrated NTC thermistor at Tc = 25°C. The resistance value is 100 kΩ ±3% and the value of the B−Constant (25−50°C) is 4250K ±1%. The temperature depended value is calculated as shown in the formula.

$$R(t) = R_{25} \times e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

The resulting in the NTC values over temperatures

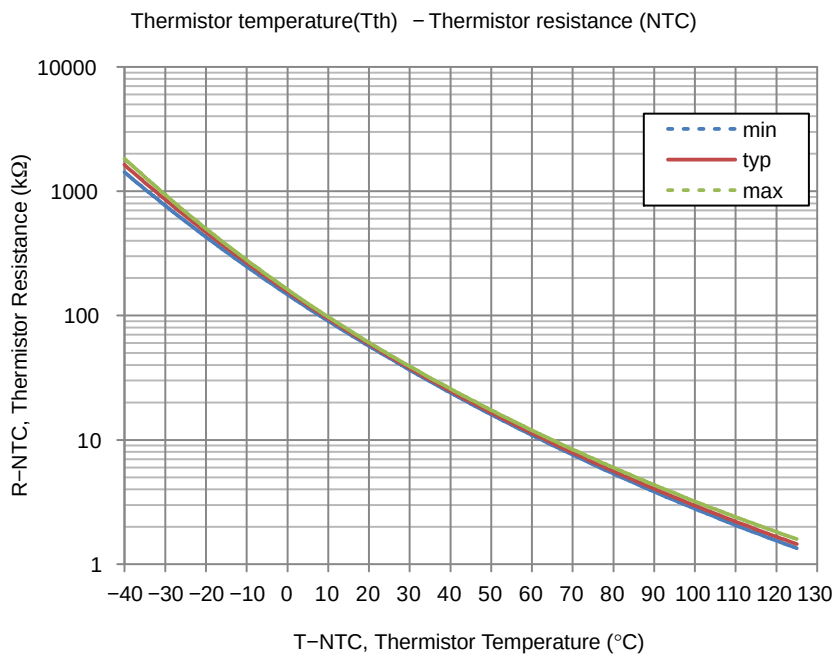


Figure 8. NTC Thermistor Resistance versus Temperature

Table 3. NTC THERMISTOR RESISTANCE VALUES

Tc [°C]	Resistance value [kΩ]			Tc [°C]	Resistance value [kΩ]			Tc [°C]	Resistance value [kΩ]		
	Min	Typ	Max		Min	Typ	Max		Min	Typ	Max
−40	4191.52	4397.12	4612.34	16	152.51	154.73	156.96	72	13.69	14.1	14.52
−39	3904.3	4092.87	4290.13	17	145.2	147.23	149.28	73	13.19	13.59	14
−38	3638.69	3811.72	3992.58	18	138.27	140.14	142.02	74	12.71	13.1	13.51
−37	3392.92	3551.75	3717.65	19	131.72	133.43	135.16	75	12.25	12.64	13.03
−36	3165.38	3311.24	3463.47	20	125.51	127.08	128.66	76	11.81	12.19	12.57
−35	2954.6	3088.6	3228.35	21	119.63	121.07	122.51	77	11.39	11.76	12.13
−34	2759.25	2882.4	3010.74	22	114.05	115.37	116.69	78	10.99	11.34	11.71
−33	2578.1	2691.31	2809.21	23	108.77	109.97	111.17	79	10.6	10.95	11.3
−32	2410.02	2514.14	2622.49	24	103.75	104.85	105.95	80	10.23	10.57	10.91
−31	2253.99	2349.78	2449.39	25	99	100	101	81	9.87	10.2	10.54
−30	2109.07	2197.23	2288.84	26	94.4	95.4	96.4	82	9.53	9.85	10.18
−29	1974.4	2055.56	2139.84	27	90.04	91.03	92.03	83	9.2	9.51	9.83
−28	1849.2	1923.93	2001.49	28	85.9	86.89	87.88	84	8.88	9.18	9.5
−27	1732.73	1801.57	1872.97	29	81.97	82.96	83.94	85	8.57	8.87	9.18
−26	1624.34	1687.77	1753.51	30	78.25	79.22	80.2	86	8.28	8.57	8.87
−25	1523.41	1581.88	1642.43	31	74.71	75.68	76.65	87	8	8.28	8.58
−24	1429.2	1483.1	1538.88	32	71.35	72.31	73.27	88	7.73	8.01	8.29
−23	1341.42	1391.11	1442.51	33	68.16	69.1	70.05	89	7.47	7.74	8.02
−22	1259.58	1305.41	1352.78	34	65.13	66.06	67	90	7.22	7.48	7.75
−21	1183.25	1225.53	1269.2	35	62.25	63.17	64.09	91	6.98	7.23	7.5
−20	1112.02	1151.04	1191.3	36	59.51	60.42	61.33	92	6.75	7	7.26
−19	1045.53	1081.54	1118.67	37	56.91	57.8	58.7	93	6.52	6.77	7.02
−18	983.42	1016.66	1050.92	38	54.43	55.31	56.19	94	6.31	6.55	6.8
−17	925.39	956.08	987.69	39	52.07	52.93	53.8	95	6.1	6.34	6.58
−16	871.14	899.48	928.65	40	49.83	50.68	51.53	96	5.9	6.13	6.37
−15	820.4	846.58	873.51	41	47.7	48.53	49.37	97	5.71	5.93	6.17
−14	772.93	797.11	821.97	42	45.67	46.48	47.31	98	5.53	5.74	5.97
−13	728.49	750.83	773.79	43	43.73	44.53	45.34	99	5.35	5.56	5.78
−12	686.88	707.52	728.72	44	41.89	42.67	43.47	100	5.18	5.38	5.6
−11	647.89	666.97	686.55	45	40.13	40.9	41.68	101	5.01	5.21	5.42
−10	611.35	628.99	647.07	46	38.46	39.21	39.98	102	4.85	5.05	5.26
−9	577.04	593.34	610.04	47	36.86	37.6	38.35	103	4.7	4.89	5.09
−8	544.86	559.93	575.36	48	35.34	36.06	36.8	104	4.55	4.74	4.94
−7	514.67	528.6	542.85	49	33.89	34.6	35.31	105	4.41	4.59	4.79
−6	486.34	499.21	512.38	50	32.5	33.19	33.9	106	4.27	4.45	4.64
−5	459.73	471.63	483.79	51	31.18	31.86	32.55	107	4.14	4.32	4.5
−4	434.77	445.77	457.01	52	29.92	30.58	31.26	108	4.01	4.18	4.36
−3	411.31	421.48	431.86	53	28.72	29.37	30.03	109	3.89	4.06	4.23
−2	389.25	398.65	408.25	54	27.57	28.2	28.85	110	3.77	3.93	4.1
−1	368.5	377.19	386.06	55	26.47	27.09	27.72	111	3.66	3.82	3.98
0	348.97	357.01	365.2	56	25.42	26.03	26.64	112	3.55	3.7	3.86
1	330.58	338.01	345.57	57	24.42	25.01	25.62	113	3.44	3.59	3.75
2	313.25	320.12	327.11	58	23.46	24.04	24.63	114	3.33	3.48	3.64
3	296.94	303.29	309.74	59	22.55	23.11	23.69	115	3.24	3.38	3.53
4	281.57	287.43	293.39	60	21.67	22.22	22.79	116	3.14	3.28	3.43
5	267.08	272.5	278	61	20.84	21.37	21.92	117	3.05	3.19	3.33
6	253.42	258.43	263.5	62	20.04	20.56	21.1	118	2.96	3.09	3.23
7	240.54	245.16	249.84	63	19.27	19.78	20.31	119	2.87	3	3.14
8	228.39	232.65	236.97	64	18.54	19.04	19.55	120	2.79	2.92	3.05
9	216.91	220.85	224.83	65	17.83	18.32	18.82	121	2.71	2.83	2.96
10	206.08	209.71	213.38	66	17.16	17.64	18.13	122	2.63	2.75	2.88
11	195.85	199.2	202.58	67	16.52	16.99	17.46	123	2.55	2.67	2.8
12	186.18	189.27	192.38	68	15.91	16.36	16.83	124	2.48	2.6	2.72
13	177.05	179.89	182.76	69	15.32	15.76	16.21	125	2.41	2.52	2.64
14	168.41	171.03	173.67	70	14.75	15.18	15.63				
15	160.24	162.65	165.08	71	14.21	14.63	15.06				

Protection Functions

This chapter describes the protection functions.

- Over−current protection
- Short circuit protection
- Under voltage lockout (UVLO) protection
- Cross conduction prevention

Over−current Protection

STK544UC63K−E modules use an external shunt resistor for the OCP functionality. As shown in Figure 9, the emitters of all three low−side IGBTs are brought out to module pins. The external OCP circuit consists of a shunt resistor and a RC filter network. If the application uses three separate shunt resistor, op−amp circuit or comparator circuit are used to monitor the three separate shunts and provide an over−current signal.

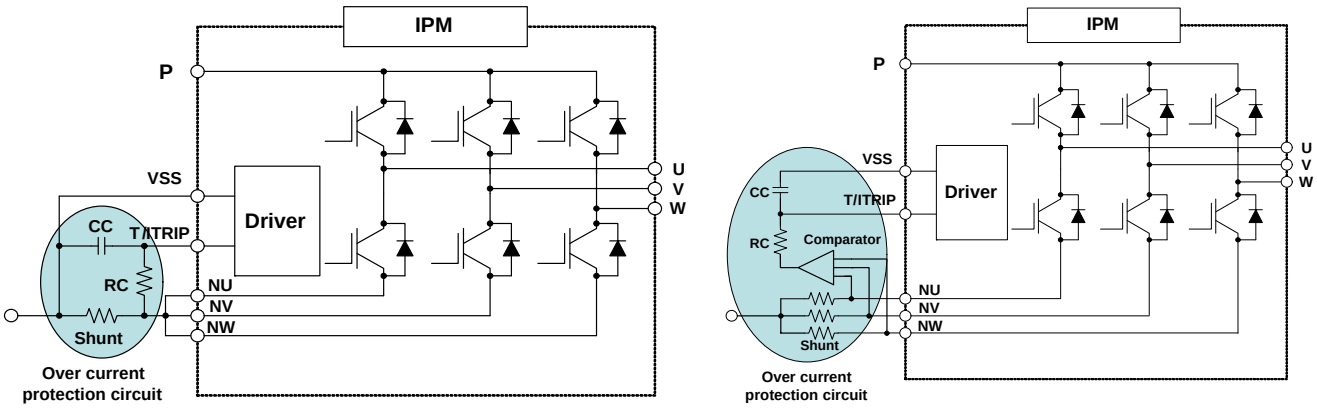


Figure 9. Over−current Protection Circuit, One Shunt R Type and Three Shunt R Type

The OCP function is implemented by comparing the T/ITRIP input voltage with an internal reference voltage of 4.17 V (typ). If the voltage on this terminal exceeds the trip level, an OCP fault is triggered. This voltage is the same as the voltage across the shunt resistor.

NOTE: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to less than the module's maximum current rating.

When an OCP fault is detected, all internal gate drive signals for the IGBTs become inactive.

A RC filter is used on the T/ITRIP input to prevent an erroneous OCP detection due to normal switching noise or recovery diode current. The time constant of that RC filter should be set to a value between 1.5 μs to 2 μs. The recommended RC filter value for the time constant 2 μs is as RC = 200 Ω, CC = 10 nF.

In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to Data Sheet for SCSOA. The resulting OCP level due to the filter time constant is shown in Figure 10.

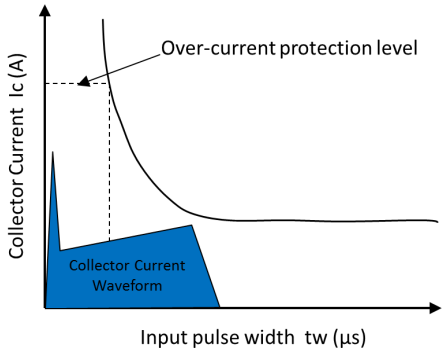


Figure 10. Filter Time Constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 11 shows the sequence of events in case of an OCP event.

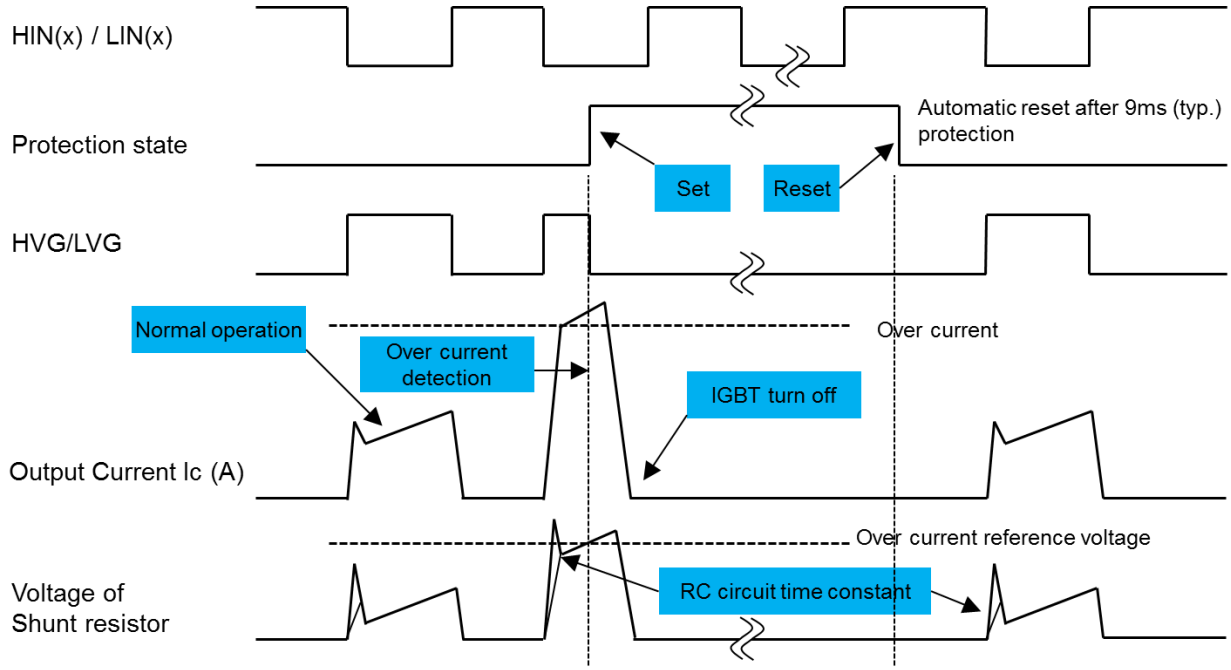


Figure 11. Over−current Protection Timing Diagram

Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 4. Both High−side and Low−side have under voltage protection.

Table 4. MODULE OPERATION ACCORDING TO VDD VOLTAGE

VDD Voltage (Typ. Value)	Operation Behavior
< 12.5 V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 14.0 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
14.0 V − 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short−circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. Rating is 20 V.

The sequence of events in case of a low−side UVLO event (IGBTs turned off) is shown in Figure 12.

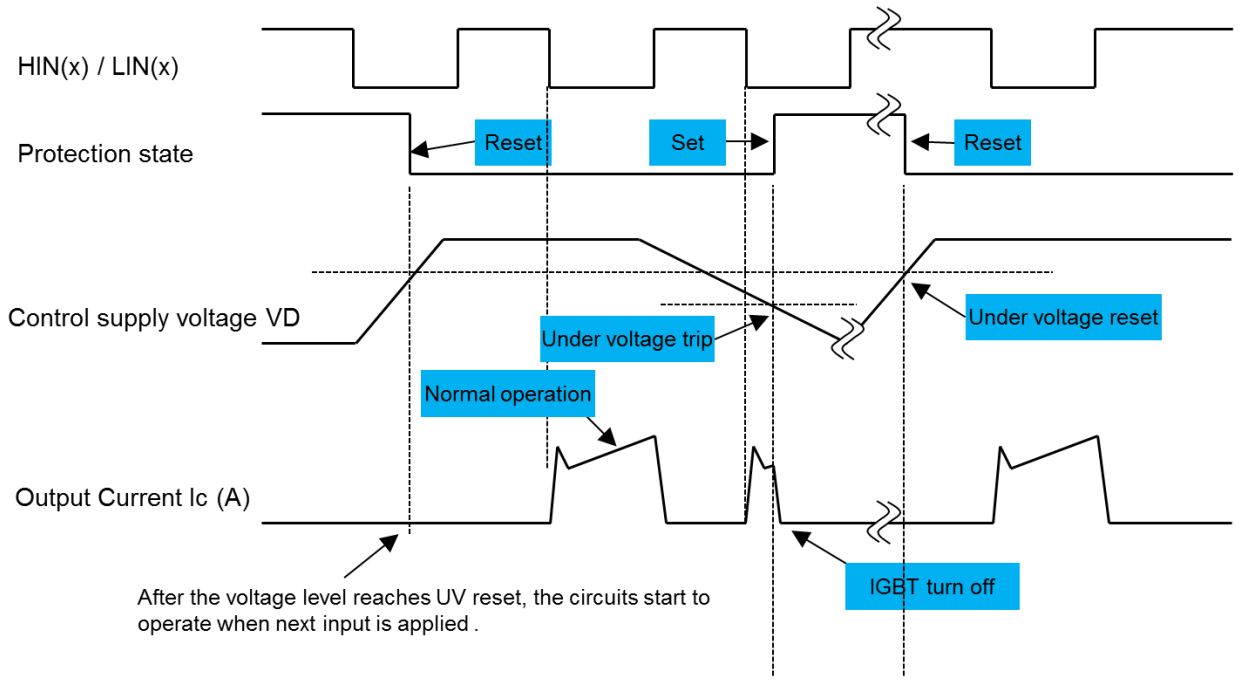


Figure 12. Low−side UVLO Timing Diagram

Cross−conduction Prevention

The STK544UC63K−E series implements cross−conduction prevention logic at the gate driver to avoid simultaneous drive of the low−side and high−side IGBTs as shown in Figure 13.

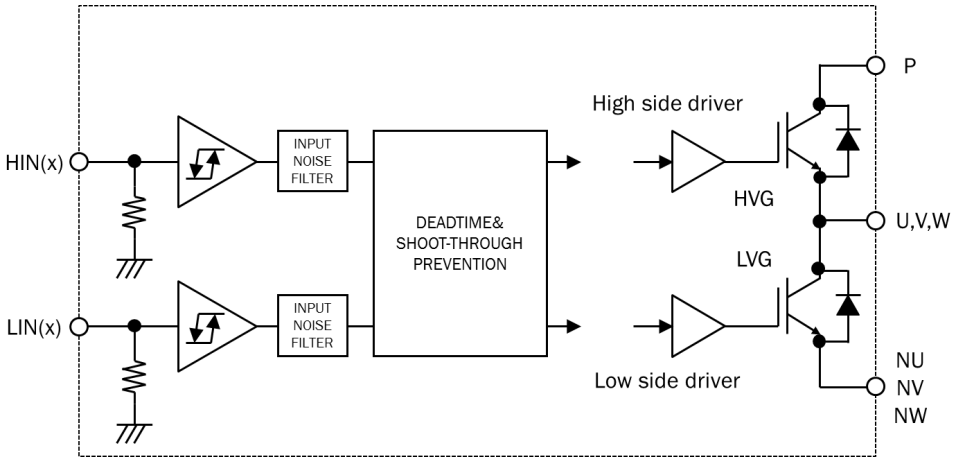


Figure 13. Cross−conduction Prevention

If both high−side and low−side drive inputs are active Low the logic prevents both gates from being driven as shown in Figure 14 below.

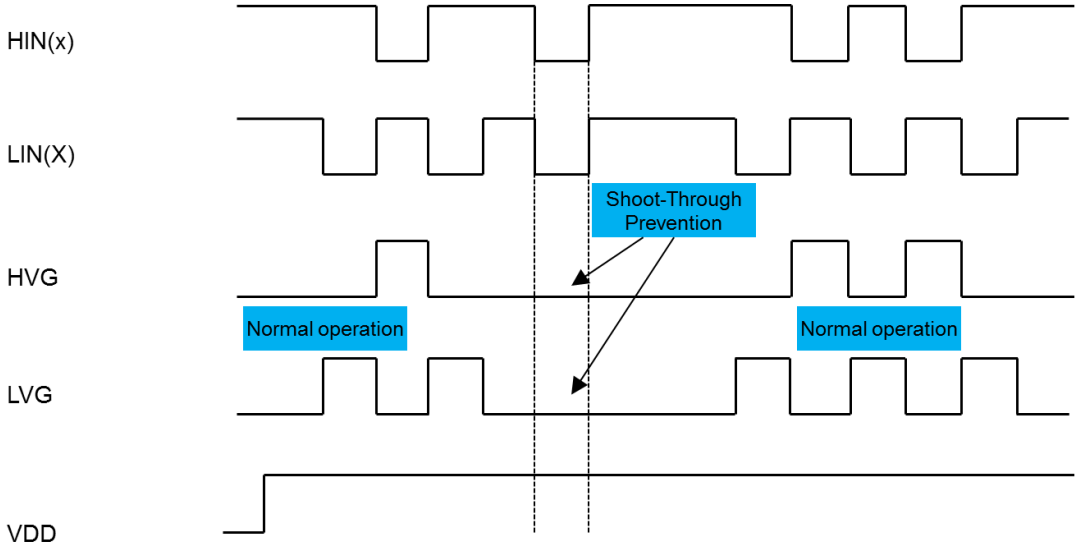


Figure 14. Cross−conduction Prevention Timing Diagram

Even if cross−conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry, the driving signals (HIN(x) and LIN(x)) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 15 shows the delay from the HIN(x)−input via the internal high−side gate driver to high−side IGBT, the delay from the LIN(x)−input via the internal low−side gate driver to low−side IGBT and the resulting minimum dead time which is equal to the potential shoot through period:

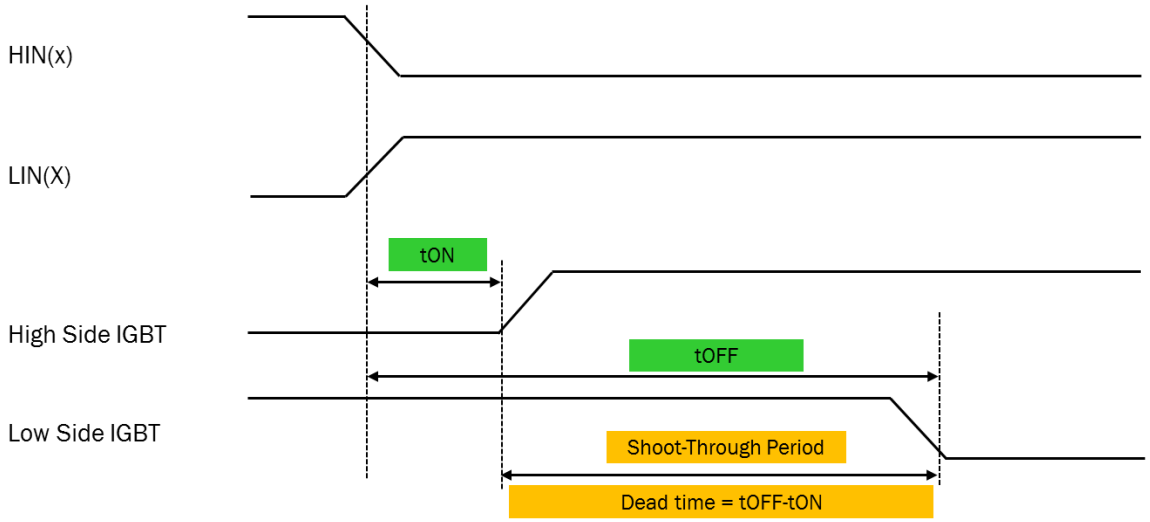


Figure 15. Shoot−through Period

PCB Design and Mounting Guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

Application (Schematic) Design

Figure 16 gives an overview of the external components and circuits when designing with the STK544UC63K−E series modules.

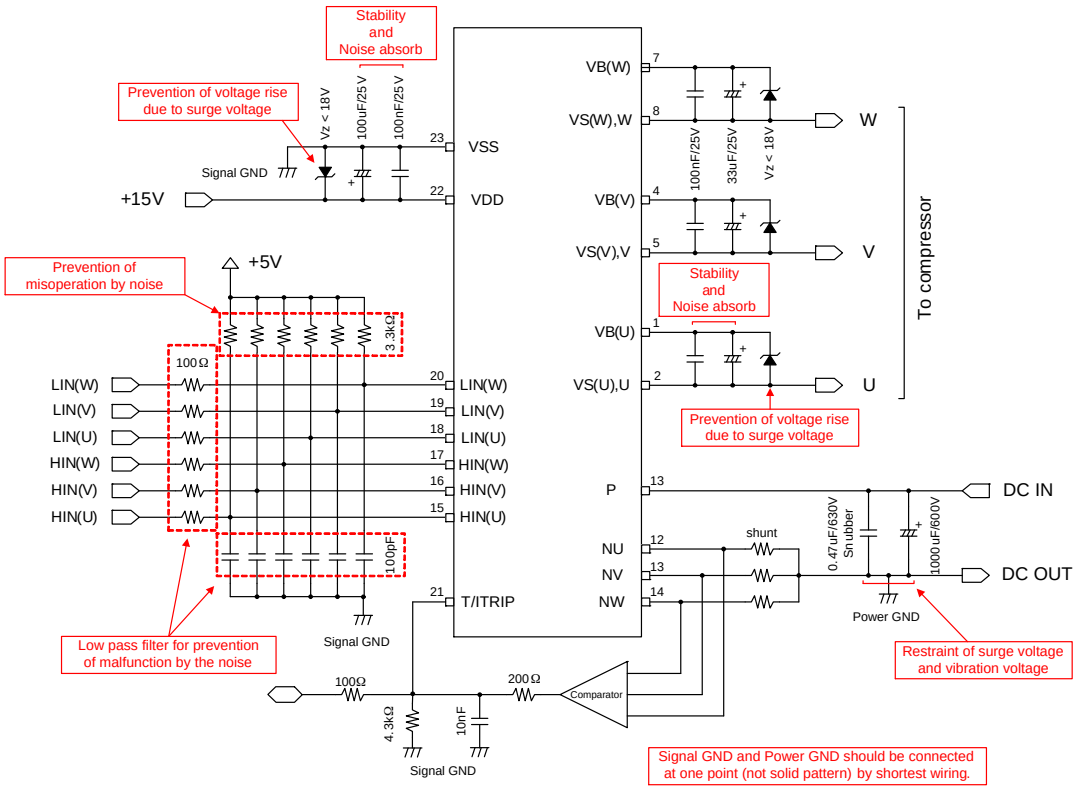


Figure 16. STK544UC63K−E Series Application Circuit

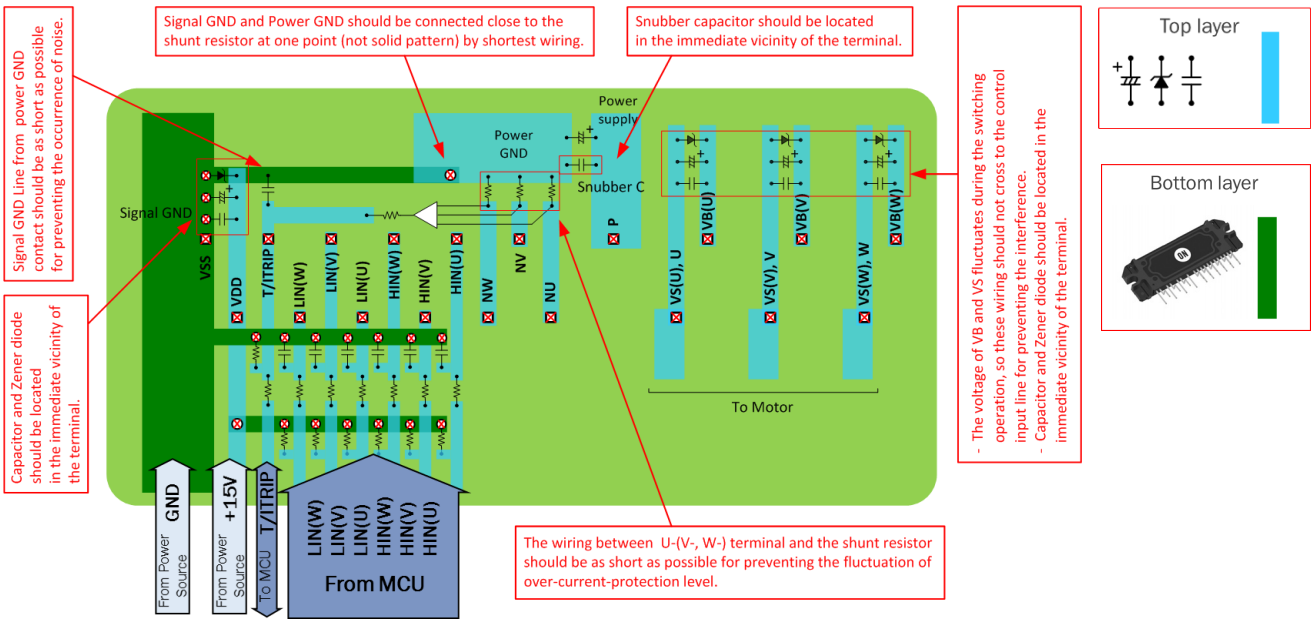


Figure 17. STK544UC63K−E Recommended Layout

Pin by Pin Design and Usage Notes

This section provides pin by pin PCB layout recommendations and usage notes. A complete list of module pins is given in Package Outline chapter.

P NU NV NW	These pins are connected with the main DC power supply. The applied voltage is up to the VPN level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.
VS(U),U VS(V),V VS(W),W	These are the output pins for connecting the 3−phase motor. They share the same GND potential with each of the high−side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.
VDD VSS	These pins provide power to the low−side gate drivers, the protection circuits and the bootstrap circuits. The voltage between these terminals is monitored by the UVLO circuit. The VSS terminal is the reference voltage for the input control signals. Since current flows instantaneously when switching IGBTs, place decoupling capacitor for ripple and surge noise as close as possible to the VDD terminal.
VB(U) VB(V) VB(W)	The VB(x) pins are internally connected to the positive supply of the high−side drivers. The supply needs to be floating and electrically isolated. The boot−strap circuit shown in Figure 18 forms this power supply individually for every phase. Due to integrated boot FET only an external boot capacitor (CB) is required. CB is charged when the following conditions are met. Motor terminal voltage is low level for low side IGBT or low side diode conducting. The capacitor is discharged while the high−side driver is activated. Thus CB needs to be selected taking the maximum on time of the high−side and the switching frequency into account.

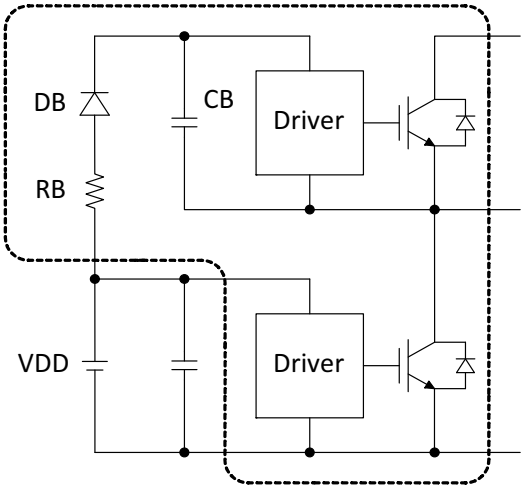


Figure 18. Bootstrap Circuit

The voltages on the high−side drivers are individually monitored by the under voltage protection circuit. If there is a UVLO fault on any given phase, the output on that phase is disabled.

Typically a CB value of less or equal 47uF (±20%) is used. In case the CB value needs to be higher, an external resistor (20 Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

HIN(U) HIN(V) HIN(W) LIN(U) LIN(V) LIN(W)	These pins are the control inputs for the power stages. The inputs on HIN(U)/HIN(V)/HIN(W) control the high−side transistors of U/V/W, and the inputs on LIN(U)/LIN(V)/LIN(W) control the low−side transistors of U/V/W respectively. The input are active Low and the input thresholds VIH and VIL are 5V compatible to allow direct control with a microcontroller system Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead−time.

The equivalent input stage circuit is shown in Figure 19.

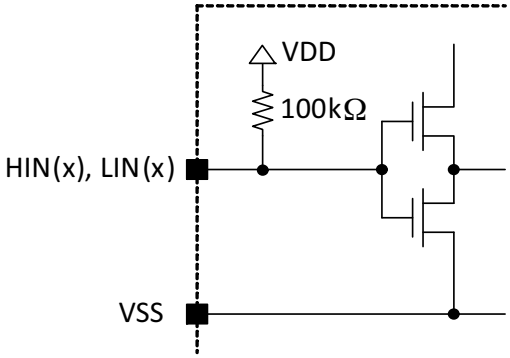


Figure 19. Internal Input Circuit

For fail safe operation the control inputs are internally tied to VDD via a 100kΩ (typ) resistor. To avoid switching captured by external wiring to influence the module behavior an additional external low−ohmic pull−up resistor with a value of 2.2 kΩ to 3.3 kΩ should be used.

The output might not respond when the width of the input pulse is less than 1 μs (both ON and OFF).

T/ITRIP An internal thermistor to sense the substrate temperature is connected between “VDD” and the “T/ITRIP” terminal. The substrate temperature is accessible externally by this terminal.

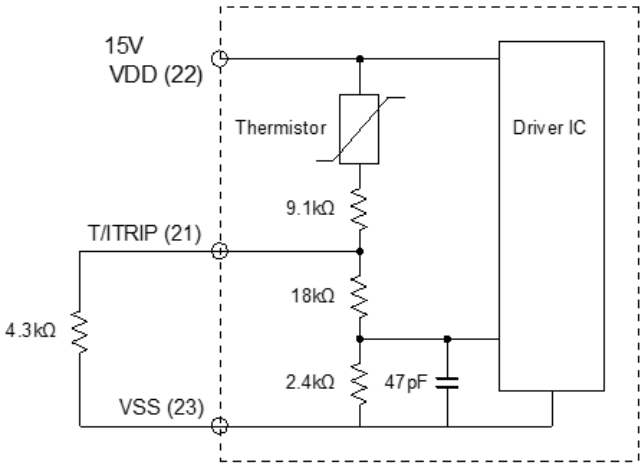


Figure 20. Internal Input Circuit

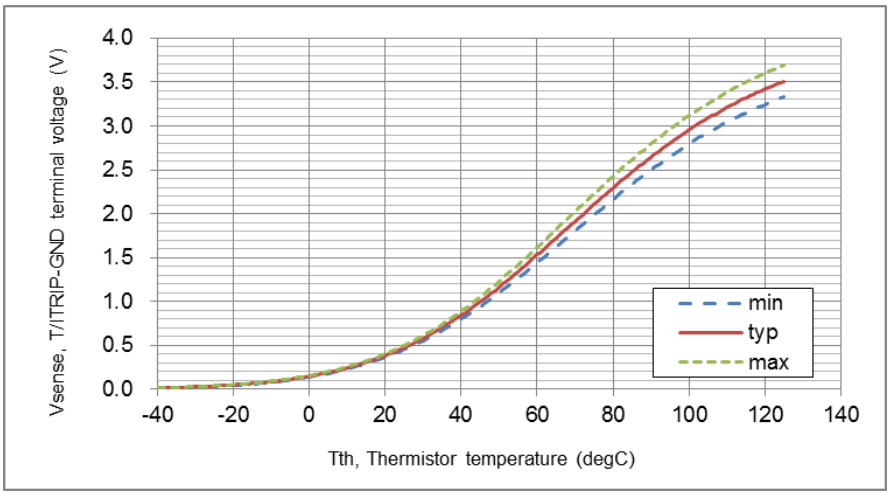


Figure 21. Variation of Temperature Sense Voltage with Internal Thermistor by using External Bias Resistance of 4.3 kΩ ±1% and VDD = 15 V

This terminal also has the function for shutdown input. When the input voltage to “T/ITRIP exceed threshold, all IGBTs are shut down. And Normal operation resumes 9 ms (typ.) after the condition of over current is removed.

Note: with this mimic only the substrate temperature can be monitored.

Heat Sink Mounting and Torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts IPM.
   - There must be no contamination on the heat sink surface that contacts IPM.
2. Highly thermal conductive silicone grease needs to be applied to the whole back (substrate side) uniformly, and mount IPM on a heat sink. If the device is removed, grease must be applied again.

3. For a good contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack.

The standard heat sink mounting condition of the STK544UC63K−E series is as follows.

Table 5. HEAT SINK MOUNTING

Item	Recommended Condition
Pitch	56.0 ± 0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Bind machine screw, Truss machine screw, Pan machine screw
Washer	Plane washer The size is D = 7 mm, d = 3.2 mm and t = 0.5 mm (Figure 23) JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : –50 to 100 μm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Final tightening : 0.6 to 0.9 Nm Temporary tightening : 20 to 30% of final tightening
Grease	Silicone grease. Thickness : 100 to 200 μm Uniformly apply silicon grease to whole back. (Figure 24)

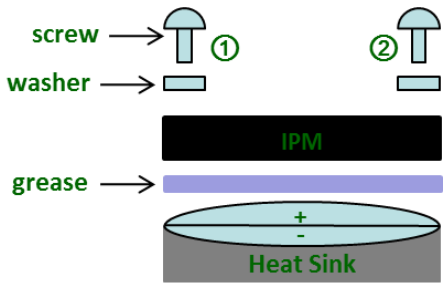


Figure 22. Mount IPM on a Heat Sink

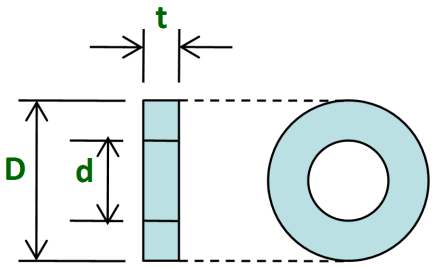


Figure 23. Size of Washer

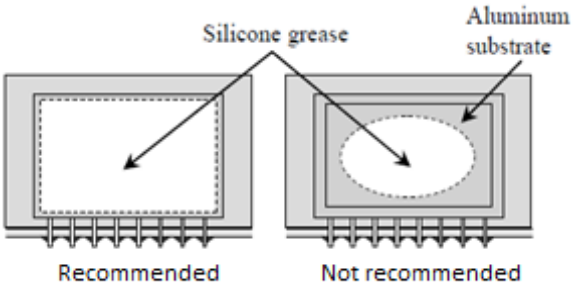


Figure 24. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink
1st: Temporarily tighten maintaining a left/right balance.
2nd: Finally tighten maintaining a left/right balance.

Mounting and PCB Considerations

In designs in which the PCB and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that slipping IPM is forcibly fixed to the heat sink with a screw.

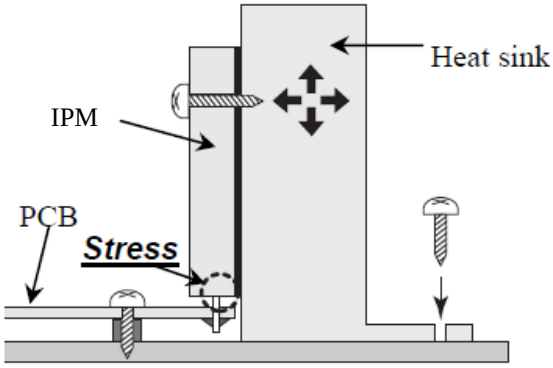


Figure 25. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the PCB. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the PCB. Do not mount IPM with a tilted condition for PCB. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the PCB. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out.

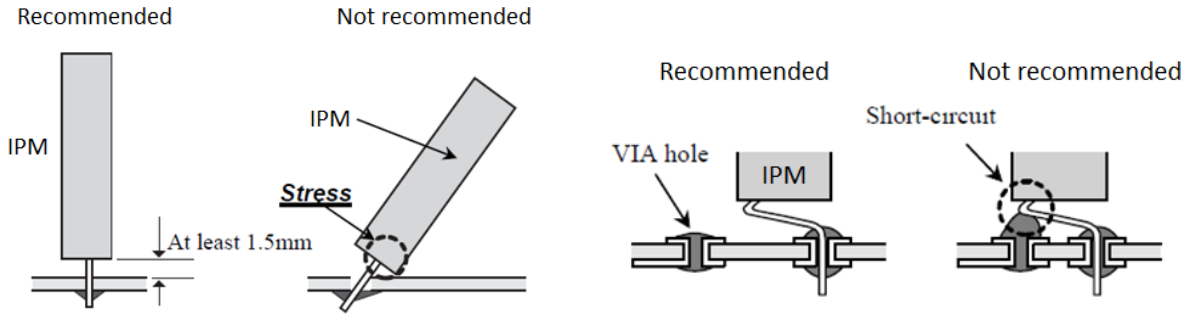


Figure 26. Mounting Position on PCB

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.IPMs are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the IPM should also be flame retard−ant.

Mounting on a PCB

1. Align the lead frame with the holes in the PCB and do not use excessive force when inserting the pins into the PCB. To avoid bending the lead frames, do not try to force pins into the PCB unreasonably.
2. Do not insert IPM into PCB with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPMs may be destroyed or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

Package Outline

STK544UC63K−E series is Single−inline−package.

Every second pin is bent forward to form two rows on the PCB see Figure 28.

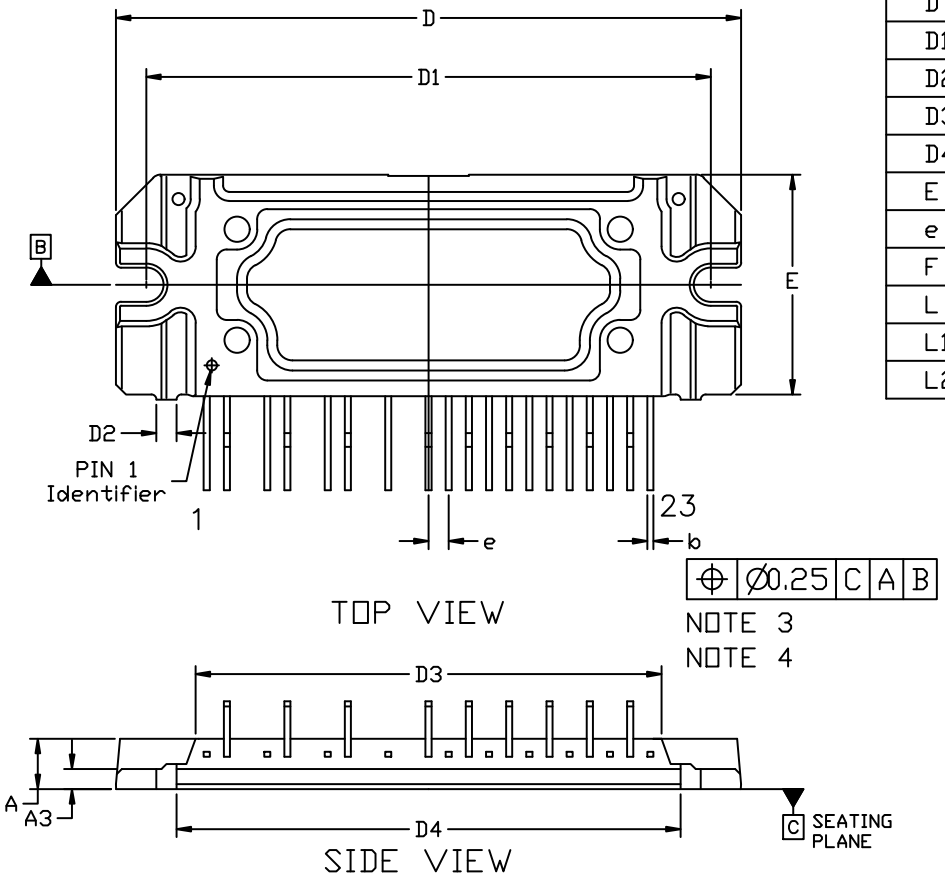
Package Outline and Dimension

Unit: mm

SIP23, 62x21.8 FP−4
CASE 127FC
ISSUE O

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. PIN 1 IDENTIFICATION IS A MIRRORED SURFACE INDENT.
6. MISSING PINS ARE 3,6,9 and 11.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.5	5.0	5.5
A1	2.7	3.2	3.7
A2	4.5	5.0	5.5
A3	1.5	2.0	2.5
b	0.55	0.6	0.8
c	0.45	0.5	0.7
D	61.5	62.0	62.5
D1	55.5	56.0	56.5
D2	1.5	2.0	2.5
D3	45.7	46.2	46.7
D4	49.5	50.0	50.5
E	21.3	21.8	22.3
e	2.0 REF		
F	2.9	3.4	3.9
L	8.5	9.0	9.5
L1	3.8	4.3	4.8
L2	0.0	0.5	1.0



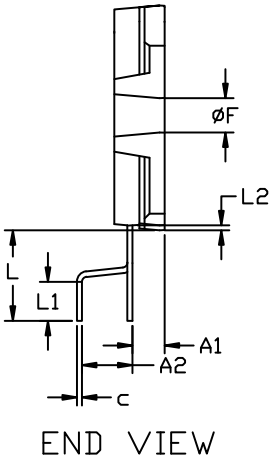


Figure 27. Package Outline

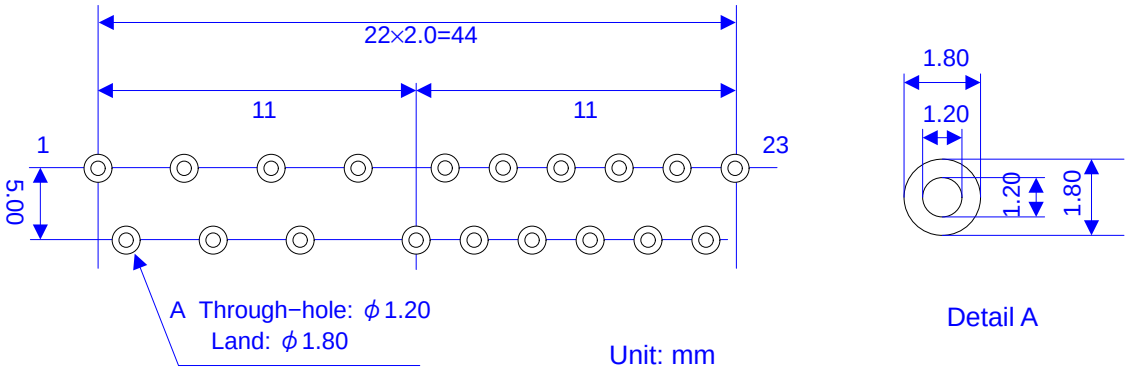
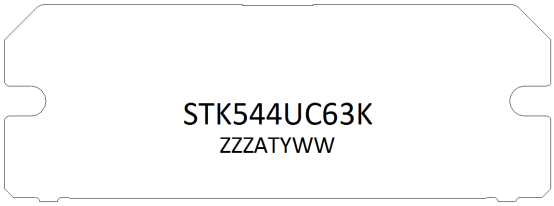


Figure 28. Recommended Land Pattern

Marking Diagram



STK544UC63K = Specific Device Code
ZZZ = Assembly Lot Code
A = Assembly Location
T = Test Location
Y = Year
WW = Work Week
Device marking is on package top side

Figure 29. Marking Diagram

Table 6. PIN OUT DESCRIPTION

Pin	Name	Description
1	VB(W)	High Side Floating Supply Voltage for W phase
2	VS(W),W	Internally connected to W phase high side driver ground. W phase output
4	VB(V)	High Side Floating Supply voltage for V phase
5	VS(V),V	Internally connected to V phase high side driver ground. V phase output
7	VB(U)	High Side Floating Supply voltage for U phase
8	VS(U),U	Internally connected to U phase high side driver ground. U phase output
10	P	Positive Bus Input Voltage
12	NU	Low Side Emitter Connection − Phase U
13	NV	Low Side Emitter Connection − Phase V
14	NW	Low Side Emitter Connection − Phase W
15	HIN(U)	Logic Input High Side Gate Driver − Phase U
16	HIN(V)	Logic Input High Side Gate Driver − Phase V
17	HIN(W)	Logic Input High Side Gate Driver − Phase W
18	LIN(U)	Logic Input Low Side Gate Driver − Phase U
19	LIN(V)	Logic Input Low Side Gate Driver − Phase V
20	LIN(W)	Logic Input Low Side Gate Driver − Phase W
21	T/ITRIP	Temperature Monitor and Shut−down pin
22	VDD	+15V Main Supply
23	VSS	Negative Main Supply

NOTE: Pins 3, 6, 9 and 11 are not present

PUBLICATION ORDERING INFORMATION

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