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Electric Vehicle OBC System Design and Simulation Using Power Modules

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APPLICATION NOTE

SUMMARY

The on−board charger (OBC) market is growing rapidly as the demand for battery powered electric vehicles is increasing worldwide. An OBC system is composed of AC−DC converter with power factor correction (PFC) cascaded with a DC−DC converter to control power delivery to the battery. Typically, a two−phase interleaved PFC is coupled with an LLC DC−DC for the 3.3 kW charger. ON Semiconductor has developed a series of power modules with excellent electrical and thermal performance to enable high efficiency chargers with high power density. In this Application Note, we demonstrate detailed OBC design and analysis with the use of two such power modules (FAM65CR51DZ1 PFC and FAM65HR51DS1 H−Bridge). Through detailed circuit simulation, we demonstrate the performance of these modules in the on−board charger system.

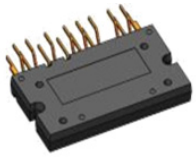
INTRODUCTION TO OBC

Figure 1 shows the common package used for both the FAM65CR51DZ1 and FAM65HR51DS1 modules, and Figure 2 illustrates the block diagram of the typical OBC system. The PFC block is composed of AC power grid (85−265 Vac) input, input filter, bridge rectifier and boost converter. The DC/DC converter block includes two−phase H−bridge, LLC tank, isolation transformer, output bridge rectifier, and output filter.

PFC Block in General

The PFC block draws AC input current that is in phase with the AC input voltage to maximize the power factor (PF) and minimize grid harmonic distortion. In the ideal case, the power factor is maintained at unity without harmonic distortion. With typical control, the PFC stage can hold 0.97 > PF > 1.0 for the OBC system.

(a) Bottom View



(b) Top View (Y−Form)

(c) Top View (L−Form)

Figure 1. FAM65CR51DZ1 Module

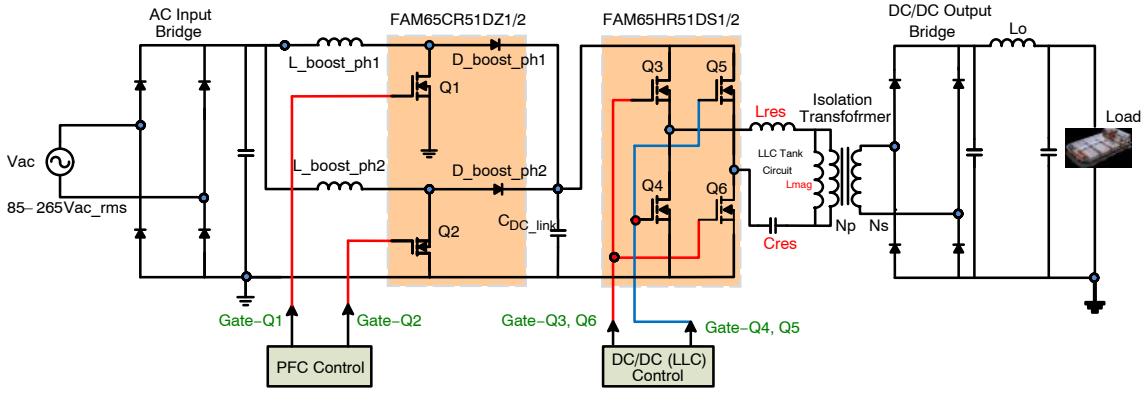


Figure 2. Typical OBC System Block Diagram

The PFC circuit can be designed to operate in continuous current mode (CCM) or critical current mode (CRM) based on the inductor current waveform in the boost converter circuit. In high power applications such as the OBC for EVs, the CCM topology is commonly used to minimize the current ripple and maximize the system efficiency. In the CCM PFC, the switch (MOSFET) in the boost converter has a fixed switching frequency with variable duty cycle (on−time), whereas the CRM PFC has variable switching frequency with fixed on−time. This characteristic of CRM makes the design of the PFC components more complicated, requiring a dedicated input EMI filter circuit due to the high current ripple. Although the CRM PFC has an advantage in reduced switching losses owing to its zero current switching, this advantage is canceled by higher conduction losses than that of the CCM PFC. Since the CCM PFC has a fixed switching frequency, power factor is higher than CRM PFC, typically by 0.2% to 0.3% and this leads to higher PFC efficiency. Figure 3 shows the phase matching between input voltage and current in the lower grid where PF is 98%, and an example waveform of the inductor current in the boost converter operating in CCM PFC mode. By contrast, Figure 4 shows the inductor current in CRM PFC.

Figure 5 represents the currents in the two phase interleaved boost converter and Figure 6 shows the effect of interleaving in the CCM PFC circuit. In a two phase interleaved boost converter, the two inductor currents are out of phase by 180° and the ripple in each inductor current is cancelled partially at the summing node.

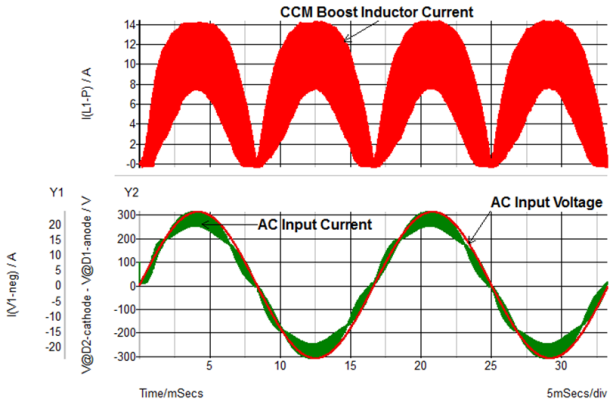


Figure 3. Phase Matching between Input Voltage and Current in a CCM PFC

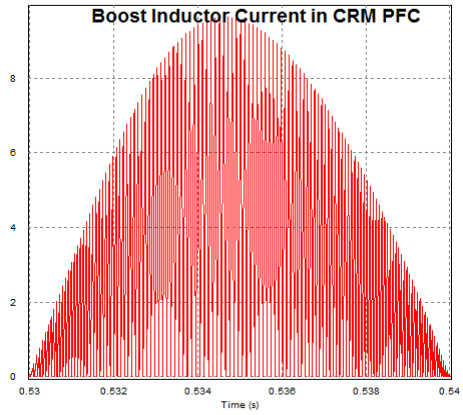


Figure 4. Boost Inductor Current in CRM PFC

In CCM PFC, duty cycle is continuously changing and maximum ripple reduction occurs when the duty cycle (D) is 0.5 as seen in Figure 7. Equation 1 below represents the current ripple reduction ratio, K(D), in a two−phase interleaved boost converter.

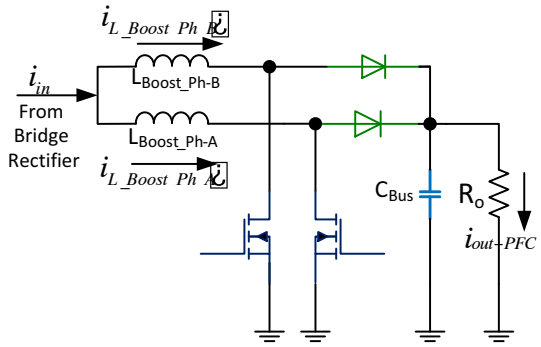


Figure 5. Two−phase Current Interleaving Circuit

$$K(D) = \frac{\Delta I_{interleaved}}{\Delta I_{L\_boost}} = \frac{1 - 2{\cdot}D}{1 - D},\ D < 0.5 \quad = \frac{2{\cdot}D - 1}{D},\ D \geq 0.5 \qquad \text{(eq. 1)}$$

Where:
ΔI_{L_boost}: Amplitude of the phase current ripple
$\Delta I_{interleaved}$: Amplitude of the phase current ripple

Also, interleaving can reduce the total boost inductor energy consumption. In a single phase boost converter, energy stored in the inductor is:

$$E_{L\_boost} = \frac{1}{2}Li^2 \qquad \text{(eq. 2)}$$

In a two phase interleaved boost converter, total inductor energy is

$$E_{L\_interleaved} = 2\cdot\left[\frac{1}{2}\cdot L\left(\frac{i}{2}\right)^2\right] = \frac{1}{4}Li^2 \qquad \text{(eq. 3)}$$

Therefore, interleaving brings a reduction in the size of the inductor and consequently reduced current ripple in the output capacitor.

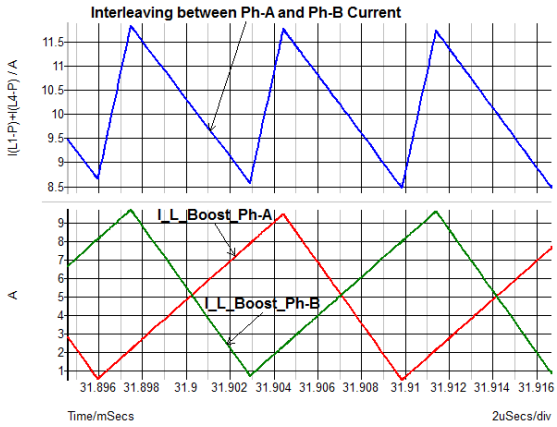


Figure 6. Current Ripple Reduction in Two−phase Interleaved Boost PFC Circuit

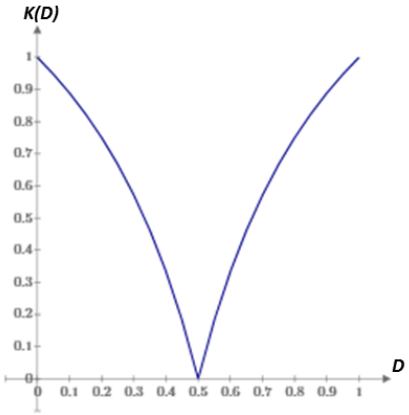


Figure 7. Ripple Reduction in PFC Boost Inductor Current by Interleaving (Ripple is Minimized at D = 0.5)

PFC Block Design Specification

Table 1 gives the design specification of 3.3 kW PFC circuit block and Figure 8 illustrates the PFC circuit block diagram including AC power grid, input rectifier bridge, and control circuit used in the PFC system simulation. The pre−charge circuit necessary to control in−rush current was not considered in the simulation.

Table 1. DESIGN SPECIFICATION OF PFC BLOCK

AC Input Voltage	85 – 265 V_{rms}, 50 – 60 Hz
PFC Output Voltage	390 – 400 V_{DC}
Rated Power	3.3 kW
Inductor Current Ripple	<25% @ Rated Power
Output Voltage Ripple	2% of Output at 120 Hz
Switching Frequency	65 kHz

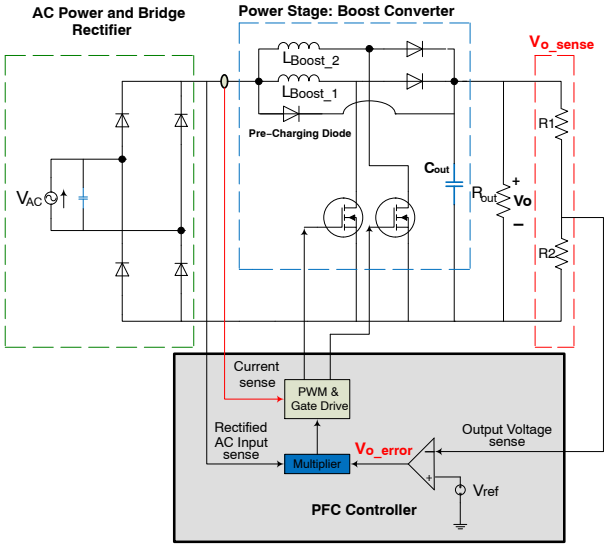


Figure 8. PFC Circuit Including Controller

Major Components in PFC Block

PFC Boost Inductor

The inductance of the boost inductor can be determined by the amount of current ripple and the switching frequency as below:

$$L_{boost} = \frac{1}{\%ripple}\cdot\frac{v_{ac\_min}^2}{P_{out}}\cdot\left(1 - \frac{\sqrt{2}\cdot v_{ac\_min}}{V_{out}}\right)\cdot\frac{1}{f_{sw}} \qquad \text{(eq. 4)}$$

By putting the design specifications (Table 1) into the Equation (2) above,

$$L_{boost} = \frac{1}{0.25}\cdot\frac{(85v_{rms})^2}{3300}\ W\cdot\left(1 - \frac{\sqrt{2}\cdot 85v_{rms}}{400\ V}\right)\cdot\frac{1}{65\cdot 10^3\ Hz}$$

$$= 130.3\ \mu H$$

In the simulation circuit, 150 μH inductor with 20 mΩ of ESR was applied.

Output Capacitor

The value of the output capacitor is determined by the PFC output voltage, the rated power of PFC and capacitor hold−up time. Suppose the PFC output voltage should not fall below 300 V during a single AC line cycle period (e.g., 16.7 msec for 60 Hz), the hold−up time, t_{hold} = 16.7 msec and V_{out_min} = 300 V. Assuming V_{out} = 400 V, the output capacitor size can be determined as below [1]:

$$C_{out} \geq \frac{2 \cdot P_{out\_max} \cdot t_{hold}}{V_{out}^2 - V_{out\_min}^2} = 1.575\ mF$$

In the simulation, a 2.0 mF capacitor with 10 nH ESL was applied.

Input Rectifier Diode

The bridge rectifier must be able to handle the AC input current peak defined as:

$$i_{in\_ac\_max} = \sqrt{2} \cdot \frac{P_{out\_max}}{\eta \cdot v_{ac\_min} \cdot PF} = \sqrt{2} \cdot \frac{3300W}{0.98 \cdot 85v_{rms} \cdot 0.98} = 40.4\ A$$

η = target PFC efficinecy

In the simulation, 1000 V − 80 A ON Semiconductor UltraFast diode model RURG80100 was applied, considering the necessary voltage margin.

Boost Converter MOSFET and diode

FAM65CR51DZ1 modules were developed specially for multi−phase interleaved boost converter operation, composed of a pair of MOSFET die and series−connected diodes to form a two−phase interleaved PFC circuit as shown in the Figure 9.

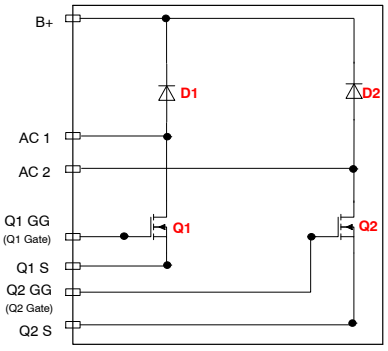


Figure 9. FAM65CR51DZ1 PFC Module Block Diagram

In the module, ON Semiconductor 3rd generation Super Junction (SJ) MOSFET die are used for the main boost converter switches. Two different sizes of the die (51 mΩ die and 80 mΩ) are available. Table 2 shows the electrical characteristics of the MOSFET die in FAM65CR51DZ1 module.

Since the PFC boost converter experiences hard switching, the MOSFET parameters should be optimized to have low switching loss along with low thermal impedance. As seen from Table 2, the 3rd generation of 650 V SJ MOSFETs have: 1) low Q_g that enables the fast switching, 2) small C_{oss} resulting in low switching loss, and 3) low thermal resistance compared to major competitor parts.

DC/DC (LLC) Converter in General

Figure 10 represents a DC/DC converter block in an electric vehicle OBC. The PFC output voltage is fed into the DC/DC converter input. This input waveform is not a pure DC signal, but includes 120 Hz AC ripple from the PFC block. The DC/DC converter modulates the input waveform to generate a square pulse waveform. Typically, the DC/DC converter has a half bridge or full bridge circuit with LLC resonant topology to minimize the switching loss by zero voltage switching (ZVS). The LLC tank circuit follows the DC switching block. The resonant tank circuit is named LLC because it is composed of resonant inductor, resonant capacitor and magnetizing inductance of the isolation transformer. The square waveform from the DC/DC switching block (full bridge or half bridge) becomes an "almost−sinusoidal" signal through the LLC tank circuit, which is transferred to the isolation transformer. The transformer isolates the primary switching block from the secondary load side to prevent the propagation of conductive EMI noise and protect against a short circuit on the load side.

Table 2. ELECTRICAL CHARACTERISTICS OF MOSFET DIE IN FAM65CR51DZ1 MODULE

Symbol	Parameter	Typical Value	Units
V_{DS} (Q1−Q2)	Drain to Source Voltage	650	V
V_{DS} (Q1−Q2)	Gate to Source Voltage	±20	V
I_D (Q1−Q2)	Drain Current Continuous (T_c = 25°C, V_{GS} = 10 V)	33	A
	Drain Current Continuous (T_c = 100°C, V_{GS} = 10 V)	23	A
BVDSS (Q1−Q2)	Drain to Source Breakdown Voltage	650	V
Coss	Output Capacitance (VDS = 400V, VGS = 0 V and fsw = 1 MHz)	100	pF
Qg	Total Gate Charge	126	nC
$R_{DS(ON)}$	ON−Resistance of the MOSFET die	51	mΩ
R_{θ_JC}	Junction to Case Thermal Resistance	0.66	°C/W
R_{θ_JS}	Junction to Heatsink Thermal Resistance	1.2	°C/W
T_J	Maximum Junction Temperature	−55 to 150	°C
T_C	Maximum Case Temperature	−40 to 125	°C
T_{STG}	Storage Temperature	−40 to 125	°C

Table 3. BOOST CONVERTER DIODE (ISL9R1560) CHARACTERISTICS

Symbol	Parameter	Typical Value	Units
V_{RRM}	Peak Repetitive Reverse Voltage	600	V
V_{RWM}	Working Peak Reverse Voltage	600	V
V_R	DC Blocking Voltage	600	V
$I_{F(AV)}$	Average Rectified Forward Current Tc = 25°C	15	A
I_{FSM}	Non−Repetitive Peak Surge Current (Half Wave 1 Phase 60 Hz)	45	A
I_{RR}	Reverse Recovery Current (I_F = 15 A, dI_F/dt = 200 A/μsec, VR = 390 V)	5.0	A
T_J	Maximum Junction Temperature	−55 to 175	°C
T_C	Maximum Case Temperature	−40 to 125	°C
T_{STG}	Storage Temperature	−40 to 125	°C
E_{AVL}	Avalanche Energy (1A, 40 mH)	20	mJ
Q_{RR}	Reverse Recovery Charge (I_F =15 A, dI_F/dt = 800 A/μsec, V_R = 390 V)	390	nC
T_{RR}	Reverse Recovery Time (I_F =15 A, dI_F/dt = 800 A/μsec, V_R = 390 V)	52	nsec
S	Softness Factor t_b/t_a (I_F = 15 A, dI_F/dt = 800 A/μsec, V_R = 390 V)	1.36	–
R_{θ_JC}	Junction to Case Thermal Resistance	1.98	°C/W
R_{θ_JS}	Junction to Heatsink Thermal Resistance	2.97	°C/W

In most cases, the turns−ratio of the transformer, N_{sec}/N_{pri} is higher than unity to operate across a wide range of output (battery) voltages. On the secondary side, the transformer output signal is rectified by the bridge rectifier circuit and finally becomes the DC power delivered to the HV battery.

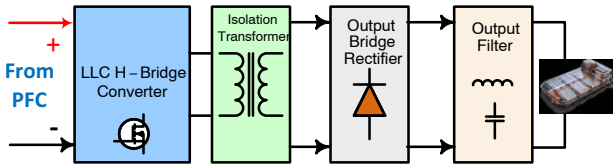


Figure 10. OBC DC/DC Converter Block Diagram

Figure 11 shows the full−bridge LLC converter circuit with current mode control. Input voltage is supplied from the PFC block between 390 V ~ 400 V. The output voltage is determined by the HV battery, typically 220 V~450 V. In the DC/DC converter stage, the largest portion of power loss is generated in the MOSFET switches and reduction of switching loss of the MOSFET is a critical factor in a converter design. As the size of the die increases, conduction loss decreases with lower $R_{DS(ON)}$ value, but at the same time, increased switching loss reduces the benefit of using large die. Using smaller die can bring reduced switching loss but increases conduction loss, and may produce higher junction temperature due to the higher thermal impedance. For those reasons, applying larger MOSFET die in the LLC topology is justified owing to the zero voltage switching (ZVS) during the turn−on switching transient. Currently, LLC converter topology is the most viable choice to use the ZVS characteristics.

In a conventional full−bridge converter, the two diagonal MOSFETs form a switching pair sharing the same gate drive signal with duty cycle of 50%. The two pairs have 180° phase difference. As an alternative, the phase−shifted full bridge topology can be implemented without the LC resonant tank circuit, enabling natural ZVS through the free−wheeling of the body diode, and control is also simpler than that of the LLC topology. However, in the OBC application, system efficiency is critical and excessive power loss from the body diode free−wheeling becomes a hurdle to achieve the target efficiency. Therefore, the phase−shifted full bridge topology is in general not used for OBC systems, but is mainly used in HV to LV DC/DC converters where efficiency is not the highest priority.

In terms of control, either the peak current mode control or average current mode control method may be used to set the charging current in accordance with the HV battery charging state. Here, the DC/DC converter control method will not be discussed further. In this application note, LLC full bridge converter circuit with average current mode control is implemented to evaluate the performance of the FAM65HR51DS1full−bridge module, including switching behavior, power loss, and efficiency.

LLC Resonant Tank Circuit Analysis

Figure 12 shows the simplified LLC resonant converter circuit and equivalent secondary side signal processing block diagram. The LLC resonant tank circuit is composed of resonant inductor, L_r, resonant capacitor, C_r and the transformer magnetizing inductance, L_{mag}. As seen from Figure 12(a), the input voltage of the LLC resonant circuit is a squarewave alternating between the positive and negative value of DC input voltage of the full−bridge converter block. Assuming only the fundamental frequency component of the input voltage is used to transfer energy from the primary side to the secondary side of the isolation transformer, the First Harmonic Approximation (FHA) method can be applied to perform the analysis of an LLC resonant circuit avoiding complex analytical method [4].

In Figure 12(b), the primary side is replaced by an AC current source model. Since the average value of $|i_{ac}(t)|$ is equal to the DC output current, I_o, $i_{ac}(t)$ can be represented as in equation (5).

$$i_{ac}(t) = \frac{\pi \cdot I_0}{2} \sin(2\pi f_{sw} t) \qquad \text{(eq. 5)}$$

Using the FHA method, $v_{ac}(t)$ can be approximated by the fundamental component of the squarewave $V_P(t)$ as the Equation (6).

$$\begin{aligned} V_P(t) &= V_0 : \text{if } \sin(2\pi f_{sw} t) \geq 0 \\ V_P(t) &= -V_0 : \text{if } \sin(2\pi f_{sw} t) < 0 \end{aligned} \qquad \text{(eq. 6)}$$

Therefore,

$$v_{ac}(t) = V_{P\_f0}(t) = \frac{4V_0}{\pi} \sin(2\pi f_{sw} t)$$

where (eq. 7)

$V_{P\_f0}(t)$ = Fundamental frequency conponent of $V_P(t)$

The ac equivalent resistance, r_{ac}, can be obtained using $i_{ac}(t)$ and $v_{ac}(t)$.

$$r_{ac} = \frac{v_{ac}(t)}{i_{ac}(t)} \cdot \frac{8}{\pi^2} \cdot \frac{V_0}{I_0} = \frac{8}{\pi^2} R_0 \qquad \text{(eq. 8)}$$

Considering the transformer turns ratio $n = N_{pri}/N_{sec}$, the actual AC equivalent load resistance seen from the primary side is given by Equation 9.

$$r_{ac} = \frac{8 \cdot n^2}{\pi^2} R_0 \qquad \text{(eq. 9)}$$

Using this AC equivalent resistance, the AC equivalent circuit for the entire LLC converter can be obtained as illustrated in Figure 13.

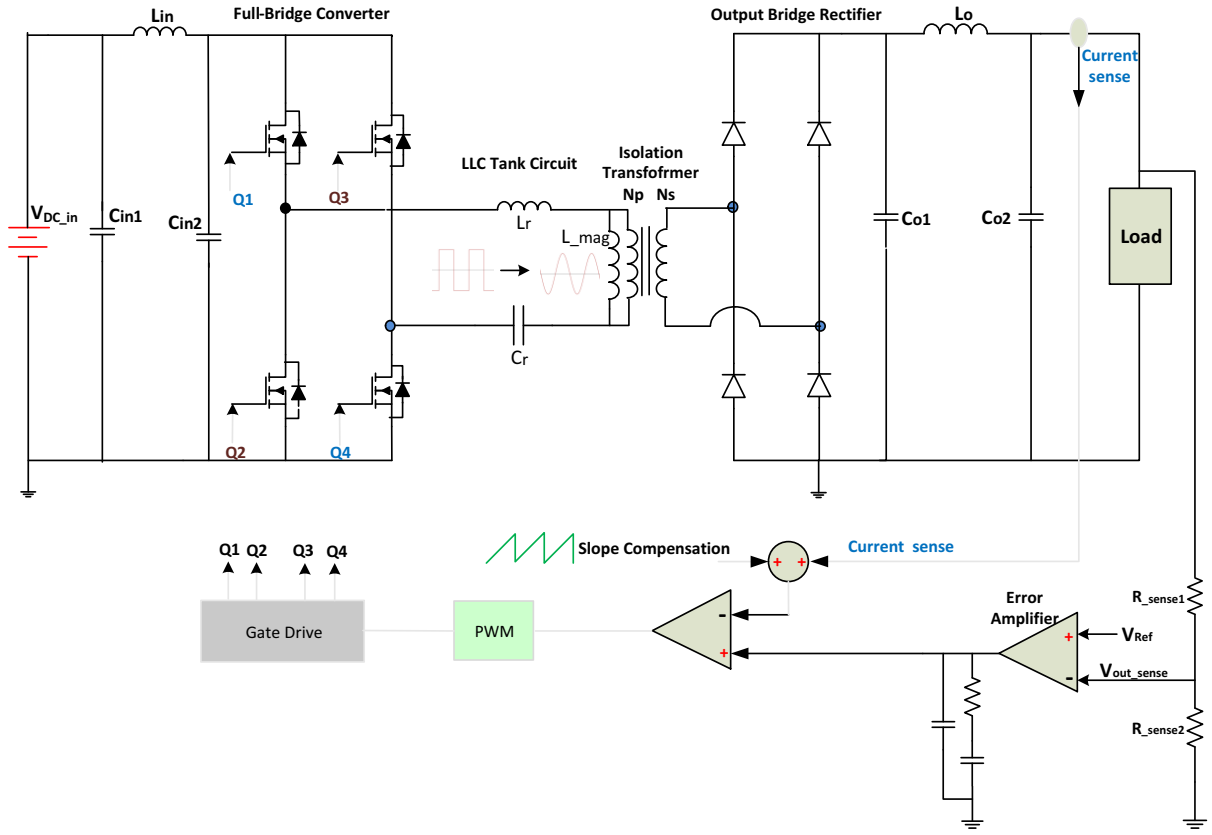


Figure 11. Full−Bridge LLC Converter Circuit with Current Mode Control

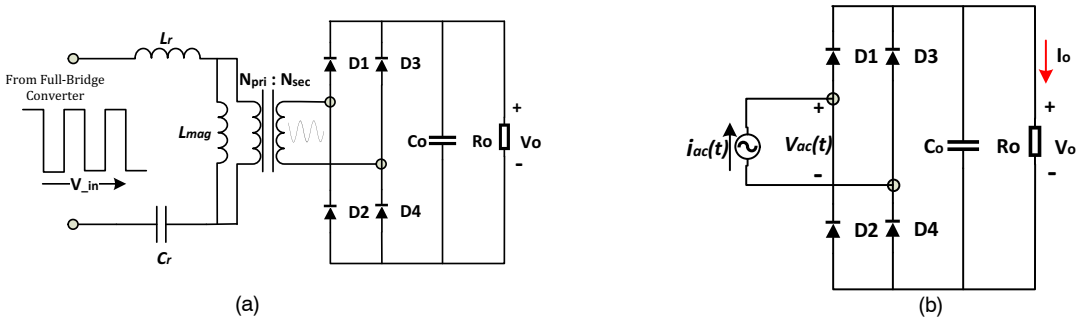


Figure 12. (a) Simplified LLC Circuit and (b) Equivalent Model Replacing Primary Side with AC Current Source

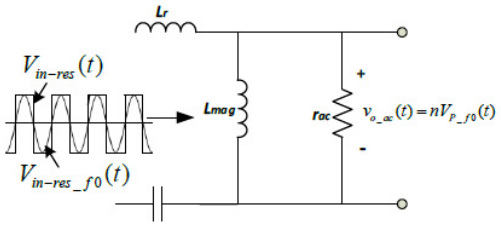


Figure 13. AC Equivalent Circuit for LLC Resonant Converter

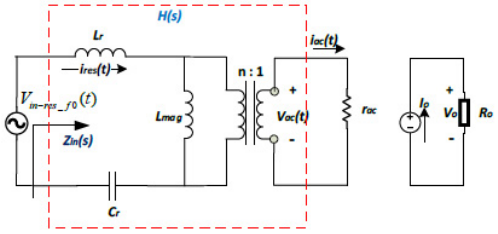


Figure 14. Two Port Network Model of FHA Resonant Circuit

The quality factor, Q, of the resonant tank circuit in Figure 13 is defined as given in Equation (10).

$$Q = \frac{\sqrt{L_r/V_r}}{n^2 \cdot R_0} = \frac{r_{ac}}{n^2 \cdot R_0}$$

where

$$n = \frac{N_{pri}}{N_{sec}}$$

$$r_{ac} = \frac{8}{\pi^2} \cdot \frac{N_{pri}^2}{N_{sec}^2} \cdot R_0$$

$$R_0 = \frac{V_0}{I_0} \quad \text{(eq. 10)}$$

The resonant tank gain is the magnitude of the transfer function of the AC equivalent circuit and defined as in Equation 11.

$$M = \frac{V_{o\_ac}(t)}{V_{in-res\_f0}(t)} = \frac{nV_{P\_f0}(t)}{V_{in-res\_f0}(t)} = \frac{4}{\pi} V_0 \cdot \frac{\sin(2\pi f_{sw} t)}{\frac{2}{\pi} V_{in} \cdot \sin(2\pi f_{sw} t)} = \frac{2n \cdot V_0}{V_{in}} \quad \text{(eq. 11)}$$

Alternatively, the LLC resonant tank circuit can be defined by its transfer function H(s) and input impedance $Z_{in}(s)$ using a two port network model as shown in Figure 14.

$$H(s) = \frac{V_{ac}(s)}{V_{in-res\_f0}(s)} = \frac{1}{n} \cdot \frac{n^2 \cdot r_{ac} \parallel sL_{mag}}{Z_{in}(s)}$$

where (eq. 12)

$$Z_{in}(s) = \frac{V_{in-res\_f0}(s)}{I_{res}(s)} = \frac{1}{sC_r} + sL_r + n^2 r_{ac} \parallel sL_{mag}$$

In Equation 12, the term, $n^2 \cdot r_{ac}$ is the effective resistive load reflected to the primary side of the transformer.

The term "Normalized Voltage Conversion Ratio" or "Voltage Gain" $M(f_{sw})$ is defined as:

$$M(f_{sw}) = n \cdot \| H(j2\pi F_{sw}) \| = n \cdot \frac{v_{ac}(t)|_{rms}}{V_{in-res\_f0}(t)|_{rms}} = n \cdot \frac{\frac{2\sqrt{2}}{\pi} V_0}{\frac{\sqrt{2}}{\pi} V_{in}} = \frac{2n \cdot V_0}{V_{in}} \quad \text{(eq. 13)}$$

From Equation 13, the input−to−output DC/DC voltage conversion ratio becomes:

$$\frac{V_0}{V_{in}} = \frac{1}{2n} M(f_{sw}) \quad \text{(eq. 14)}$$

After some comprehensive work using the Equations 10−14, the voltage gain can be described as a function of the quality factor Q, inductance ratio ($m = L_r/L_{mag}$) and normalized frequency, f_1 as shown in Equation 15. [2] [4]

$$M(Q, m, f_1) = \frac{f_1^2 \cdot (m-1)}{\sqrt{(m \cdot f_1^2 - 1) + f_1^2 \cdot (f_1^2 - 1)^2 \cdot (m-1)^2 \cdot Q^2}} \quad \text{(eq. 15)}$$

Table 4 shows an example of the design parameters in an LLC converter. These parameters are applied in our 3.3 kW LLC converter demonstration hardware and the corresponding simulation work.

Table 4. DESIGN PARAMETERS FOR 3.3 kW LLC FULL−BRIDGE CONVERTER

Component	Designation	Value
Converter DC Input Voltage	V_{in_DC}	390−400 V
Converter DC Output Voltage	V_{out_DC}	250−450 V
Switching Frequency	f_{sw}	100−150 kHz
Resonant Frequency	f_{res}	100 kHz
Resonant Inductor	L_r	25 μH
Resonant Capacitor	C_r	100 nF
Magnetizing Inductance	L_{mag}	125 μH
Transformer Turns Ratio	$n = N_{pri} / N_{sec}$	0.8
Inductance Ratio	$m = L_{mag} / L_r$	5
Normalized Frequency	$f1 = f_{sw} / f_{res}$	1 – 1.55

In the LLC converter circuit designed according to Table 4, Q varies from 2.217 to 0.629 as the output load varies. Figure 15 shows the LLC converter gain variation with the change in the output load. As the output load gets heavier, the peak gain point shifts closer to to the resonant point and the peak gain approaches unity. Figure 16 illustrates the LLC gain characteristics at the 3.3 kW load point. In the figure, the power transfer operation is divided into two regions: ZVS Region 1 and ZVS Region 2. During the power transfer operation ($I\_L_r > I\_L_{mag}$), the magnetizing inductor is being charged and it does not participate in the resonance operation. In this power transfer mode, the resonant frequency, f_{res} is defined as:

$$f_{res\_0} = \frac{1}{2\pi \sqrt{L_r \cdot Cr}} \quad \text{(eq. 16)}$$

ZVS is accomplished in both Region 1 and Region 2. In Region 2, the switching frequency is lower than the resonant frequency and the converter gain is higher than unity. Therefore, the converter is operated in boost mode. In Region 1, the LLC converter is working in buck mode. The switching frequency is higher than the resonant frequency, and the LLC gain is lower than the unity.

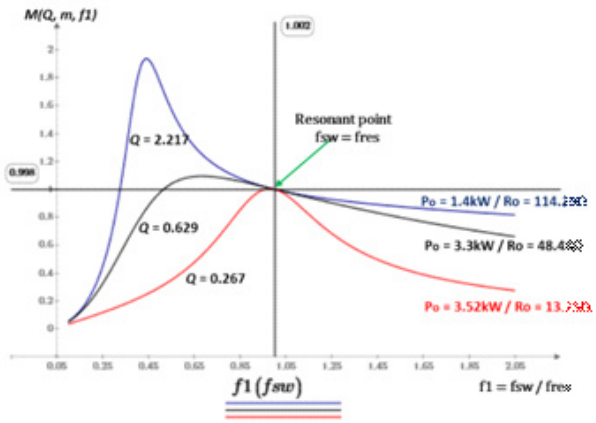


Figure 15. LLC Converter Gain Variation in Accordance with the Load Shift

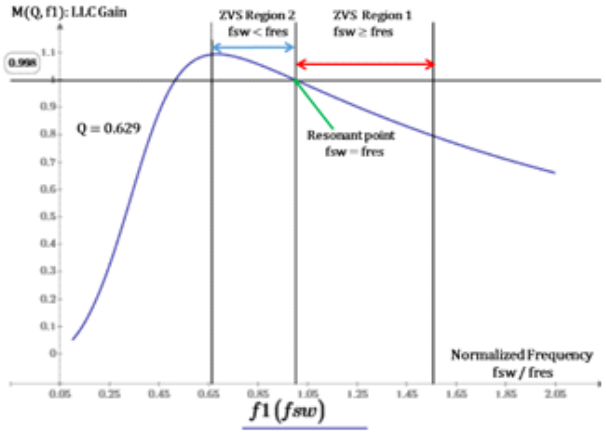


Figure 16. LLC Converter Gain Variation in Accordance with the Load Shift

The two ZVS operating regions are explained in detail below.

ZVS Region 1

Figure 17 shows the typical waveforms in the LLC converter operating in the ZVS Region 1. In this region, the switching frequency f_{sw} is set higher than the resonant frequency, f_{res}, and power is transferred from the primary side to the secondary side of the transformer until the end of each switching period. The magnetizing inductor current, I_L_{mag} is a part of the resonant inductor current, I_L_r and just charges the magnetizing inductor, L_{mag}. Therefore, L_{mag} is not involved in the resonant operation. The primary side transformer current, $I\_TXR\_Pri = I\_L_r - I\_L_{mag}$ is delivered to the secondary side. At the end of power delivery operation, I_L_r changes its direction (di/dt becomes negative) and returns back to the body diode of the MOSFET in the other phase leg to achieve ZVS turn−on.

The gate drive signal is applied at some point in this period as seen from Figure 18. One thing to observe is that as the switching period $T_s = 1/f_{sw}$ ends before the resonant current completes its own period, $T_r = 1/f_{res}$, the MOSFET has a hard−switched turn−off and the secondary side rectifier diodes experience hard commutation as seen in Figure 19. By design optimization of the LLC tank circuit, turn−off transient current of the MOSFET can be minimized, resulting in near zero current switching condition (ZCS).

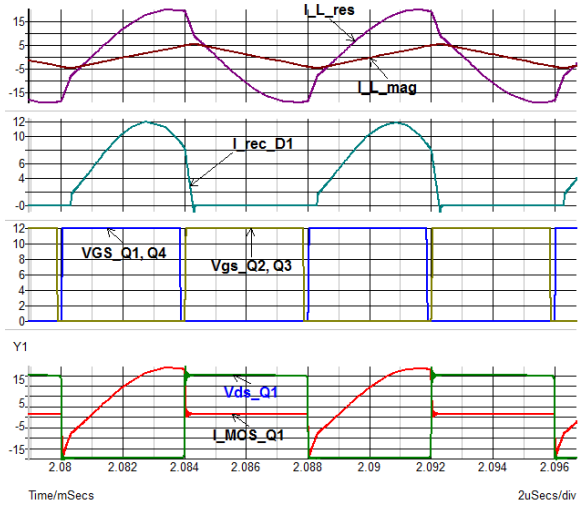


Figure 17. Typical Waveforms in LLC Full−Bridge Converter (f_{sw} = 125 kHz, f_{res} = 100 kHz)

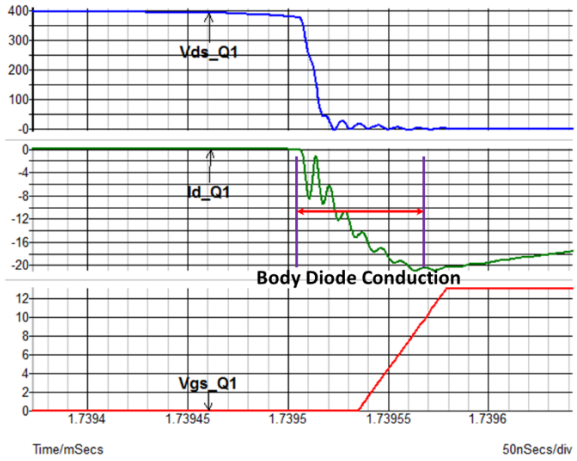


Figure 18. ZVS Operation: Gate Drive Signal is Engaged during the Body Diode Conduction ($V_{DS} \approx 0$ V)

ZVS Region 2

Figure 20 shows the LLC converter waveforms in ZVS region 2. In this region, the switching frequency f_{sw} is lower than the resonant frequency and each switching period includes the freewheeling period T_{fw} and, in this region, $I\_L_{mag} \approx I\_L_r$. In this period, resonant operation includes discharging of the magnetizing inductance and the resonant current returns back to the converter since the MOSFET channel is still open. During the freewheeling operation, the power in the primary side of the transformer is not transferred to the secondary side and generates additional conduction loss in the MOSFET. In this period, a second resonant frequency, f_{res_1} is defined as given in Equation 17.

$$f_{res\_1} = \frac{1}{2\pi\sqrt{(L_r + L_{mag})\cdot Cr}} \quad \text{(eq. 17)}$$

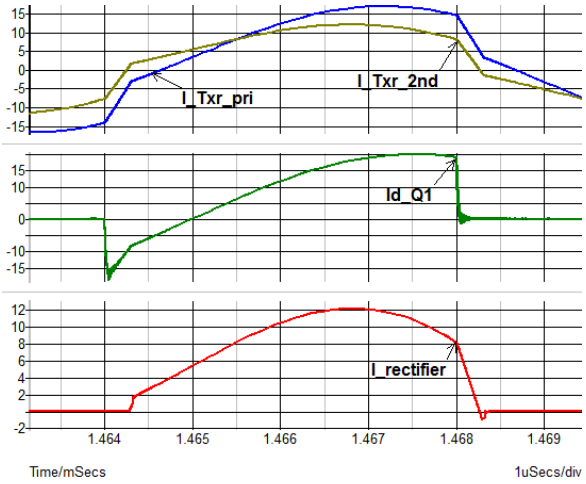


Figure 19. Secondary side rectifier diode hard commutation during the MOSFET turn−off transient

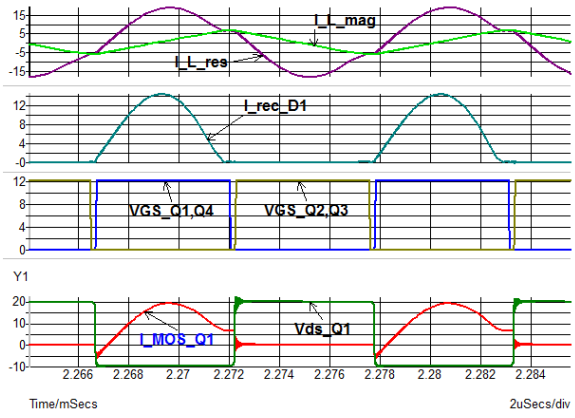


Figure 20. Secondary Side Rectifier Diode Hard Commutation During the MOSFET Turn−off Transient

MOSFET Module for the LLC Converter

Figure 21 shows the circuit diagram and pin−out configration of ON Semiconductor's FAM65HR51DS1 H−bridge module. The module was specifically designed for a full−bridge LLC DC/DC on−board charger (OBC). Each half−bridge is composed of two series connected MOSFET die (totem pole). The MOSFET die in the FAM65HR51DS1 module are identical with the ones used in the FAM65CR51DZ1 module and, likewise, two different sizes of die (51 mΩ and 82 mΩ) are available. The module has a high voltage snubber capacitor across the DC link for noise suppression and is qualified per AECQ101 and conforms to AQG324 guidelines. In the LLC converter application, MOSFET turn−off switching loss is dominant compared to the conduction loss. The simulation results for the 3.3 kW OBC system show that the 82 mΩ (smaller) die gives a bit higher efficiency than 51 mΩ die due to the smaller switching loss. But, certainly the 51 mΩ die has better thermal performance due to the lower thermal resistance. Tables 5 and 6 represent the electrical specifications and electrical characteristics of the 51 mΩ MOSFET die applied in FAM65HR51DS1 module.

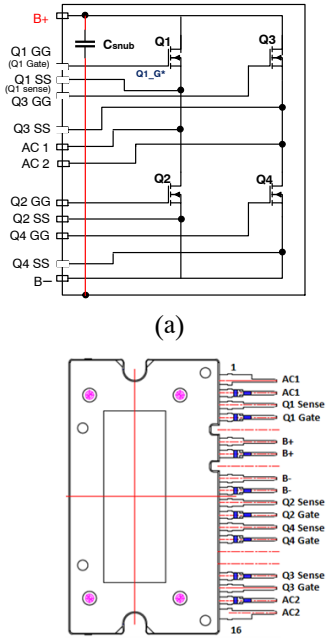


Figure 21. FAM65HR51DS1 H−bridge Module (a) Circuit Diagram and (b) Pin−out Definition

OBC SIMULATION USING FAM65CR51DZ1 AND FAM65HR51DS1 PSPICE SIMULATION MODEL

The 3.3 kW on−board charger described has been simulated to project the performance of the FAM65CR51DZ1 PFC module and the FAM65HR51DS1 H−bridge module at several operating points, including the worst case (P_{out} = 3.52 kW, V_{out} = 220 V, I_{out} = 16 A, T_{case} = 110°C). The two−phase interleaved boost PFC topology and LLC full−bridge converter topology were applied in this system simulation as well as in bench test experiments. SIMETRIX v8.1 was used as the simulation platform. Ansys Q3D−based pSpice parasitic package model and the MOSFET die model were used to simulate both FAM65CR51DZ1 and FAM65HR51DS1 modules.

The power loss of the two modules and the major components in the OBC system were estimated through simulation and system efficiency was calculated based on these component power losses. AC input power source, bridge rectifier circuit, and the boost PFC circuit were combined into the PFC simulation block. The LLC full−bridge converter, isolation transformer, secondary side bridge rectifier and output filter circuit forms the separate DC/DC converter simulation block. The OBC system efficiency is obtained by multiplying the efficiency of the PFC block by the DC/DC converter block efficiency. Through the simulation, the junction temperature, T_J, was assumed 90°C in the normal case and 110°C in the worst case simulation.

Finally, the performance of FAM65CR51DZ1 and FAM65HR51DS1 modules were compared to those of discrete MOSFETs by applying them in the same circuit used in the module simulation. The simulation results reveal that the OBC with FAM65CR51DZ1 and FAM65HR51DS1 modules has higher system efficiency than the OBC with discrete MOSFET devices due to lower switching loss of the module.

Table 5. ELECTRICAL SPECIFICATION FOR THE 51 mΩ SJ MOSFET DIE IN FAM65HR51DS1 MODULE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	650	–	–	V
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 3.3 mA	3.0	–	5.0	V
$R_{DS(ON)}$	Q1 – Q4 MOSFET On Resistance	V_{GS} = 10V,I_D = 20A	–	44	51	mΩ
$R_{DS(ON)}$	Q1 – Q4 MOSFET On Resistance	V_{GS} = 10 V, I_D = 20 A, T_J = 150°C	–	79	–	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 20 A	–	30	–	s
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	−100	–	+100	nA
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 650 V, V_{GS} = 0 V	–	–	10	μA

Table 6. ELECTRICAL CHARACTERISTICS FOR THE SF3 51mΩ MOSFET DIE IN FAM65HR51DS1 MODULE

Symbol	Parameters	Conditions	Min	Typ.	Max	Unit
C_{iss}	Input Capacitance	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz	–	4864	–	pF
C_{oss}	Output Capacitance		–	109	–	pF
C_{rss}	Reverse Transfer Capacitance		–	16	–	pF
$C_{oss(eff)}$	Effective Output Capacitance	V_{DS} = 0 to 520 V V_{GS} = 0 V	–	652	–	pF
R_g	Gate Resistance	f = 1 MHz	–	2	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{DS} = 380 V I_D = 20 A V_{GS} = 0 to 10 V	–	123	–	nC
Q_{gs}	Gate to Source Gate Charge		–	37.5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	49	–	nC

Note, this page is held separate so that the remainder of the formatting will remain the same. If these two tables don’t make up most of a page, more formatting will need to be done.

Simulation Software

Simetrix v.8.1 software was used to estimate the power loss of the major components in 3.3 kW OBC system and the resulting OBC system efficiency. Simetrix is a non−linear mixed−signal circuit simulator. The software is based on the SPice programing language developed by the CAD/IC group of UC Berkeley and the XSPice from CS & IT Laboratory at the Georgia Institute of Technology.

The software features: 1) fully integrated hierarchical schematic editor, simulator graphical post−processor, 2) fast convergence for both DC transient analysis, 3) support for BSIM3 & BSIM4, 4) Monte Carlo analysis including tolerance specification, 5) easy SPice model importing 6) various measurement probe functions including voltage, current and device power. Simetrix includes the Simplis simulator, which achieves much faster simulation speed than Simetrix in a switching circuit simulation. Simplis characterizes the complete system as a cyclical sequence of linear circuit topologies to accomplish this. Simplis gives fast and reliable results in a linear steady state analysis or AC analysis. However, given that the non−linear behavior of the switching MOSFET and diode is the critical factor to be analyzed, Simetrix is the right tool for the transient analysis of the power converter circuit. Even though Simetrix is used as the main tool for the OBC system simulation, the model importing process for Cadence PSpice is also described in the section Package Simulation Model for FAM65CR51DZ1 and FAM65HR51DS1 Modules since PSpice is a popular alternative to Simetrix. Cadence PSpice is frequently used for the device level simulation and Simetrix is favored in a system level circuit simulation. The Ansys Q3D−based parasitic package model can be imported into either PSpice or Simetrix without any modification in accordance with a user's preferred simulation platform.

Package Simulation Model for FAM65CR51DZ1 and FAM65HR51DS1 Modules

Figure 22 shows an example of 3D image of the physical connections between the device in a module (source) and outer pins (sink). Ansys Q3D analyzes the module structure in 3D space and extracts the R, L and C parasitic components between all the sink and source nodes. Table 7 shows an example of Q3D−based parasitic R and L values computed for the module. Once a source file (netlist) is created based on the Q3D analysis result, the circuit simulation tool imports the sorce file and generates the package simulation model as shown in Figure 23(a).

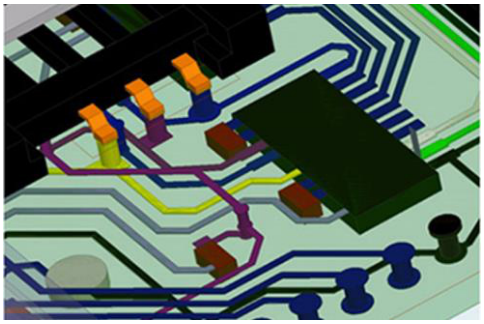


Figure 22. An example of Q3D image to extract the parasitic R, L and C components

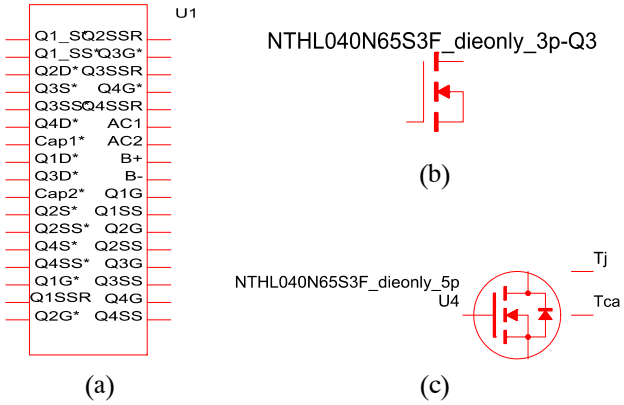


Figure 23. (a) Q3D−extracted FAM65CR51DZ1 and FAM65HR51DS1 Parasitic Package Model, (b) 3−pin Electrical Spice Simulation Model, and 5−pin Electro−thermal Spice Simulation Model

The FAM65CR51DZ1 and FAM65HR51DS1 module package model netlists are written in SPice programing language. The source files are compiled by the various simulation software tools and they create their own representation of the package models. The source file of the package simulation model has either ".LIB" or ".TXT" type of file extension. Cadence PSpice uses typically ".LIB" file extension whereas Ansys Simplorer and Simetrix uses both types of the file extension. Next, Cadence PSpice and Simetrix step−by−step instructions are given to explain how to create the simulation model from the original source file of the Q3D package model.

Table 7. FAM65HR51DS1 CAA PARASITIC R, L C VALUES EXTRACTED FROM ANSYS Q3D ANALYSIS (VALUES ARE EMBEDDED IN THE Q3D PACKAGE SIMULATION MODEL)

Sink	Source	DC Resistance	AC Inductance @20 KHz	Capacitance, pF
AC1	SRC_Q1S	1.1616	12.922	80.734
	SRC_Q2D	0.62705	14.579	
AC2	SRC_Q3S	1.1912	13.133	80.013
	SRC_Q4D	0.62058	14.921	
BM	SRC_Cap2	0.56135	10.968	67.536
	SRC_Q2S	1.0246	14.257	
	SRC_Q4S	1.0501	15	
BP	SRC_Cap1	0.41802	8.0862	94.311
	SRC_Q1D	0.41016	7.2403	
	SRC_Q3D	0.67266	13.103	
Q1_Gate	SRC_Q1G	3.1784	8.7028	2.3192
Q1_Sense	SRC_Q1SS	3.6118	8.792	2.4423
Q2_Gate	SRC_Q2G	13.651	23.466	4.7489
Q2_Sense	SRC_Q2SS	11.722	19.889	5.4937
Q3_Gate	SRC_Q3G	4.6801	9.4025	2.5984
Q3_Sense	SRC_Q3SS	4.2057	10	2.5047
Q4_Gate	SRC_Q4G	10.811	22.332	6.0436
Q4_Sense	SRC_Q4SS	10.558	18.639	5.3266

Cadence PSpice

1. Open the Model Editor in the directory as [Cadence 17.x/Product Utilities/PSpice Utilities/Model Editor]
2. In Model Editor utility screen in Figure 24, open the ".LIB" simulation file by clicking "File"→ "Open"
3. In the Model List window, click each sub circuit file name; the file opens in the main window
4. Click File menu → Click Export to Part Library: sub window for part creation pops up → click "OK" in the sub window; file compilation starts and completes
5. Repeat the process 3) and 4) until all the sub circuit files are compiled
6. The PSpice simulation model for FAM65CR51DZ1 and FAM65HR51DS1 package will be created in the Capture part library as shown Figure 23(a). The symbol file having file extension, ".OLB" will be created in the same directory where the original ".LIB" file exists
7. Include the created ".OLB" file in the PSpice library window using "Add Library" function in PSpice main simulation window as Figure 25
8. If ".OLB" is already available along with original ".LIB" file, it means that the original ".LIB" file was already compiled successfully. You can skip the above process and directly go to the process 7)

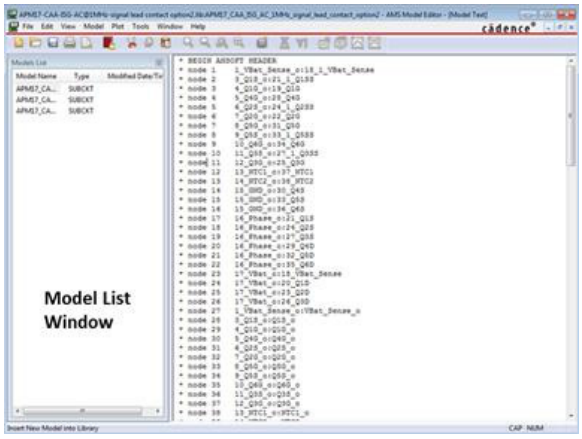


Figure 24. Model Editor Window is Divided into Model List sub−window and Main Program Window

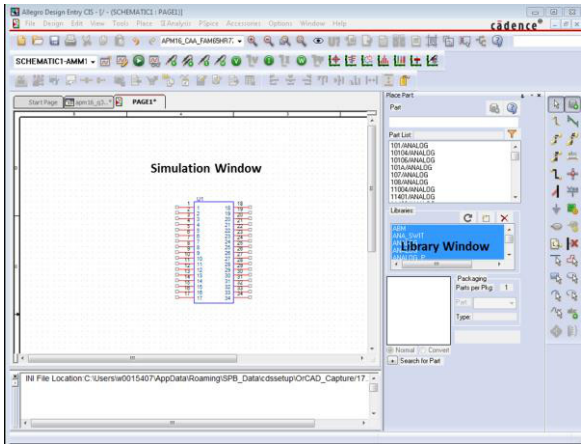


Figure 25. pSpice Main Simulation Window and Library Window

SIMETRIX

1. Simetrix software uses either ".LIB" type or ".TXT" type of model file
2. Open the main Simetrix and drag and drop the model file into the commend shell window in Figure 26 and then the sub−window appears asking to install the simulation model
3. Click "OK" in the sub−window, then the simulation model symbol is generated as seen in Figure 23(a)
4. You can find the package simulation model in "All user Models" window from the "Place menu" (Place → From Model Library → All user Models)

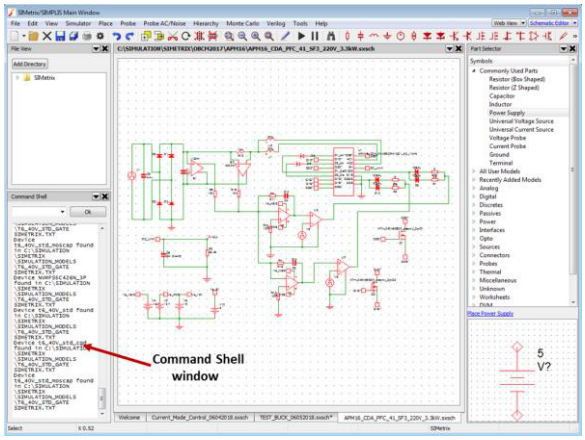


Figure 26. Main Screen of Simetrix Simulation

Figure 27 shows the FAM65HR51DS1 H−Bridge module schematic diagram and corresponding PSpice package simulation model extracted from Ansys Q3D. The Spice package model includes all the parasitic R, L, and C components between the sink nodes (actual module pin−out) and the source nodes (internal circuit components). Since the package model does not include the MOSFET dies, the die−only model for individual MOSFET should be connected externally as shown in Figure 30 and Figure 31. Therefore, a die−only model is required along with a package model in order to run the simulation. Two types of die−only model can be chosen based on the purpose of a simulation. For an electrical performance evaluation, a three−pin electrical model is used and for an electro−thermal simulation, the five pin electro−thermal model is used. Two different types of thermal simulations are possible. The first type is to estimate the junction temperature when the case temperature is set to a fixed point as shown in Figure 28. In this case, "T_{case}" port becomes the temperature input source and "T_J" port works as output port connected to a high resistance (1 MΩ) load, whose voltage potential represents junction temperature.

The second type of thermal simulation is to fix the junction temperature at a certain point and measure the performance of the MOSFETs including power loss and $R_{DS(on)}(T_J)$. In this case, a constant temperature source is connected to the T_J port and the T_{case} port is shorted to the T_J port as shown in Figure 29.

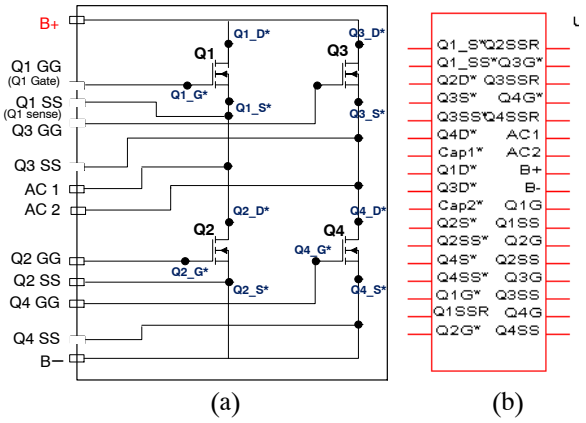


Figure 27. FAM65HR51DS1 H−Bridge (a) Schematic and (b) pSpice Package Model Pin−out

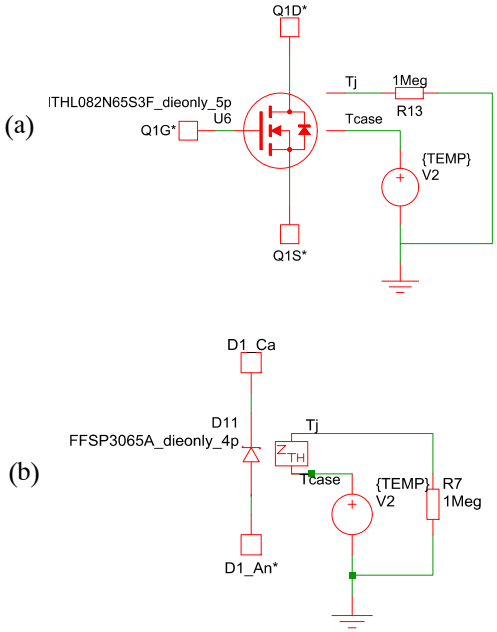


Figure 28. Connection of Electro−thermal Die−only Model to Measure (a) MOSFET and (b) DIODE Loss−dependent Junction Temperature, TJ

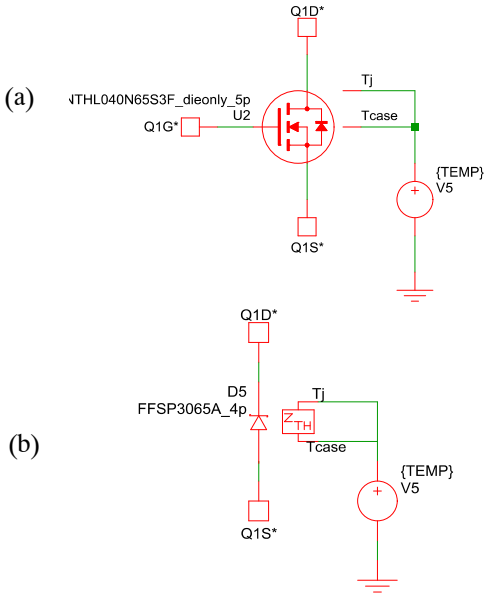


Figure 29. Connection of Electro−thermal Die−only Model to Measure the Performance of (a) MOSFET and (b) DIODE at Fixed TJ Condition

OBC System Simulation

Figure 30 shows the simulation circuit for LLC full−bridge converter using the Q3D−extracted Spice package model of FAM65HR51DS1 full−bridge module. The gate, drain and source connection points for each MOSFET are provided using the twelve outer pins of the package model and the four “die−only” MOSFET models are connected externally to represent the total FAM65HR51DS1 module. The values of parasitic R, L, and C components can be determined from Q3D analyses using a frequency sweep, depending on the application environment. Generally, the gate loop and power switching loop oscillations occur in the frequency range of 1to 20 MHz. Hence, a 1 MHz excitation signal is used to extract the parasitic inductance and capacitance values.

The analysis setup is very important in the electrical circuit simulation because the convergence, accuracy, and simulation speed are determined by this setup. In Simetrix, there are three critical parameters to specify: max/min time step, integration method and convergence option.

Table 8. SIMULATION CONDITIONS FOR PFC AND DC/DC (LLC) CONVERTER BLOCK

System Block	Vin_rms	T_j	Fsw	Vout	Iout	Pout
PFC	220 V	90°C	65 kHz	400 V_{DC}	3.5 A	1.4 kW
	110 V	90°C			4.5 A	1.8 kW
	220 V	90°C			6 A	2.4 kW
	220 V	90°C			8.25 A	3.3 kW
	220 V	110°C			8.8 A	3.52 kW
DC/DC Converter	400 V_{DC}	90°C	139 kHz	400 V_{DC}	3.5 A	1.4 kW
			154 kHz	360 V_{DC}	5 A	1.8 kW
			144 kHz	360 V_{DC}	6.7 A	2.4 kW
			141 kHz	400 V_{DC}	8.25 A	3.3 kW
		110°C	151 kHz	220 V_{DC}	16 A	3.52 kW
PFC Inductor	L = 150 μH, ESR = 20 mΩ					
Resonant L, C	L_resonant = 25 μH (ESR = 10 mΩ) C_resonant = 100 nF					
Transformer	L_Pri = 125 μH, ESR_Pri = 20 mΩ, ESR_sec = 30 mΩ					

1. Max/min time step defines the time resolution for the transient analysis. Users can adjust the time resolution directly using manual input or conveniently using the default setup. Since the default setup proceeds with the adaptive convergence method, it is convenient to use the default setup in normal transient analysis. In case of device characterization simulation, user should set up the time resolution based on reference material such as the datasheet of the device
2. In a transient analysis, the user can choose between trapezoidal integration method and gear integration method. In case of simulating a resonant circuit such as LLC converter, gear integration introduces a numerical damping effect that causes the resonant circuit to decay more rapidly than it should and for this reason, trapezoidal integration method should be selected for the transient analysis of the power converter circuits
3. Under the [Simulator] menu in the menu bar window, the user can choose various convergence options by clicking the [Convergence Options] sub−menu. For instance, when the message “No convergence in transient analysis” pops up, the user can change the iteration mode from the default [Normal Mode] to [Extended Precision] first, then [Advanced Iteration] or [Extended/quad precision]. These options improve the convergence at the expense of simulation speed without losing simulation accuracy. Also, there are additional convergence improvement options including [Absolute current tolerance] and [Circuit modifiers] options. [Convergence Options] menu window includes the explanation on the setting of those options

OBC System Simulation Condition

The simulations were carried out for the PFC block and DC/DC (LLC) converter block separately. In the simulation, the power losses of the components were measured in the steady state condition excluding the startup transient period. The efficiency of each function block was measured first and the total OBC system efficiency was obtained at each power level by multiplying the PFC block efficiency by the DC/DC converter efficiency. Because of the complexity of the simulation circuit of the PFC and DC/DC blocks, convergence problems could be encountered if both stages were simulated togeter. Table 8 represents the simulation condition for PFC and LLC converter circuits at each of the five operating points. Figures 30 and 31 illustrate respectively the simulation block diagram of the PFC and DC/DC with the parasitic package model and the die−only MOSFET models.

OBC システムのシミュレーション条件

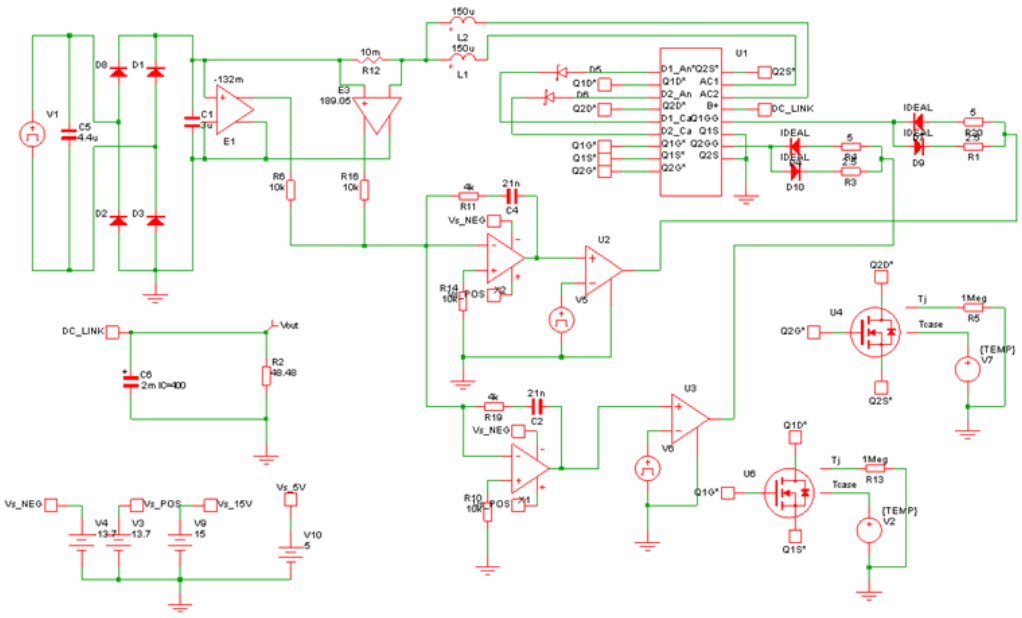


Figure 30. PFC Circuit Simulation Block Diagram using FAM65CR51DZ1 PFC Module and 5−pin Electro−thermal Die−only MOSFET Model: TJ was set to 90°C using External Temperature Source

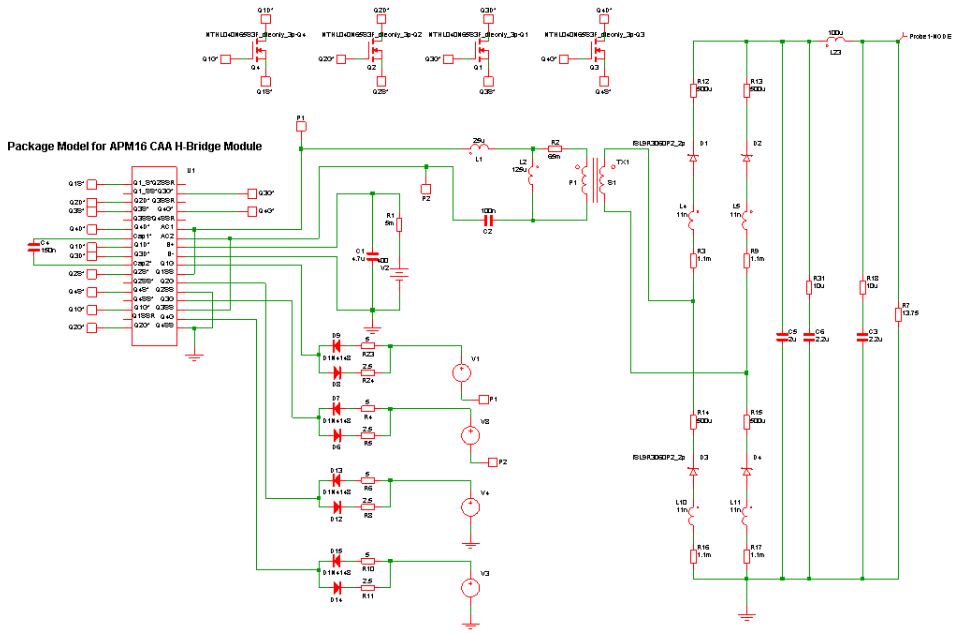


Figure 31. LLC Converter Circuit Simulation Block Diagram using FAM65HR51DS1 H−bridge Module and 3−pin Electrical Die−only MOSFET Model: Tj was set to 90°C in the Simulation Setup Option

System Simulation Results

Table 9 shows the OBC system simulation results. System efficiency was calculated based on Equation 18.

$$E_{OBC} = E_{PFC} \times E_{DC/DC} = \frac{P_{out\_PFC}}{P_{in\_PFC}} \times \frac{P_{out\_DC/DC}}{P_{in\_DC/DC}} \times 100\% \quad \text{(eq. 18)}$$

In the simulation, the performance of the FAM65CR51DZ1 and FAM65HR51DS1 modules was compared to that of discrete MOSFETs by comparing the individual power loss and the system efficiency. Figures 32 to 34 illustrate respectively the efficiency of the PFC, DC/DC, and the entire OBC system at each operating point.

Figure 34 implies that the OBC with module solution gives 95% or higher efficiency except at the worst case conditions. Comparing to the actual bench evaluation test result in Figure 35, the efficiency obtained from the simulation is very close to the bench evaluation data with the difference within ±0.2%. This validates the simulation data to be consistent and reliable.

Figures 36 and 37 show the power loss distribution in the PFC and DC/DC. The results reveal that the OBC with FAM65CR51DZ1 PFC module and FAM65HR51DS1 H−bridge module has clearly higher efficiency compared to the OBC with discrete SJ MOSFET devices due to the lower switching loss of the two modules. This lower switching loss is enabled by the lower parasitic inductance and resistance of the modules. Figure 36 indicates that the power loss of the AC input bridge dominates over all other components in the PFC block. Figure 32 shows that the efficiency of the PFC block is higher than 97.5% through the main operating range with 220 Vac input. Therefore, OBC system efficiency is mainly determined by the efficiency the DC/DC stage.

Figure 37 indicates that the power loss from the four MOSFETs in the full−bridge converter is the critical factor to determine the efficiency of the DC/DC. In the DC/DC stage, the power loss of the four MOSFETs accounts for 57% of the total power consumption. Also, Figures 36 and 37 suggest the designer should focus on reduction of power loss from the AC input bridge and MOSFET switching loss from DC/DC converter to increase the OBC efficiency. Implementation of the bridgeless PFC including a totem pole topology would be the most effective way to minimize the power loss from the AC input rectifier. In the DC/DC converter block, all the operating points are above the resonate point and consequently the majority of the MOSFET switching loss occurs during the turn−off transient, because turn−on loss is very low due to the ZVS operation. Ideally, ZCS can be achieved for the turn−off transient when the operating point is exactly on the resonant point. In this case, MOSFET turn−on loss would be minimized. As long as the operating point of the LLC converter is located above the resonant point, the hard−switched turn−off is inevitable and the design optimization of the converter block, including the transformer and the LLC resonant circuit, is necessary to reduce the turn−off switching loss.

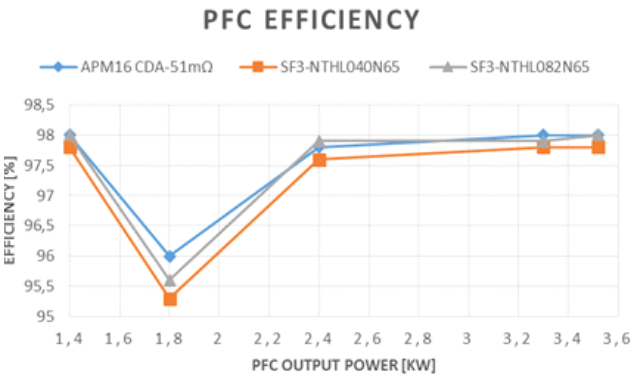


Figure 32. PFC Block Efficiency at each Operating Points: at 1.8 kW Power, Vac_in = 110 vrms (Worst Case) and Vac_in = 220 vrms at all other Points

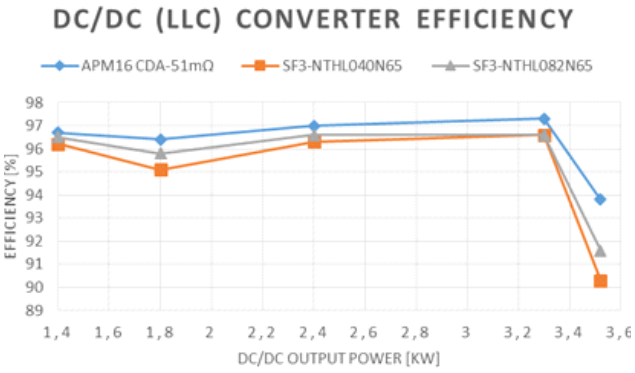


Figure 33. DC/DC (LLC) Converter Block Block Efficiency: at 3.52 kW, Vout = 220 V Iout = 16 A (Worst Case)

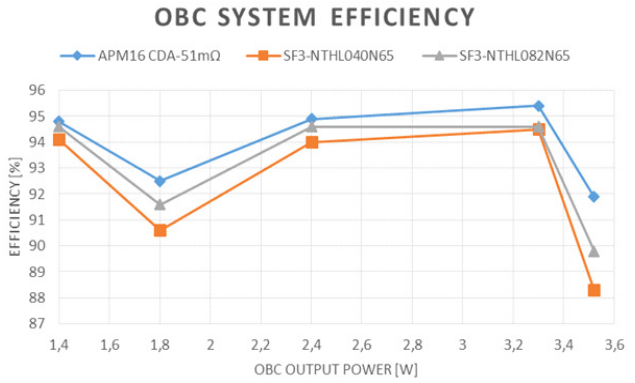


Figure 34. OBC System Efficiency with WCS at 1.8 kW and 3.52 kW

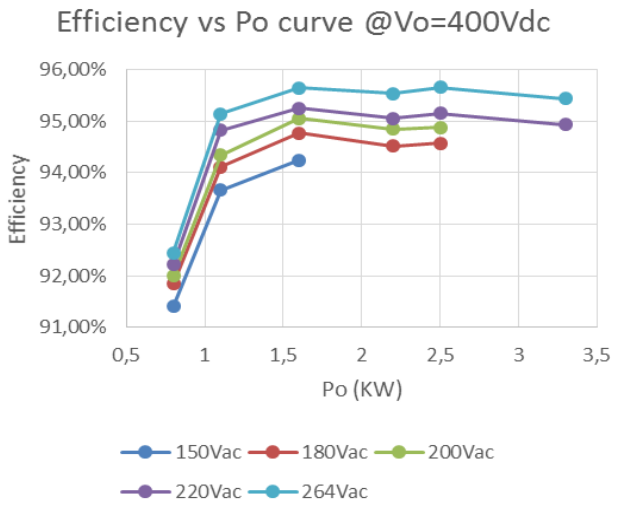


Figure 35. OBC Efficiency Measured from Bench Test using FAM65CR51DZ1 PFC Module and FAM65HRDS1 H−bridge Module

Table 9. EFFICIENCY SIMULATION RESULTS FOR 3.3 kW OBC SYSTEM

OBC Power	Switching Device	Efficiency [%]		
		PFC	DC/DC	OBC Total
1.4 kW	FAM65CR51DZ1 and FAM65HR51DS1−51 mΩ Die	98	96.7	94.8
	NTHL040N65 (TO247)	97.8	96.2	94.1
	NTHL082N65 (TO247)	98	96.5	94.6
1.8 kW	FAM65CR51DZ1 and FAM65HR51DS1−51 mΩ Die	96	96.4	92.5
	NTHL040N65 (TO247)	95.3	95.1	90.6
	NTHL082N65 (TO247)	95.6	95.8	91.6
2.4 kW	FAM65CR51DZ1 and FAM65HR51DS1−51 mΩ Die	97.8	97	94.9
	NTHL040N65 (TO247)	97.6	96.3	94
	NTHL082N65 (TO247)	97.9	96.6	94.6
3.3 kW	FAM65CR51DZ1 and FAM65HR51DS1−51 mΩ Die	98	97.3	95.4
	NTHL040N65 (TO247)	97.8	96.6	94.5
	NTHL082N65 (TO247)	97.9	96.6	94.6
3.52 kW (Worst Cace in DC/DC)	FAM65CR51DZ1 and FAM65HR51DS1−51 mΩ Die	98	93.8	91.9
	NTHL040N65 (TO247)	97.8	90.3	88.3
	NTHL082N65 (TO247)	98	91.6	89.8

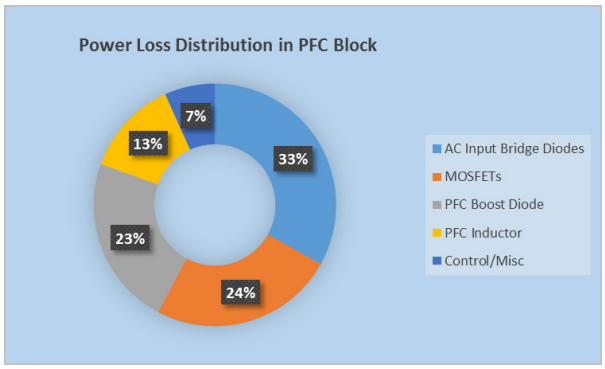


Figure 36. Power Loss Distribution in PFC Function Block

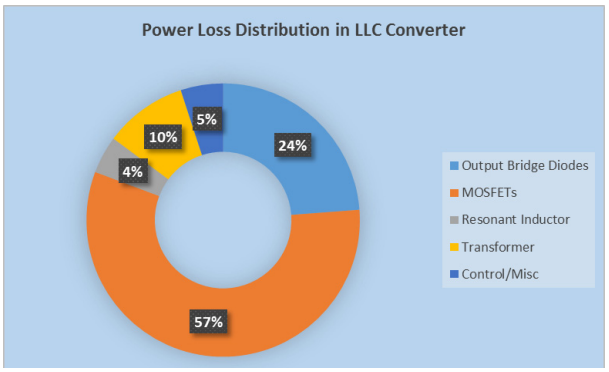


Figure 37. Power Loss Distribution in DC/DC Converter Function Block

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