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Signal Driven Multiplexing of Silicon Photomultiplier Arrays

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APPLICATION NOTE

Silicon Photomultiplier (SiPM) technology is rapidly becoming the primary choice of photosensor in a wide range of applications, such as medical imaging and hazard and threat detection. These sensors have many advantages over other types of photodetector, such as low bias, uniformity, compactness, ruggedness and insensitivity to magnetic fields. SiPMs also have the benefit of allowing a great deal of flexibility in the creation of 2D arrays of sensors for imaging applications.

ON Semiconductor produces a range of SiPM sensors in compact surface mount packages that are suitable for reflow soldering. Creating large arrays with minimal dead space on PCB is now a well developed process that makes custom arrays easily available to a wide range of users. There is an Application Note that provides guidance on creating large area arrays with SiPMs.

The challenge in many imaging applications is how to read out and process the data from arrays that may contain a large number of pixels. This document describes one method of multiplexing SiPMs, employing Schottky diodes to provide summed readout of the fast output.

An additional Application Note gives a more general discussion of multiplexed readout of arrays of SiPMs, using either fast or standard output.

Figure 1. The SDM Concept for a 2-pixel SiPM Array. Vbias and Sbias are Negative Voltages with Respect to 0 V

INTRODUCTION

Multiplexing with arrays of SiPM sensors introduces specific problems. If a number of channels are summed together the dark noise from each connected pixel is also summed. This can result in significant dark current upon which the signal is superimposed. This could impact the detection of smaller signals and certainly worsen the signal to noise ratio of the detector.

Another limitation of multiplexing of SiPM pixels is that of the summed capacitive load connected to each readout channel. Connecting many SiPM pixels to a single readout channel will result in slower signal rise times and recovery times and reduced pulse amplitude, with degradation of the achievable timing.

ON Semiconductor C-, J- and R-Series SiPM sensors have a fast, capacitively coupled output that gives a high speed output signal, which is suitable for timing applications. Summing the fast output directly is not recommended as this would negatively affect the resulting signal. By introducing a diode pair (fast Schottky) as shown in Figure 1, the Fast signal from the active SiPM is transferred to the Common Readout node while the Fast outputs of the remaining pixels in the array are effectively isolated from the Common Readout node.

Figure 2. P-on-N SiPM Structure. This Applies to B-Series, C-Series and J-Series SiPM Sensor Families

SPICE simulations and testing by ON Semiconductor have shown that the presence of the Schottky diodes has minimal impact on the individual pixel readout, and preserves the performance when arrays of SiPMs are multiplexed together. This application note details an evaluation that was performed on an array of ON Semiconductor SiPMs employing this SDM (Signal Driven Multiplexing) method to multiplex the Fast outputs.

SCHOTTKY DIODE

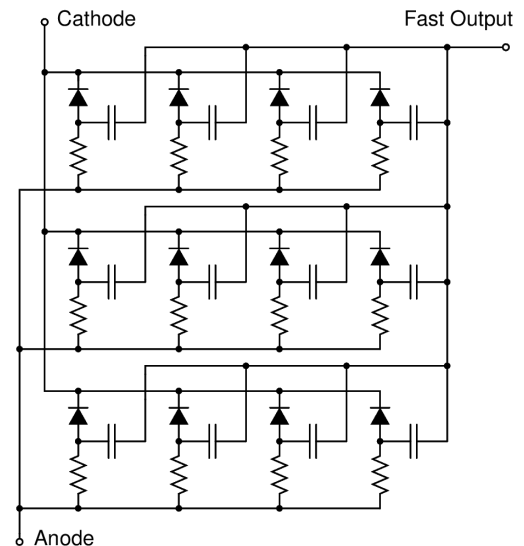Schottky diodes are nonlinear, signal driven devices that have very low capacitance and differ from normal diodes in that they have a lower voltage drop (0.15 V−0.45 V compared with 0.6 V−1.7 V for a standard diode) and are very fast (switching times of ~100 ps). Their main limitation is that of a 50 V rating. However, this is of no consequence for ON Semiconductor SiPM sensors which are biased in the range of 25 V−30 V.

FAST OUTPUT

The ON Semiconductor SiPM Fast output is a capacitively coupled output that provides a short pulse proportional in amplitude to the photocurrent signal at the SiPM standard output. It is beneficial in applications where the optical signal of interest is pulsed and timing is critical. The fast output is available in addition to the standard output and both may be read out simultaneously. A schematic of the SiPM architecture for a ON Semiconductor P-on-N sensor, showing the fast output is illustrated in Figure 2.

SIGNAL DRIVEN MULTIPLEXING METHOD

In applications requiring arrays of SiPMs, it may be desirable to obtain the sum of the signals from the fast outputs in the SiPM array. Direct summing of the fast outputs is not recommended. The total capacitance from all fast outputs together with the parasitic capacitance of the circuit would cause an increase in the fast output rise time, reduction in pulse height and lengthening of pulse width. The total noise at the summed output would also become more significant and cause a reduction in SNR with increasing pixel count.

The SDM method is proposed as a means to sum together the Fast outputs of a SiPM array without loss of the Fast output signal pulse shape or SNR. The SDM concept is illustrated in Figure 1.

In the schematic D1 and D2 comprise the SiPM array and are reverse biased by Vbias, as per normal Geiger mode operation. The Fast outputs of D1 and D2 are connected via the Schottky readout network, S1−S4. The summed readout signal is now at the Common Readout node, where the total capacitance seen by this trace due to the Schottky readout network ($C_{S1} + C_{S3}$) is less than the sum of the SiPM Fast output capacitances that would be seen if summed directly ($C_{D1} + C_{D2}$).

The theory of operation is as follows (referring to Figure 1): When the SiPM, D1, responds to incoming photons its fast output produces a positive voltage pulse that turns Schottky diode S1 on and at the same time turns the Schottky diode S2 off. When Schottky diode S1 turns on, the fast pulse is transferred to the Common Readout node and is coupled to Fout via coupling capacitor, C1. The Schottky diode pair creates a symmetry whereby the sum of current at the fast node is constant. The positive signal on the Common Readout node also reverse biases Schottky diodes of the other sensors, i.e. S3 is turned off. This has the effect of suppressing any noise generated by the other sensors during readout.

In this way, Schottky diodes are used as a 'signal driven' multiplexing scheme that will connect only the SiPM sensor that is activated by incident photons to the multiplexed readout channel. This approach significantly reduces the effective capacitance and noise at the common node such that single pixel performance is preserved.

Unbiased Schottky diodes will provide the benefits described above, but additional benefits can be achieved by applying a bias to the Schottky diodes themselves. The applied voltage, Sbias, together with the series resistor, Rs, set up a forward bias across the Schottky diodes such that a standing current is flowing through the diodes. Maintaining the Schottky diodes in this state allows the diodes to respond faster, and with greater sensitivity, to a breakdown in the SiPM, thus reducing rise times and improving timing measurements. This is also useful for applications where the signal output is weak.

As the value of the Schottky Bias voltage increases the effective resistance of S2 will decrease. This decrease in resistance between the Fast terminal of D1 and the 0 V terminal will have the effect of reducing the amplitude of the Fast output pulse. This effect becomes less significant with increasing bias voltage as the Schottky diodes reach saturation. A bias point can be found where the reduced pulse amplitude is sufficiently offset by the improved rise time such that the pulse timing at Fout is optimized.

EXPERIMENTAL TESTING OF SDM

ON Semiconductor built and tested dedicated evaluation boards using 3 mm B-Series SiPM arrays employing the SDM technique, details of which are described in the following sections.

The aim of this experimental testing was to:
1. Validate the SDM method
2. Demonstrate optimized board design for SDM
3. Determine the degree of multiplexing that is achievable using this method

B-Series sensors are pin compatible with C-Series so the following information can be considered equally valid for C-Series SiPMs. Other SiPMs such as J-Series have a similar architecture with fast readout and are also considered suitable for use with this readout method. Arrays of 1 mm or 6 mm sensors may also be combined using the SDM method. While full evaluation of all sensor families has not been carried out to date, the concept has been shown to work well with 6 mm B-Series sensors, where the higher

amplitude of the output signal is beneficial. Similarly the same method has been shown to work with N-on-P M-Series SiPMs.

SDM EVALUATION BOARD DETAILS

A multi-pixel SDM evaluation board was built and tested. The SDM evaluation design uses 3 mm B-Series SiPMs (MicroFB−30035−SMT). SiPMs are mounted in a rectangular array on one side of a 4-layer PCB with a 1 mm gap between adjacent SiPMs. The Schottky diodes are mounted on the opposite side of the array. The diode pair is placed directly opposite the connected SiPM to minimise routing between them. The PCB has internal layers dedicated to bias and 0 V planes.

To avoid PCB parasitics influencing test results, the evaluation board design was simplified to provide only a single multiplexed Fast output, Fout. No additional outputs were routed and there is no on board amplification of the SDM output.

Extra circuit elements are not included for the purpose of the evaluation because the addition of such elements could impact circuit performance metrics by introducing parasitic effects and it may be difficult to separate such effects during analysis.

To evaluate the effect of the degree of multiplexing on timing performance 3 evaluation boards were built with increasing pixel count. 16-pixel, 32-pixel and 64-pixel versions of the design were characterized.

A picture of the three boards is shown in Figure 3. Figure 5 shows the schematic for the 16-pixel version of the evaluation board.
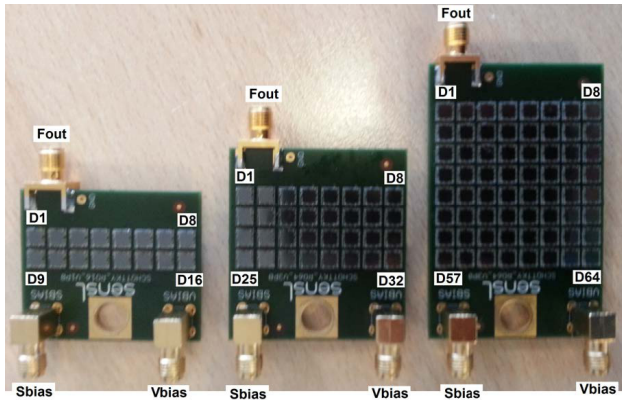

Figure 3. 16, 32 and 64-pixel Evaluation Boards

The evaluation boards have just 3 connectors: Fout is the capacitively coupled output from the Common Readout node and this is output via a SMA connector. SiPM bias voltage (Vbias) and Schottky bias voltage (Sbias) are applied via additional SMA connectors.

Vbias is a negative voltage (−29.5 V used in this evaluation) and is applied at the SiPM array common anode.

Sbias is also a negative voltage and this applies a forward bias across the Schottky diodes. A 1 kΩ resistor, Rs, is

placed in series with Sbias at the Common Readout node. The bias voltage is adjusted such that an optimal standing current of < 1 mA per Shottky diode is set up.

The SMA Input and Output stages of the 16, 32 and 64-Pixel arrays are identical. The only difference between the circuits is the number of pixels per array.
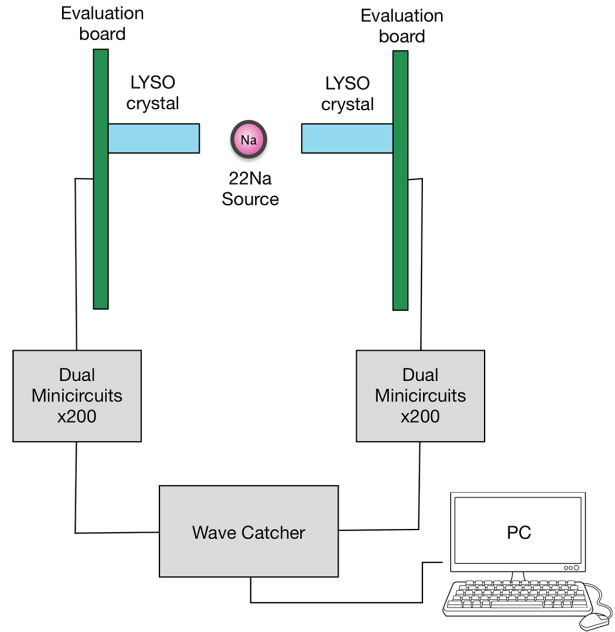
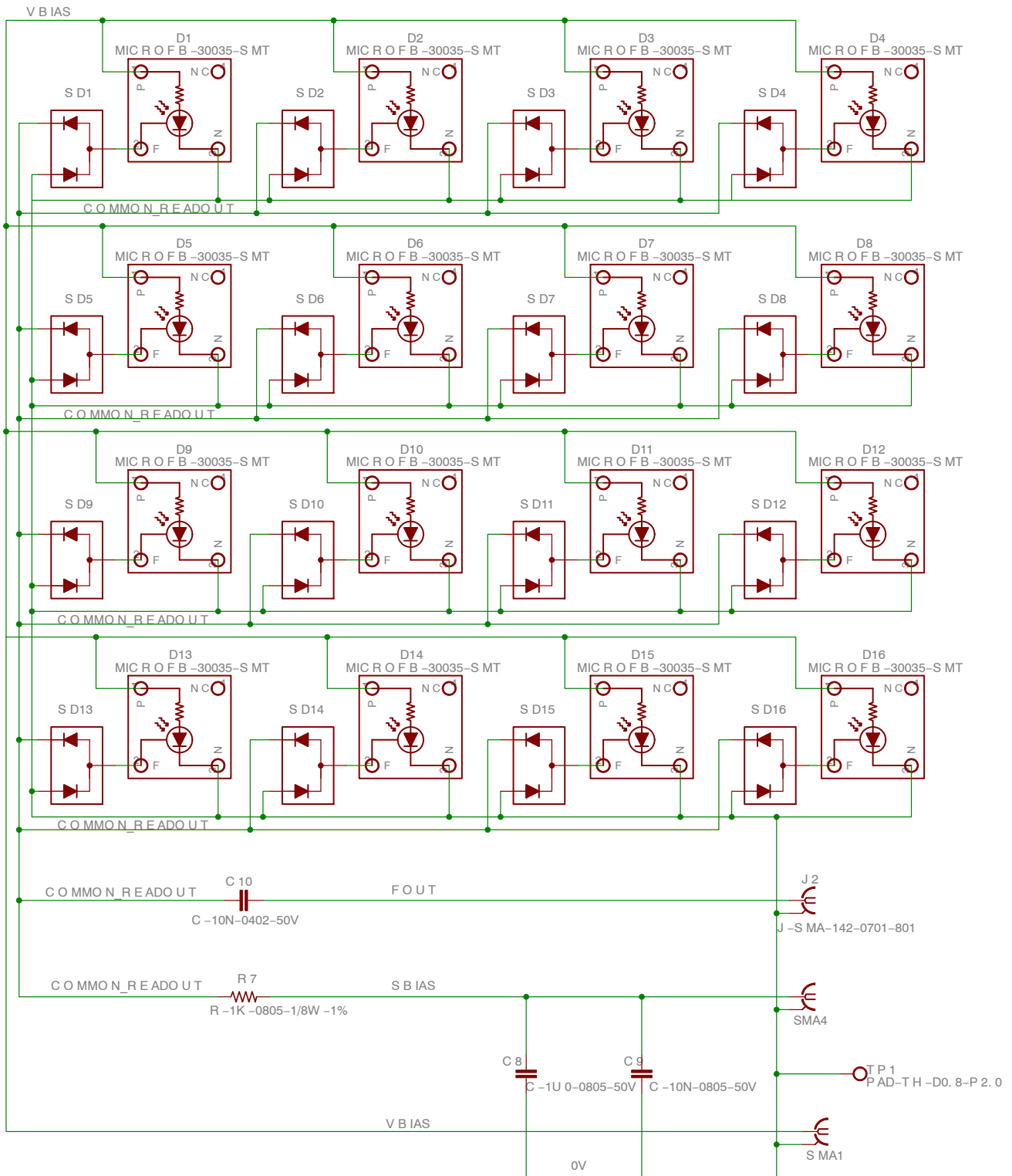**Figure 4. CRT Measurement Set-up**

EXPERIMENTAL SETUP AND TEST PROCEDURE

In order to assess the timing performance of the method the evaluation boards were used to make Coincidence Resolving Time (CRT) measurements. In a PET medical imaging application CRT is a time window such that any events detected within the CRT window may be considered coincident. A low CRT value is required in PET applications to facilitate collection of Time of Flight information.

A simple schematic of the test setup used to measure the CRT is shown in Figure 4. Two identical evaluation boards (both boards having either 16, 32 or 64 pixels) were set up opposite each other in a light-tight box. For each board a 3 x 3 x 20 mm^3 LYSO crystal was coupled, using optical grease, to a specific sensor in the array. A Na22 source of 511 keV gamma rays was mounted between the two crystals. The source and crystals were mounted on X, Y, Z stages to allow for easy alignment of crystals and source at various sensor locations.

To amplify the SDM output signal Minicircuits amplifiers were used between the evaluation boards and acquisition system. MiniCircuits ZX60−43 and ZFL−1000LN+ were connected in series providing a total gain of ~200 on Fout. The amplified signal was fed to the Wave Catcher, and the data was acquired, via high speed USB interface, by the host computer for analysis. ON Semiconductor Wave Catcher Analysis software was used to calculate the CRT.

Figure 5. Schematic of the 16-pixel SDM Evaluation Board.
SDn Components are the SMS7621−005LF SOT23 Package

The same test procedure was used for the 16, 32 and 64-pixel boards. For each board type, the CRT measurement was repeated for a variety of sensor locations and Schottky bias voltages.

In all cases the same SiPM bias voltage of 29.5 V (~5 V overvoltage) was applied to the SiPM array.

Table 1. CRT RESULTS FOR DIFFERENT SDM BOARDS, PIXEL LOCATIONS AND SCHOTTKY BIAS VALUES

Board Type	Threshold	Bias	Pixel ID 1	Pixel ID 2	Schottky Bias	Measured CRT
16-pixel	0.3 V	29.5 V	D1	D1	−15 V	311 ps
			D9	D9	−20 V	312 ps
			D1	D1	−12 V	304 ps
			D1	D1	−9 V	371 ps
			D8	D16	−12 V	321 ps
32-pixel			D9	D9	−12 V	385 ps
			D9	D9	−20 V	371 ps
			D8	D8	−24 V	374 ps
			D32	D8	−20 V	385 ps
64-pixel			D2	D2	−12 V	552 ps
			D2	D2	−20 V	480 ps
			D2	D2	−24 V	480 ps
			D57	D64	−20 V	480 ps
			D57	D64	−30 V	473 ps

RESULTS

Table 1 summarizes the results obtained for each evaluation board. The best corresponding CRT plot for each array size is shown in Figures 6–8.

It was found that the best Schottky bias for the 16-pixel board was −12 V, producing a Schottky diode current of ~0.7 mA.

For the 32-pixel board, a CRT of 371 ps was achieved. Once again other combinations of pixels, farther away from the Fout SMA connector gave consistent results with variation of no greater than 14 ps.

It was found that the best Schottky bias for the 32-pixel board was −20 V, producing a Schottky diode current of ~0.6 mA.

For the 64-pixel board it was found that a Schottky bias voltage of −30 V (Schottky diode current ~0.5 mA) gave best results with a CRT of 473 ps. However, it was found that with a Schottky bias of −20 V (Schottky diode current ~0.3 mA) a CRT of 480 ps could be consistently measured over different pixel combinations including the two pixels (D57, D64) farthest from the Fout SMA connector.
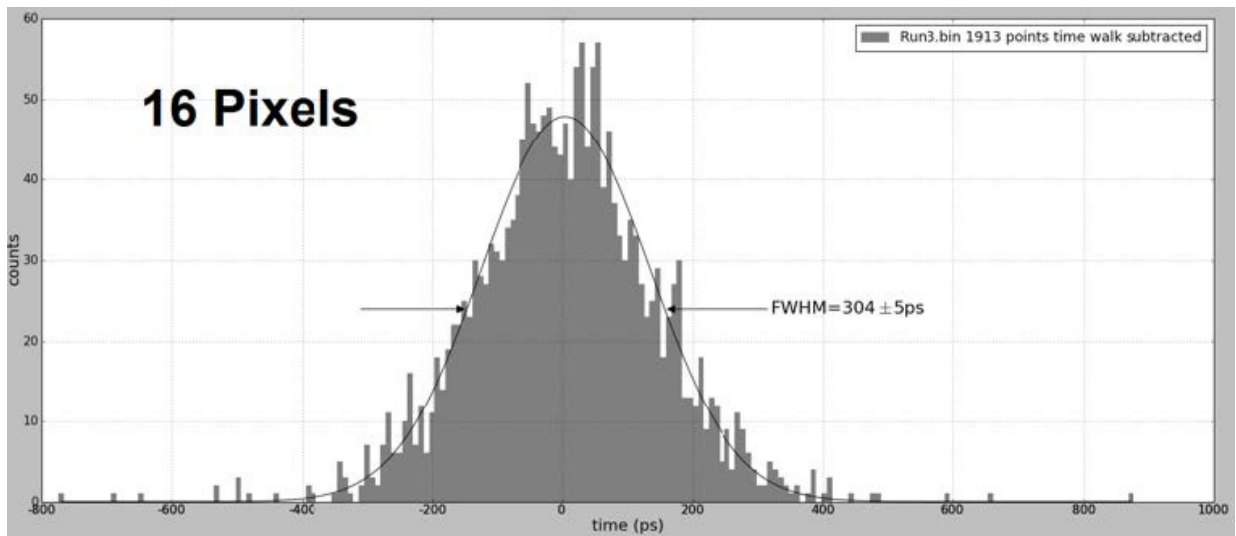
Figure 6. Plot Showing the Best CRT Achieved with the 16-pixel SDM Board
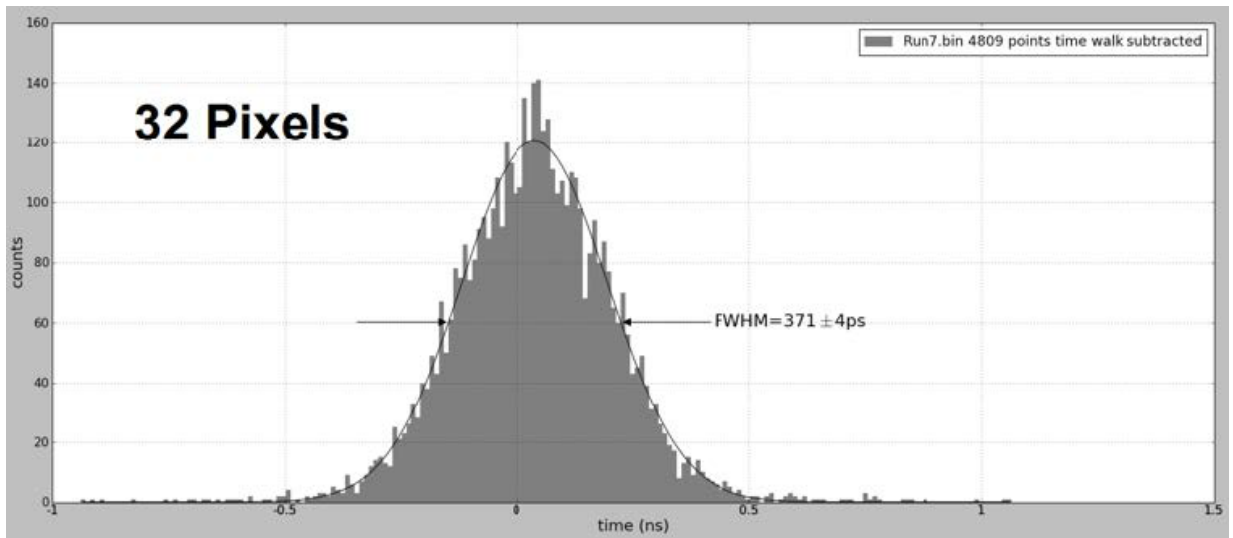
Figure 7. Plot Showing the Best CRT Achieved with the 32-pixel SDM Board
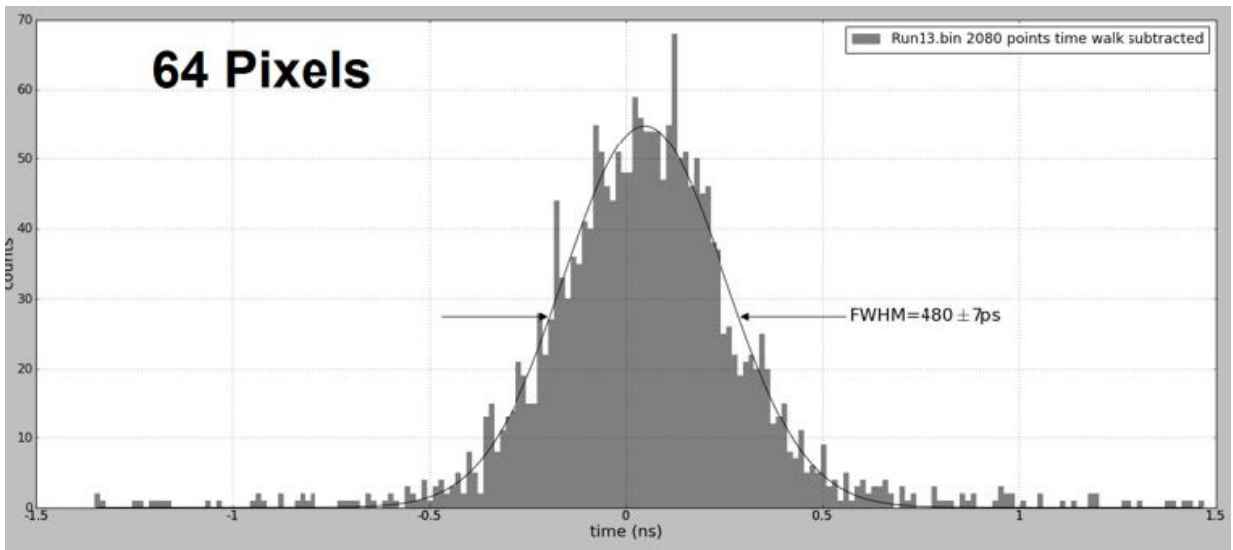

Figure 8. Plot Showing the Best CRT Achieved with the 64-pixel SDM Board

CONCLUSIONS

Characterisation of the SDM evaluation board shows that, for arrays of up to 32 pixels in size the Schottky-based SDM technique enables Fast output signals to be combined whilst maintaining sub-400ps timing. It is clear from measurements at different board locations that minimizing parasitics and maintaining a symmetrical board layout are critical to achieving a low CRT value.

As the degree of multiplexing is increased the timing deteriorates, and this is mostly due to the increase in parasitics with increasing board area. Figure 9 shows a plot of measured CRT versus number of pixels.

The applied Schottky bias voltage also affects the achievable timing. With the configuration employed here, an optimal bias voltage (and current) exists for each array type.

RECOMMENDATIONS

The following recommendations are based on observations and evaluated circuit performance and should be noted when implementing SDM or similar techniques:

- In the evaluation board design Schottky diode pairs are mounted directly beneath the SiPM to minimise routing. It is critical that caution is exercised to minimise parasitic circuit elements on all fast signal traces and that high speed PCB layout techniques are employed where necessary due to the high speed of the Fast signals.
- There is no on board amplification in the evaluation board design but it may be desirable to add this to a custom design. A carefully chosen RF amplifier is recommended to amplify the high speed pulse output. One SMT amplifier that has been found to work well with the fast

output is Analog Devices HMC580ST89. Any additional circuit elements should be carefully considered. Care should be taken so that additional components do not interfere with the SiPM array, both in terms of interfering signals and thermal coupling.

- The SiPM standard output is not simultaneously read out in the evaluation designs. It may be desirable to do so in a custom application but note that this change may affect achievable CRT measurements due to extra parasitics.

- Decoupling of the Schottky bias line is necessary. The evaluation board schematic, implements this decoupling with 1 μF and 0.01 μF ceramic capacitors.

- In the evaluation board the Schottky bias voltage is applied through a single 1 kΩ resistor, connected at the summed fast readout node. The resistor limits the current through the Schottky diodes to a useful level and isolates the output signal from the fixed Schottky bias voltage, Sbias. It also affects the trace impedance. An alternative resistor size may be used but it should be carefully evaluated and should fulfil the same functions. The optimal Schottky bias voltage can be found through experiment.

- The Schottky diode used in the evaluation is the Skyworks SMS7621−005LF. Alternative diodes may be

used but should be carefully evaluated first as the evaluation board circuit behavior may not be repeatable with alternative diodes.

- Careful optical coupling and alignment of crystal and source is necessary to achieve repeatable CRT measurements.
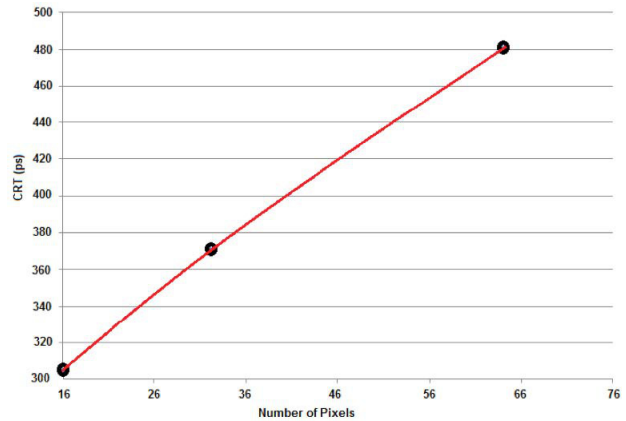
Figure 9. CRT as a Function of the Number of Pixels in the Array