AND9550/D

3-phase Inverter IPM Application Note using the STK534U3xx series

APPLICATION NOTE

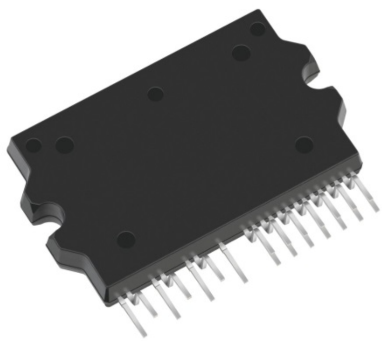
1. Product synopsis

This application note provides practical guidelines for designing with the **STK534U3xx series**.

The STK534U3xx series is an Intelligent Power Module (IPM) for 3-phase motor drives containing a three-phase inverter stage, gate drivers for the inverter stages and a thermistor. It uses ON Semiconductor's Insulated Metal Substrate (IMS) Technology.

The key functions are outlined below:

- Highly integrated power module containing an inverter power stage for a high voltage 3-phase inverter in a single in-line (SIP) package.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a fault detection output flag. Internal bootstrap diodes are provided for the high-side drivers.
- Separate pins for each of the three low-side emitter terminals.
- Thermistor for substrate temperature measurement.
- All control inputs and status outputs have voltage levels compatible with microcontrollers.
- Single VDD power supply due to internal bootstrap circuit for high-side gate driver circuit.
- Mounting holes for easy assembly of heat sink with screws.



SIP05
(SIP29 44X26.5)

A simplified block diagram of a motor control system is shown in Figure 1.

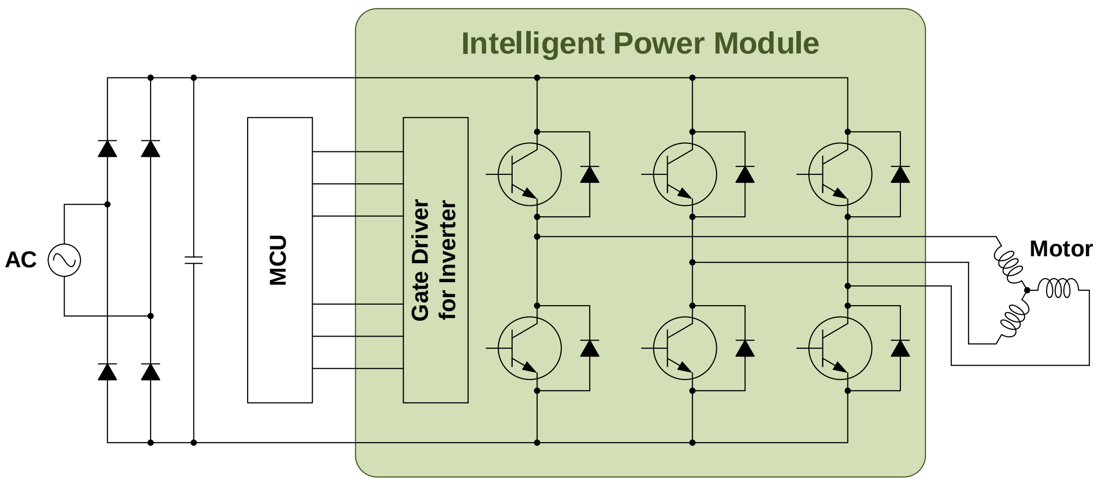


Figure 1. Motor Control System Block Diagram

2. Product description

Table1 gives an overview of the devices. For package drawing, please refer to Chapter 6.

Device	**STK534U342C-E**	**STK534U362C-E ***	**STK534U363C-E ***
Package	SIP05 – Vertical pins		
Voltage (V_{CEmax})	600 V		
Current (Ic)	5 A	10 A	
Peak current (Ic)	10 A	20 A	
Isolation voltage	2000 V		
Input logic	High-active		
Shunt resistor	triple shunts / external		

* 362: Low noise, 363: Low swiching loss

Horizontal type models: STK534U3xxA-E series are available for pin forming option.

Table 1. Device Overview

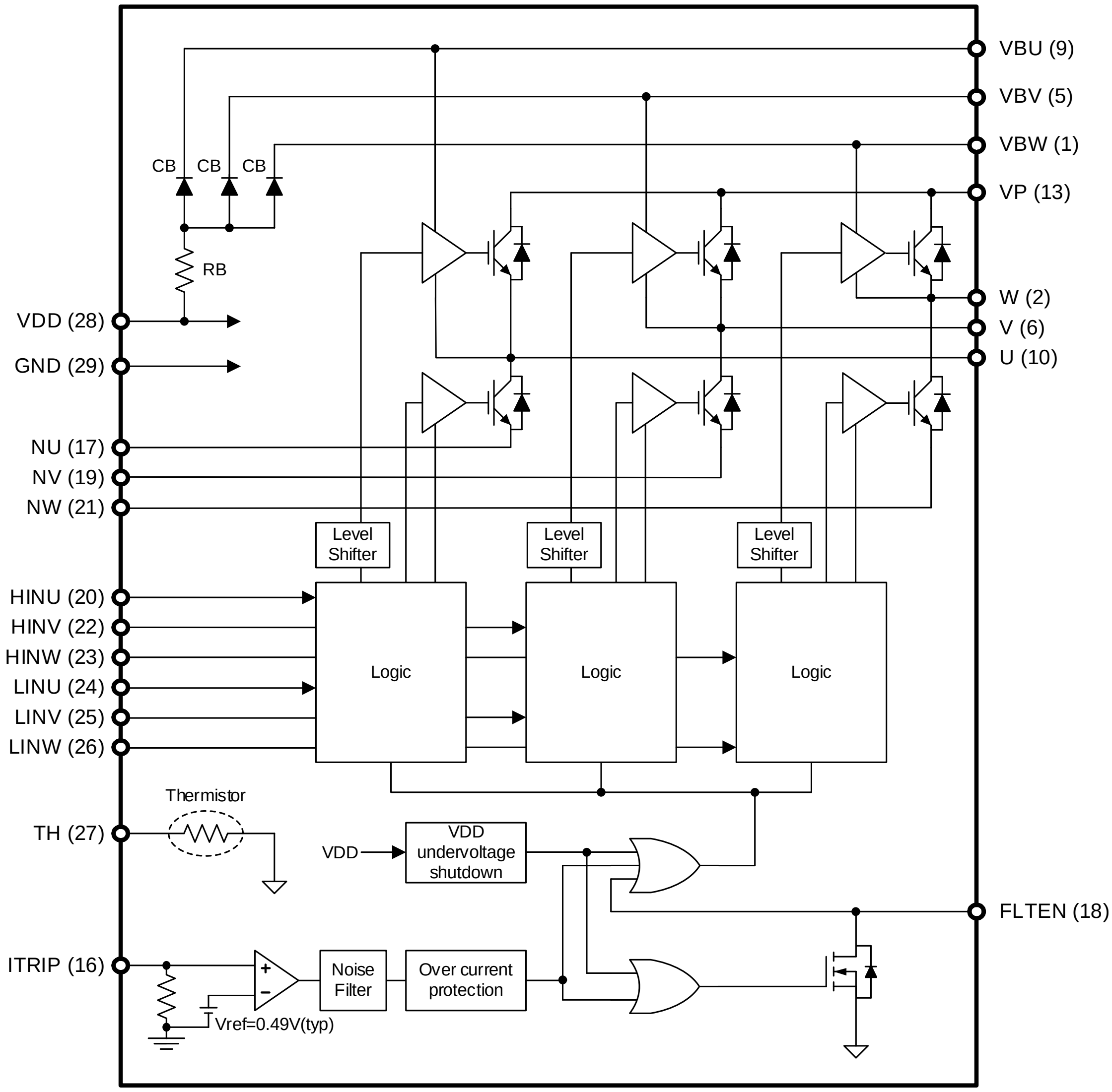


Figure 2. Internal Block Diagram

Three bootstrap circuits generate the voltage needed for driving the high-side IGBTs. The boost diodes are internal to the part and sourced from VDD (15 V). There is an internal level shift circuit for the high-side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with optocouplers.

3. Performance test guidelines

The methods used to test some datasheet parameters are shown in Figures 3 to 7.

3.1. Switching time definition and performance test method

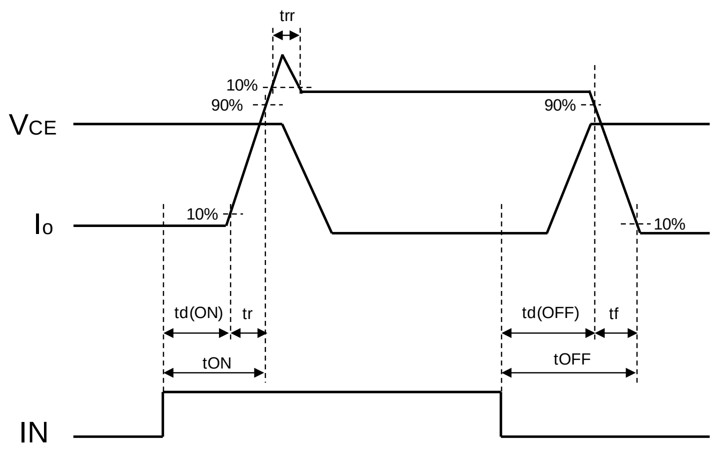


Figure 3. Switching Time Definition

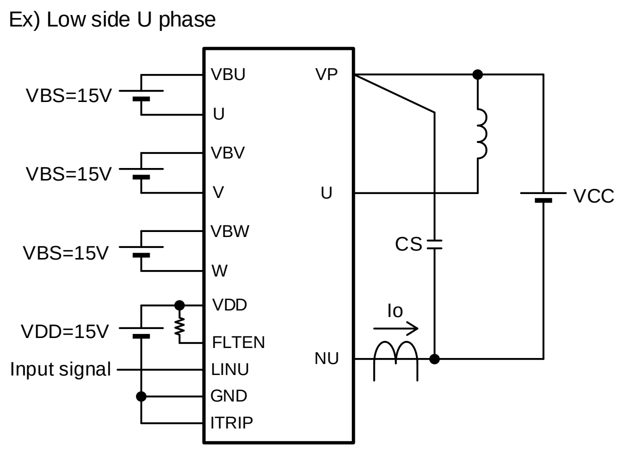


Figure 4. Evaluation Circuit (Inductive load)

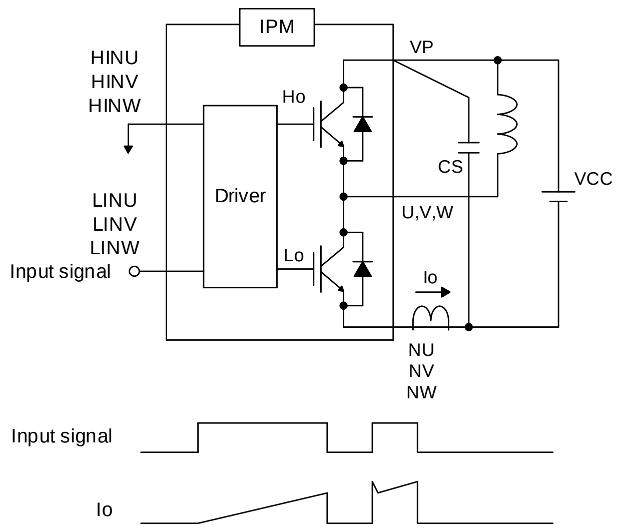


Figure 5. Switching Loss Measurement Circuit

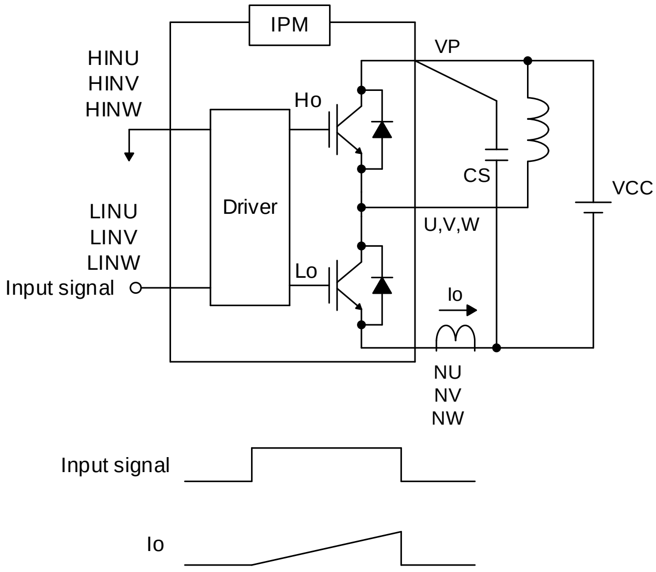


Figure 6. Reverse Bias Safe Operating Area Measurement Circuit

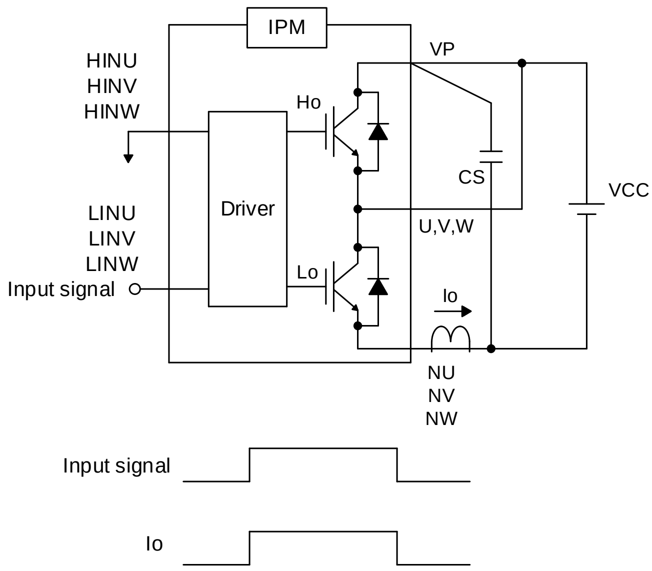


Figure 7. Short Circuit Safe Operating Area Measurement Circuit

3.2. Thermistor characteristics

The TH and GND pins are connected to a thermistor mounted on the module substrate. The thermistor is used to sense the internal substrate temperature. It has the following characteristics

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Resistance	R_{25}	Tc = 25°C	97	100	103	kΩ
Resistance	R_{100}	Tc = 100°C	5.07	5.38	5.71	kΩ
Temperature Range			–40		+125	°C

Table 2. NTC Thermistor Specification

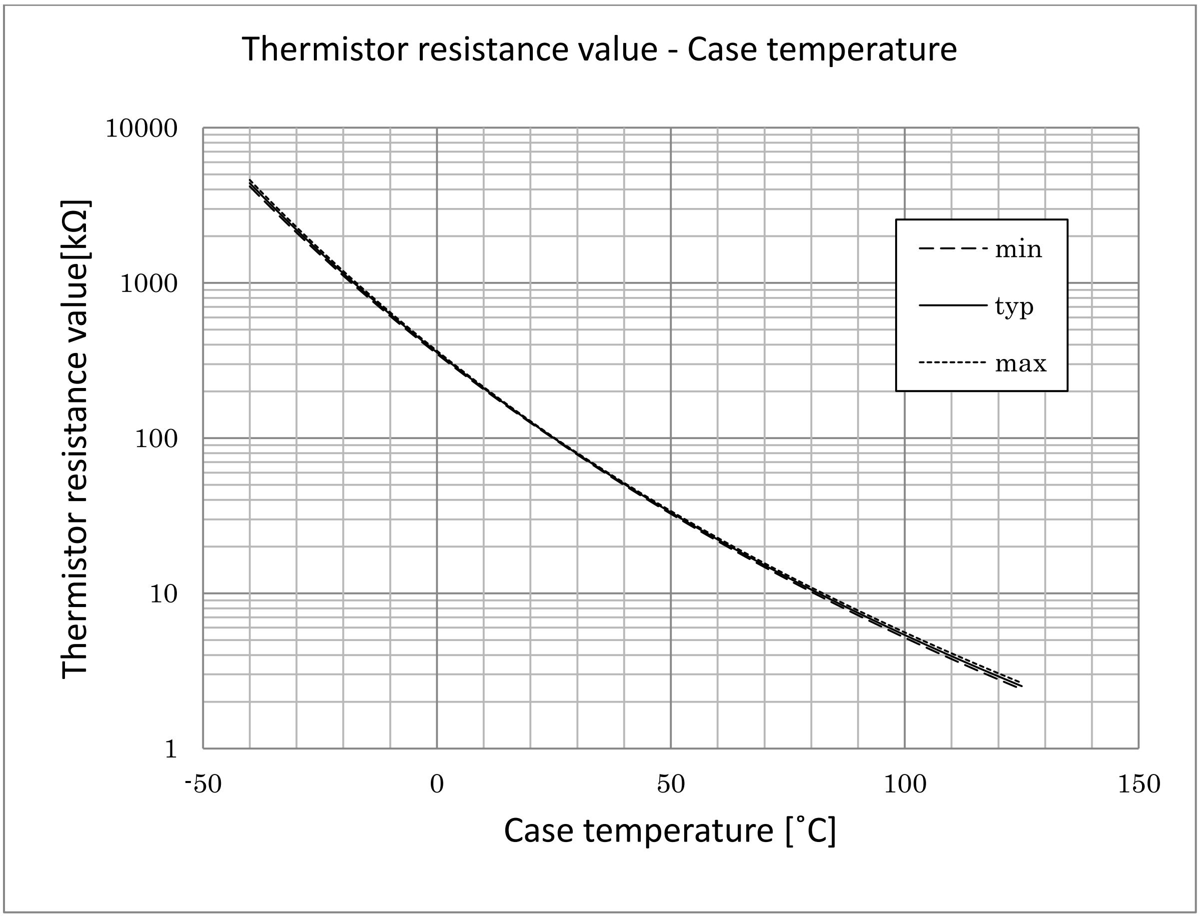


Figure 8. NTC Thermistor Resistance versus Temperature

Tc [°C]	Resistance value [kΩ]		
	Min	Typ	Max
-40	4106.84	4397.12	4703.67
-39	3825.43	4092.87	4375.08
-38	3565.18	3811.72	4071.64
-37	3324.37	3551.75	3791.26
-36	3101.43	3311.24	3532.05
-35	2894.91	3088.60	3292.28
-34	2703.51	2882.40	3070.35
-33	2526.01	2691.31	2864.84
-32	2361.33	2514.14	2674.42
-31	2208.45	2349.78	2497.90
-30	2066.46	2197.23	2334.16
-29	1934.52	2055.56	2182.21
-28	1811.84	1923.93	2041.12
-27	1697.72	1801.57	1910.05
-26	1591.52	1687.77	1788.23
-25	1492.64	1581.88	1674.95
-24	1400.33	1483.10	1569.35
-23	1314.32	1391.11	1471.07
-22	1234.13	1305.41	1379.57
-21	1159.35	1225.53	1294.33
-20	1089.56	1151.04	1214.89
-19	1024.41	1081.54	1140.82
-18	963.55	1016.66	1071.73
-17	906.69	956.08	1007.25
-16	853.54	899.48	947.04
-15	803.83	846.58	890.80
-14	757.31	797.11	838.25
-13	713.77	750.83	789.11
-12	673.00	707.52	743.15
-11	634.80	666.97	700.14
-10	599.00	628.99	659.88
-9	565.38	593.34	622.12
-8	533.86	559.93	586.75
-7	504.28	528.60	553.60
-6	476.51	499.21	522.52
-5	450.44	471.63	493.37
-4	425.98	445.77	466.06
-3	403.00	421.48	440.41
-2	381.38	398.65	416.33
-1	361.05	377.19	393.70
0	341.92	357.01	372.43
1	323.90	338.01	352.41
2	306.93	320.12	333.58
3	290.94	303.29	315.87
4	275.88	287.43	299.20
5	261.69	272.50	283.50
6	248.30	258.43	268.72
7	235.68	245.16	254.79
8	223.77	232.65	241.66
9	212.53	220.85	229.28
10	201.92	209.71	217.61
11	191.89	199.20	206.59
12	182.42	189.27	196.19
13	173.47	179.89	186.38
14	165.01	171.03	177.11
15	157.01	162.65	168.35

Tc [°C]	Resistance value [kΩ]		
	Min	Typ	Max
16	149.43	154.73	160.07
17	142.26	147.23	152.24
18	135.48	140.14	144.83
19	129.06	133.43	137.83
20	122.97	127.08	131.21
21	117.21	121.07	124.94
22	111.75	115.37	119.00
23	106.57	109.97	113.38
24	101.66	104.85	108.05
25	97.00	100.00	103.00
26	92.49	95.40	98.31
27	88.22	91.03	93.85
28	84.16	86.89	89.62
29	80.32	82.96	85.60
30	76.67	79.22	81.79
31	73.20	75.68	78.16
32	69.91	72.31	74.72
33	66.78	69.10	71.44
34	63.81	66.06	68.33
35	60.99	63.17	65.36
36	58.31	60.42	62.54
37	55.76	57.80	59.86
38	53.33	55.31	57.30
39	51.02	52.93	54.87
40	48.82	50.68	52.55
41	46.73	48.53	50.35
42	44.74	46.48	48.24
43	42.85	44.53	46.24
44	41.04	42.67	44.33
45	39.32	40.90	42.51
46	37.68	39.21	40.77
47	36.12	37.60	39.11
48	34.63	36.06	37.53
49	33.20	34.60	36.01
50	31.85	33.19	34.57
51	30.55	31.86	33.19
52	29.32	30.58	31.88
53	28.14	29.37	30.62
54	27.01	28.20	29.42
55	25.94	27.09	28.27
56	24.91	26.03	27.17
57	23.93	25.01	26.12
58	22.99	24.04	25.12
59	22.09	23.11	24.16
60	21.24	22.22	23.24
61	20.42	21.37	22.36
62	19.63	20.56	21.52
63	18.88	19.78	20.71
64	18.16	19.04	19.94
65	17.47	18.32	19.20
66	16.82	17.64	18.49
67	16.19	16.99	17.81
68	15.58	16.36	17.16
69	15.01	15.76	16.54
70	14.45	15.18	15.94
71	13.92	14.63	15.36

Tc [°C]	Resistance value [kΩ]		
	Min	Typ	Max
72	13.41	14.10	14.81
73	12.92	13.59	14.28
74	12.45	13.10	13.77
75	12.01	12.64	13.29
76	11.58	12.19	12.82
77	11.16	11.76	12.37
78	10.77	11.34	11.94
79	10.39	10.95	11.53
80	10.02	10.57	11.13
81	9.67	10.20	10.75
82	9.33	9.85	10.38
83	9.01	9.51	10.03
84	8.70	9.18	9.69
85	8.40	8.87	9.36
86	8.11	8.57	9.05
87	7.84	8.28	8.75
88	7.57	8.01	8.46
89	7.32	7.74	8.18
90	7.07	7.48	7.91
91	6.84	7.23	7.65
92	6.61	7.00	7.40
93	6.39	6.77	7.16
94	6.18	6.55	6.93
95	5.98	6.34	6.71
96	5.78	6.13	6.49
97	5.60	5.93	6.29
98	5.41	5.74	6.09
99	5.24	5.56	5.90
100	5.07	5.38	5.71
101	4.91	5.21	5.53
102	4.76	5.05	5.36
103	4.61	4.89	5.19
104	4.46	4.74	5.03
105	4.32	4.59	4.88
106	4.19	4.45	4.73
107	4.06	4.32	4.59
108	3.93	4.18	4.45
109	3.81	4.06	4.31
110	3.69	3.93	4.19
111	3.58	3.82	4.06
112	3.47	3.70	3.94
113	3.37	3.59	3.82
114	3.27	3.48	3.71
115	3.17	3.38	3.60
116	3.08	3.28	3.50
117	2.99	3.19	3.40
118	2.90	3.09	3.30
119	2.81	3.00	3.20
120	2.73	2.92	3.11
121	2.65	2.83	3.02
122	2.57	2.75	2.94
123	2.50	2.67	2.85
124	2.43	2.60	2.77
125	2.36	2.52	2.70

Table 3. NTC Thermistor Resistance Values

4. Protection functions

This chapter describes the protection functions.

- Over-current protection
- Short circuit protection
- Under voltage lockout (UVLO) protection
- Cross conduction prevention

4.1. Over-current protection (OCP)

The STK534U3xx series module uses an external shunt resistor for the OCP functionality. As shown in Figure 9, the emitters of all three low-side IGBTs are brought out to module pins. The external OCP circuit consists of a shunt resistor and a RC filter network. If the application uses three separate shunts, an op-amp circuit is used to monitor the three separate shunts and provide an over-current signal.

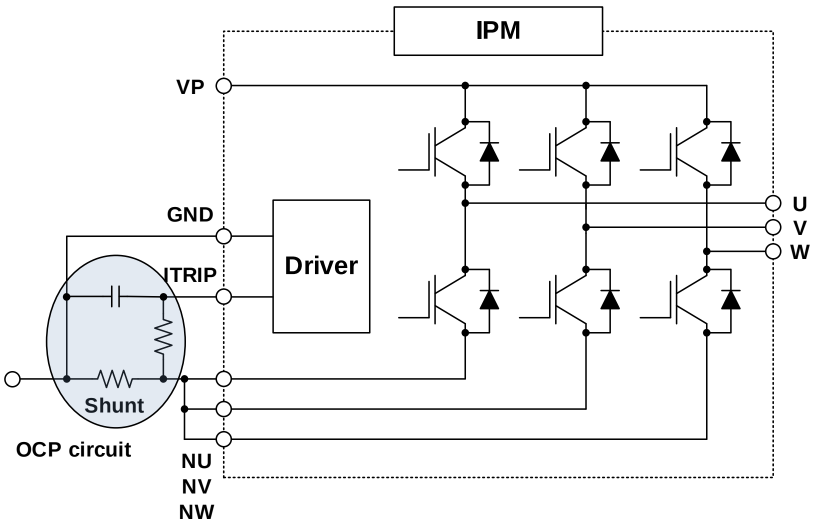


Figure 9. Over-current Protection Circuit

The OCP function is implemented by comparing the ITRIP input voltages with an internal reference voltage of 0.49 V (typ). If the voltage on this terminal exceeds the trip levels, an OCP fault is triggered. For single shunt applications, this voltage is the same as the voltage across the shunt resistor.

Note: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to be less than the module’s maximum current rating.

When an OCP fault is detected, all internal gate drive signals for the IGBTs become inactive and the fault signal output is activated. The FLTEN signal has an open drain output, so when there is a fault, the output is pulled low.

A RC filter is used on the ITRIP input to prevent an erroneous OCP detection due to normal switching noise or recovery diode current. The time constant of the RC filter should be set to a value between 1.5 µ to 2 µs. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to data sheet for SCSOA. The resulting OCP level due to the filter time constant is shown in Figure 10.

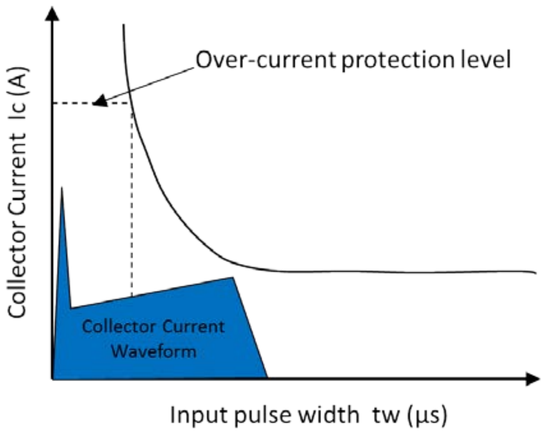


Figure 10. Filter Time Constant

For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 11 shows the sequence of events in case of an OCP event.

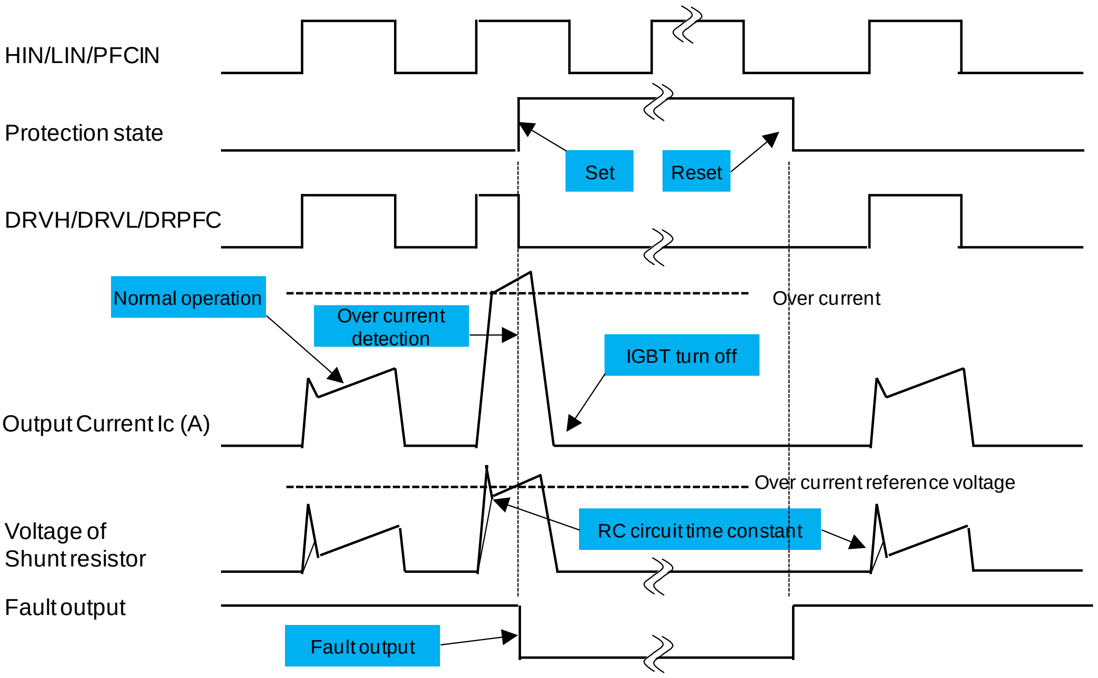


Figure 11. Over-current Protection Timing Diagram

4.2. Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 4. Both High-side and Low-side have undervoltage protection. The low-side UVLO condition is indicated on the FLTEN output. During the low-side UVLO state the FLTEN output is continuously driven low. A high-side UVLO condition is not indicated on the FLTEN output.

VDD Voltage (typ. Value)	Operation behavior
< 12.5V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12.5 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 16.5 V	Recommended conditions
16.5 V – 20.0 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk.
> 20.0 V	Control circuit is destroyed. Absolute max. rating is 20 V.

Table 4. Module Operation according to VDD Voltage

The sequence of events in case of a low-side UVLO event (IGBTs turned off and active fault output) is shown in Figure 12. Figure 13 shows the same for a high-side UVLO (IGBTs turned off and no fault output).

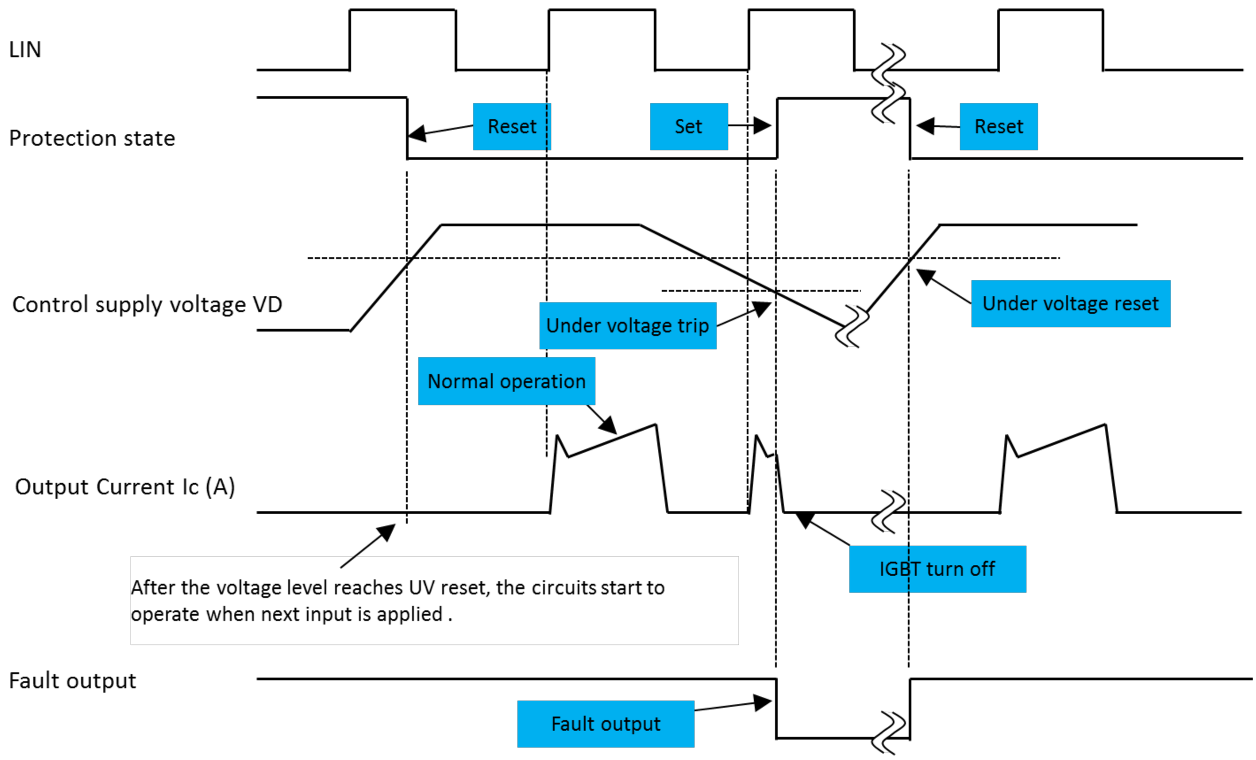


Figure 12. Low-side UVLO Timing Diagram

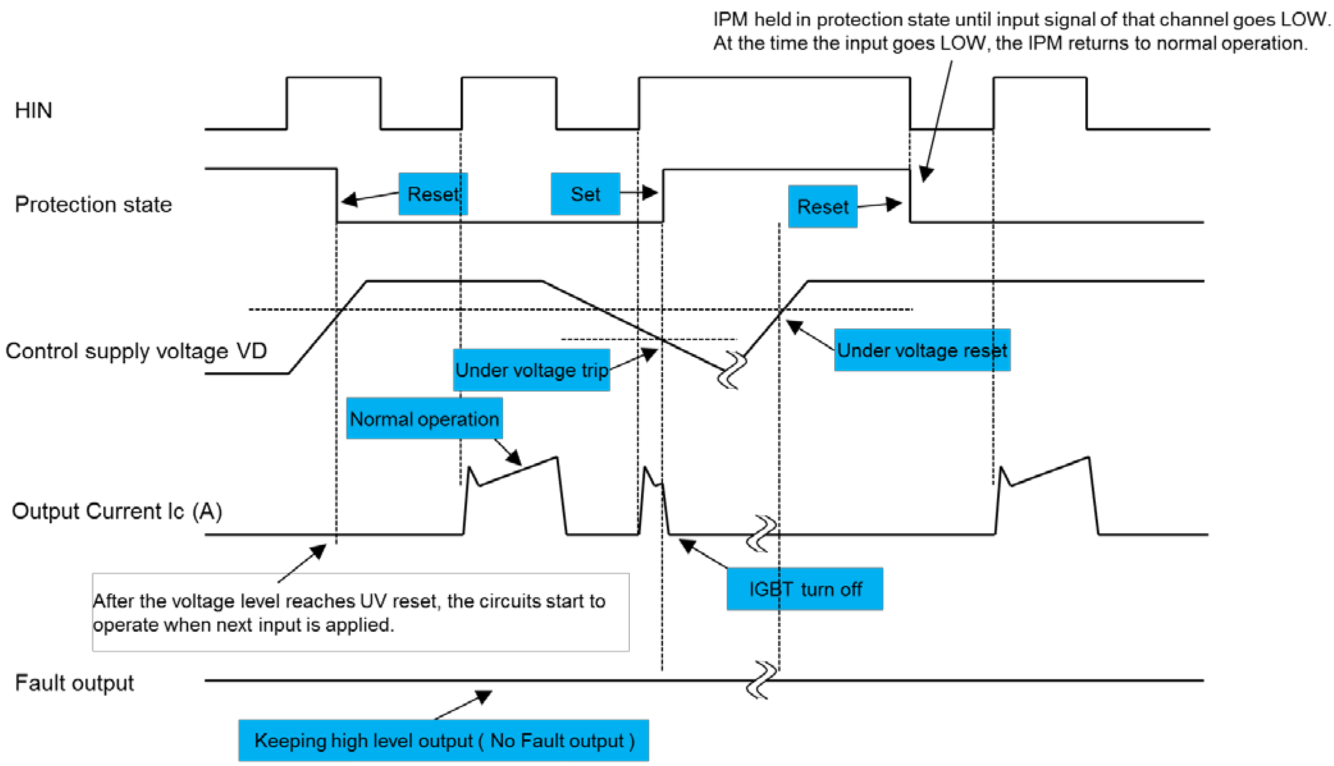


Figure 13. High-side UVLO Timing Diagram

4.3. Cross-conduction prevention

The STK534U3xx series module implements cross-conduction prevention logic at the gate driver to avoid simultaneous drive of the low-side and high-side IGBTs as shown in Figure 14.

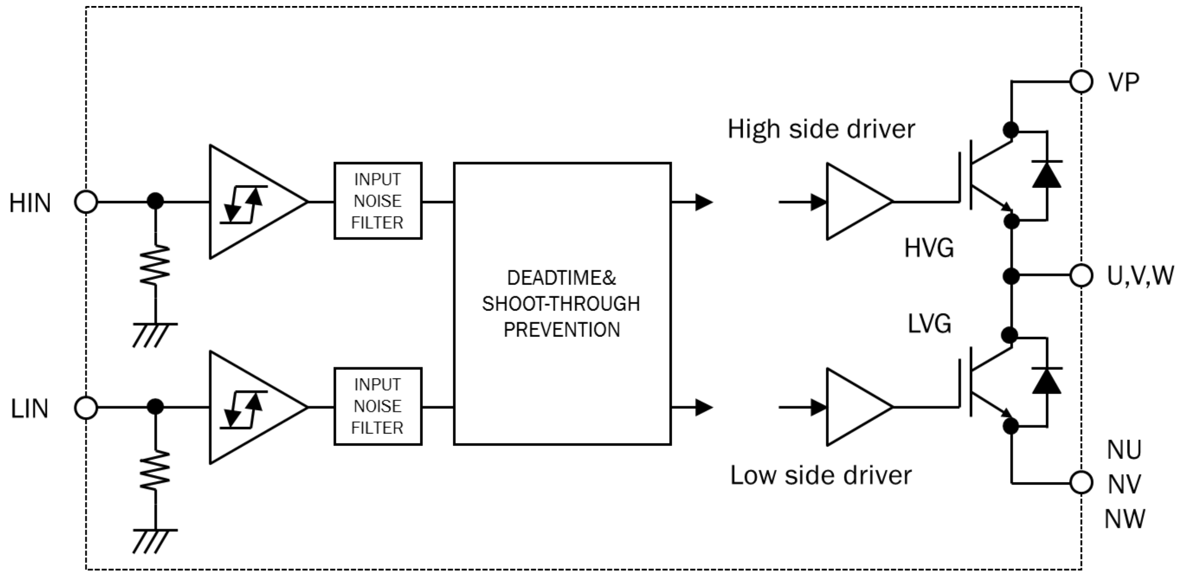


Figure 14. Cross-conduction Prevention

If both high-side and low-side drive inputs are active (HIGH) the logic prevents both gates from being driven as shown in Figure 15 below.

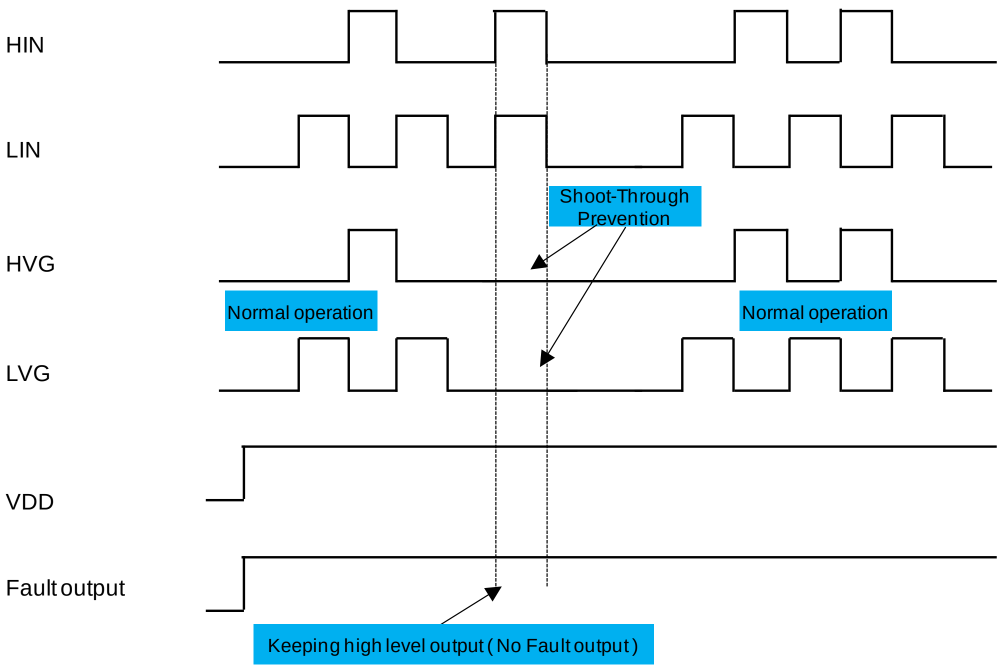


Figure 15. Cross-conduction Prevention Timing Diagram

Even if cross-conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry, the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 16 shows the delay from the HIN-input via the internal high-side gate driver to high-side IGBT, the delay from the LIN-input via the internal low-side gate driver to low-side IGBT and the resulting minimum dead time which is equal to the potential shoot through period:

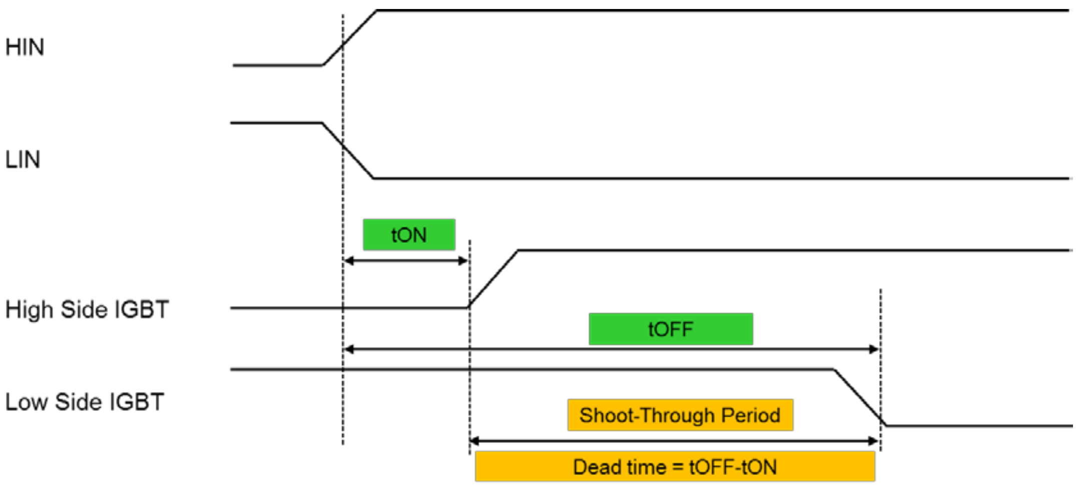


Figure 16. Shoot-through Period

5. PCB design and mounting guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

5.1. Application (schematic) design

Figure 17 gives an overview of the external components and circuits used when designing with the STK534U3xx series module.

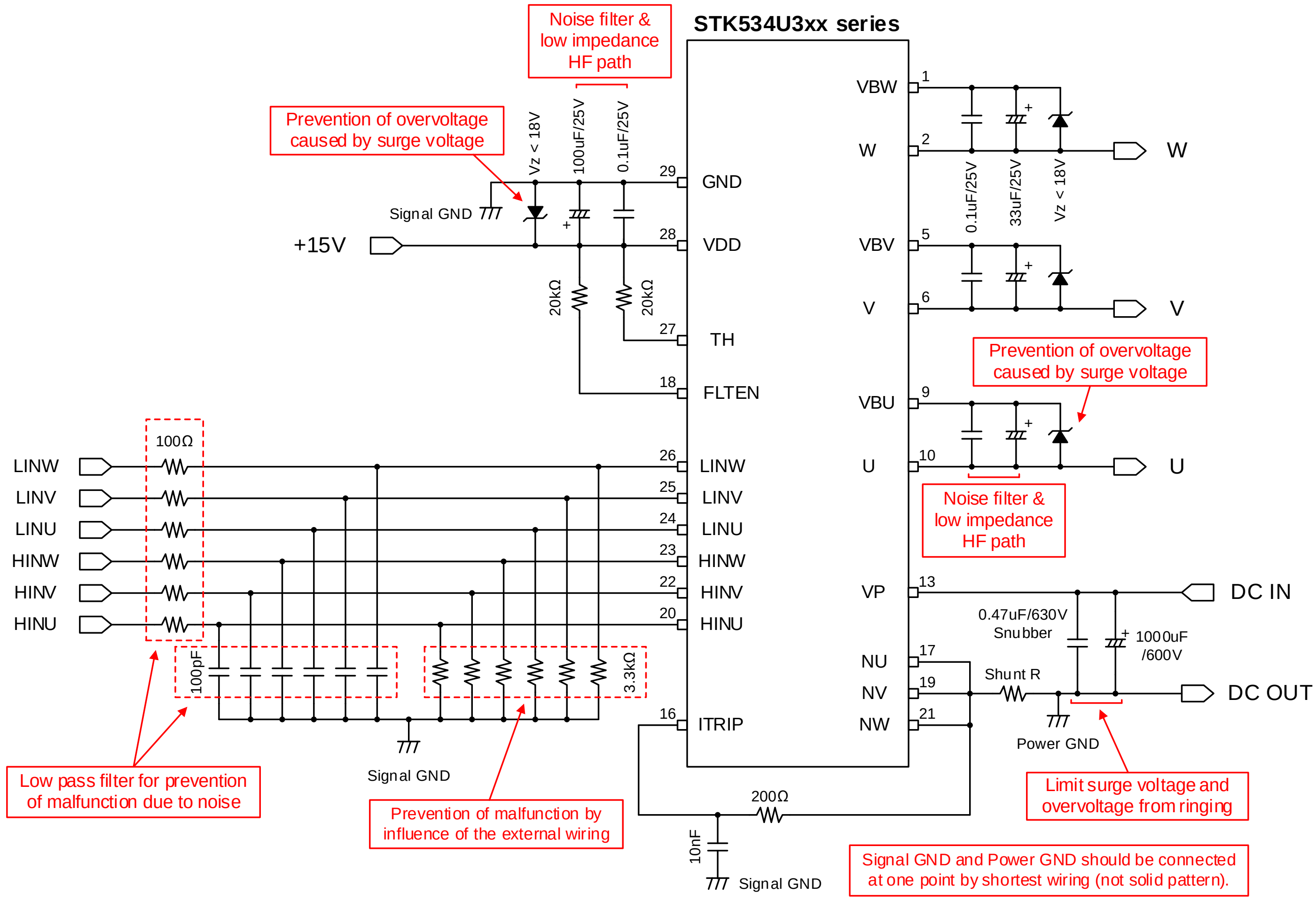


Figure 17. Application Circuit

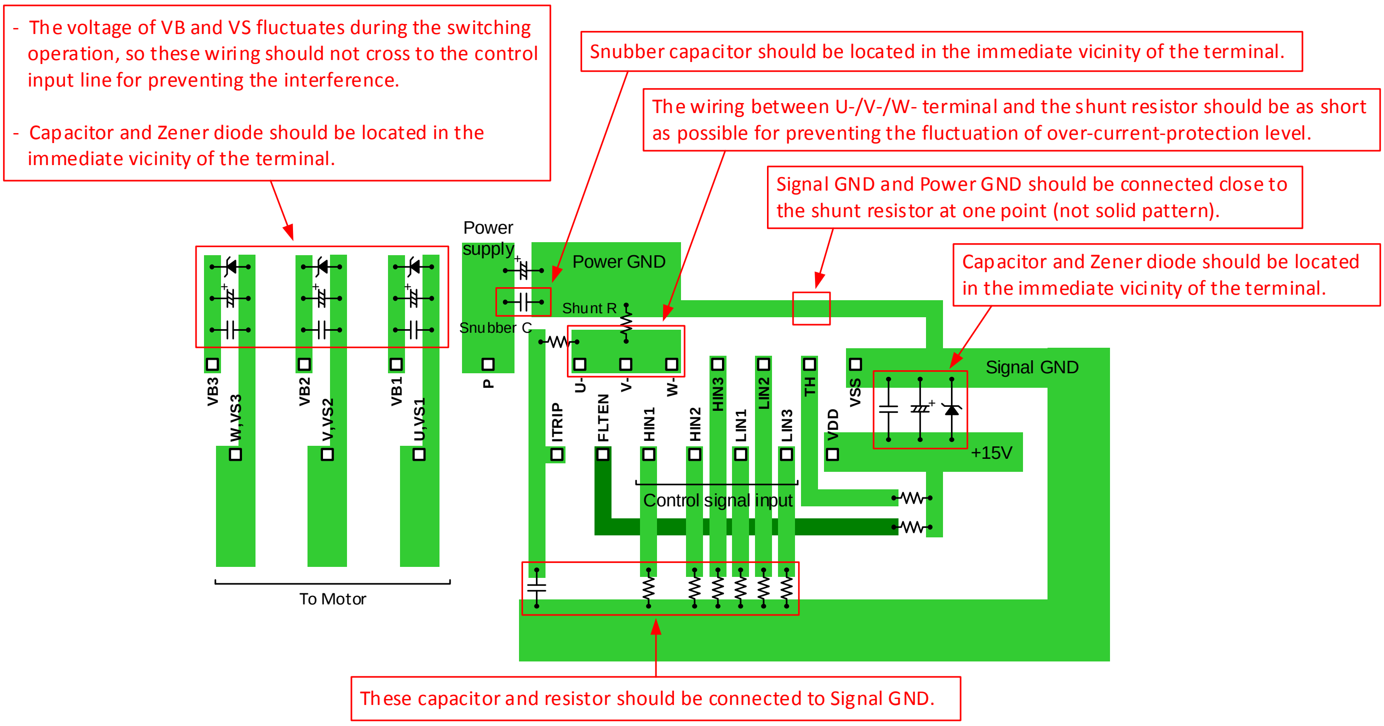


Figure 18. Recommended layout

5.2. Pin by pin design and usage notes

This section provides pin by pin PCB layout recommendations and usage notes. A complete list of module pins is given in Chapter 6.

VP
NU, NV, NW

DC Power supply terminal for the inverter block. Voltage spikes could be caused by longer traces to these terminals due to the trace inductance, therefore traces are recommended to be as short as possible. In addition a snubber capacitor should be connected as close as possible to the VP terminal to stabilize the voltage and absorb voltage surges.

U, V, W

These are the output pins for connecting the 3-phase motor. They share the same GND potential with each of the high-side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD, GND

These pins provide power to the low-side gate drivers, the protection circuits and the bootstrap circuits. The voltage between these terminals is monitored by the UVLO circuit. The GND terminal is the reference voltage for the input control signals.

VBU, VBV
VBW

The VBx pins are internally connected to the positive supply of the high-side drivers. The supply needs to be floating and electrically isolated. The bootstrap circuit shown in Figure 19 forms this power supply individually for every phase. Due to integrated boot resistor and diode (RB & DB) only an external boot capacitor (CB) is required.

CB is charged when the following two conditions are met.

① Low-side signal is input

② Motor terminal voltage is low level

The capacitor is discharged while the high-side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high-side and the switching frequency into account.

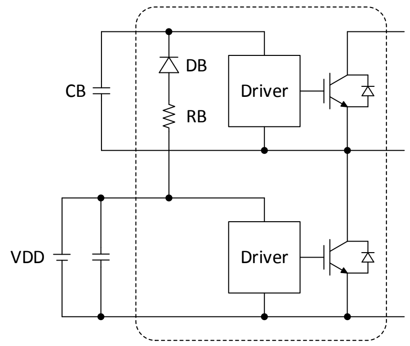


Figure 19. Bootstrap Circuit

The voltages on the high-side drivers are individually monitored by the under voltage protection circuit. If there is a UVLO fault on any given phase, the output on that phase is disabled.

Typically a CB value of less or equal 47 μF (±20%) is used. If the CB value needs to be higher, an external resistor (20 Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.

HINU, LINU
HINV, LINV
HINW, LINW

These pins are the control inputs for the power stages. The inputs on HINU/HINV/HINW control the high-side transistors of U/V/W, the inputs on LINU/LINV/LINW control the low-side transistors of U/V/W respectively. The input logic is active HIGH. An external microcontroller can directly drive these inputs without need for isolation.

Simultaneous activation of both low-side and high-side is prevented internally to avoid shoot-through at the power stage. However, due to IGBT switching delays the control signals must include a dead-time.

The equivalent input stage circuit is shown in Figure 20.

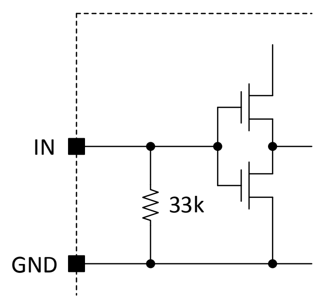


Figure 20. Internal Input Circuit

For fail safe operation the control inputs are internally tied to GND via a 33 kΩ (typ) resistor. An additional external low-ohmic pull-down resistor with a value of 2.2 kΩ - 3.3 kΩ is recommended to prevent erroneous switching caused by noise induced in the wiring. The output might not respond when the width of the input pulse is less than 1 µs (both ON and OFF).

FLTEN

This pin serves both as an enable input and an active low fault output (open-drain). It is used to indicate an internal fault condition of the module and also can be used to disable the module operation. The gate driver operates when the voltage of this pin is at 2.5 V or more, and stops at 0.8 V or less. The I/O structure is shown in Figure 21.

The internal sink current IoSD during an active fault is nominal 2 mA @ 0.1 V. Depending on the interface supply voltage the external pull-up resistor (RP) needs to be selected as shown below.

For the commonly used supplies :
Pull up voltage = 15 V -> RP >= 20 kΩ
Pull up voltage = 5 V -> RP >= 6.8 kΩ

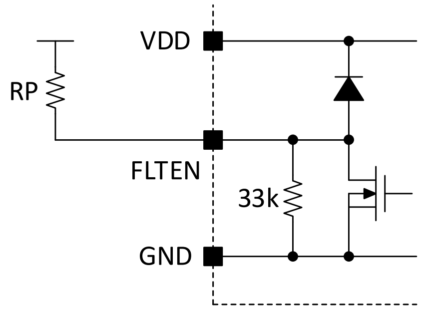


Figure 21. FLTEN Connection

For a detailed description of the fault operation refer to Chapter 4.

Note: The Fault signal does not permanently latch. After the protection event ended and the fault clear time (min. 1 ms) passed, the module's operation is automatically re-started. Therefore the input needs to be driven low externally as soon as a fault is detected.

ITRIP

This pin is used to enable an OCP function. When the voltage of this pin exceeds a reference voltage, the OCP function operates. For details of the OCP operation refer to Chapter 4.

TH

An internal thermistor to sense the substrate temperature is connected between TH and GND. By connecting an external pull-up resistor and measuring the midpoint voltage, the module temperature can be monitored. Please refer to heading 3.2 for details of the thermistor.

Note: This is the only means to monitor the substrate temperature indirectly.

5.3. Heat sink mounting and torque

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts IPM.
   - There must be no contamination on the heat sink surface that contacts IPM.

2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount IPM on a heat sink. If the device is removed, grease must be applied again.

3. For a good contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack.

The standard heat sink mounting condition of the STK534U3xx series is as follows.

Item	Recommended Condition
Pitch	40.6 ±0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter : M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer The size is D : 7 mm, d : 3.2 mm and t : 0.5 mm JIS B 1256
Heat sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM) : –50 to 100 µm Screw holes must be countersunk. No contamination on the heat sink surface that contacts IPM.
Torque	Temporary tightening : 20 to 30% of final tightening on first screw Temporary tightening : 20 to 30% of final tightening on second screw Final tightening : 0.6 to 0.9 Nm on first screw Final tightening : 0.6 to 0.9 Nm on second screw
Grease	Silicone grease. Thickness : 100 to 200 µm Uniformly apply silicone grease to whole back. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.

Table 5. Heat Sink Mounting

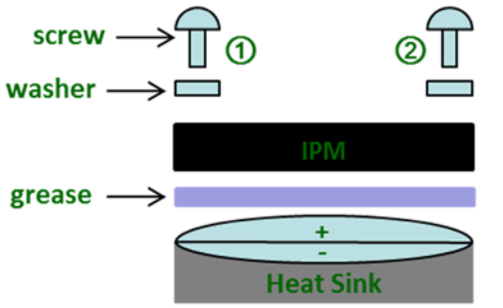


Figure 22. Mount IPM on a Heat Sink

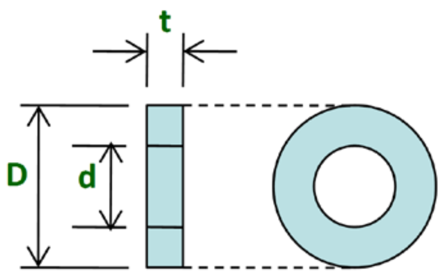


Figure 23. Size of Washer

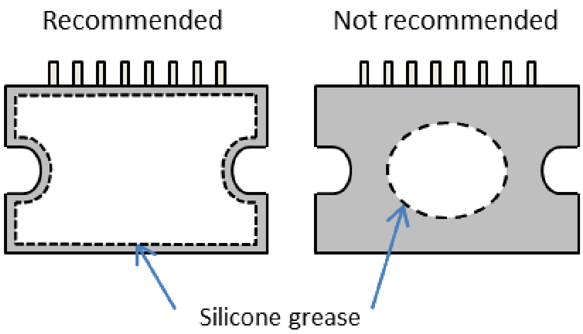


Figure 24. Uniform Application of Grease Recommended

Steps to mount an IPM on a heat sink
1st : Temporarily tighten maintaining a left/right balance.
2nd : Finally tighten maintaining a left/right balance.

5.4. Mounting and PCB considerations

In designs in which the PCB and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that slipping IPM is forcibly fixed to the heat sink with a screw.

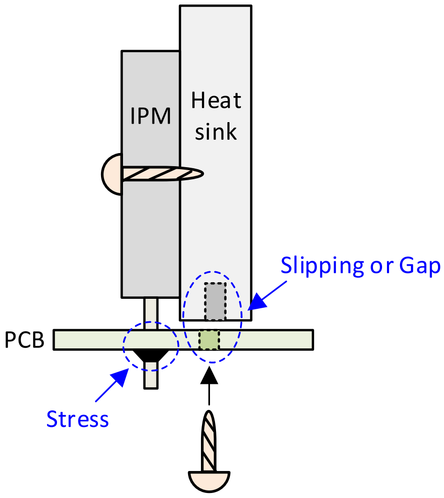
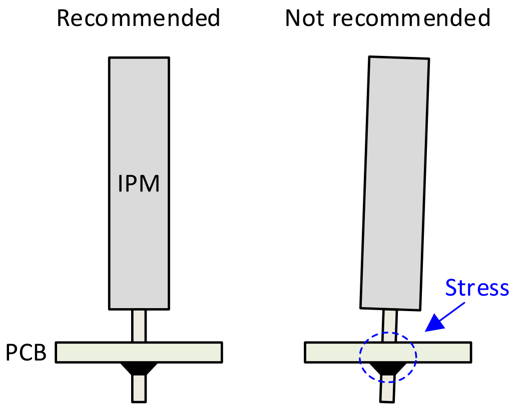


Figure 25. Fix to Heat Sink

Maintain a separation distance of at least 1.5 mm between the IPM case and the PCB. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the PCB.

Do not mount IPM with a tilted condition for PCB. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the PCB. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out.



Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

Mounting on a PCB

1. Align the lead frame with the holes in the PCB and do not use excessive force when inserting the pins into the PCB. To avoid bending the lead frames, do not try to force pins into the PCB unreasonably.
2. Do not insert IPM into PCB with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPMs may be destroyed or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

5.5. Cleaning

IPM has a structure that is unable to withstand cleaning. Do not clean independent IPM or PCBs on which an IPM is mounted

6. Package Outline

The package of STK534U3xx series is SIP05. (Single-inline-package)

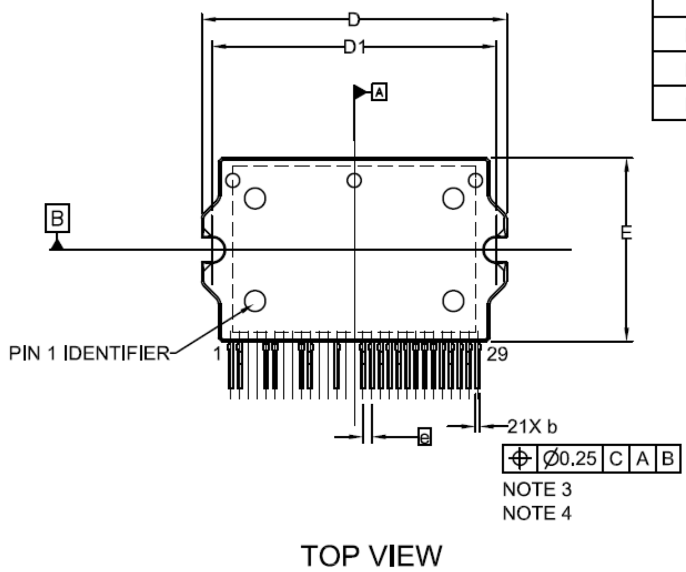
6.1. Package outline and dimension

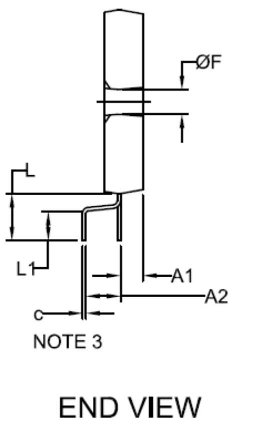
STK534U3xxC-E (SIP05 Vertical type)

SIP29 44X26.5 FP-3

NOTES:
1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP.
4. POSITION OF THE LEAD IS DETERMINED AT THE ROOT OF THE LEAD WHERE IT EXITS THE PACKAGE BODY.
5. PIN 1 IDENTIFICATION IS A MIRRORED SURFACE INDENT.
6. MISSING PINS ARE 3,4,7,8,11,12,14 AND 15.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	5.00	5.50	6.00
A1	2.70	3.20	3.70
A2	4.50	5.00	5.50
b	0.55	0.60	0.65
c	0.45	0.50	0.55
D	43.50	44.00	44.50
D1	40.50	41.00	41.50
E	26.00	26.50	27.00
e	1.27 BSC		
F	3.10	3.60	4.10
L	6.30	6.80	7.30
L1	3.80	4.30	4.80





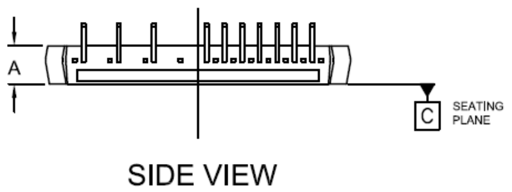


Figure 26. Package Outline

6.2. Pin Out Description

Pin	Name	Description
1	VBW	High Side Floating Supply voltage for W phase
2	W	W phase output Internally connected to W phase high side driver ground
5	VBV	High Side Floating Supply voltage for V phase
6	V	V phase output Internally connected to V phase high side driver ground
9	VBU	High Side Floating Supply voltage for U phase
10	U	U phase output Internally connected to U phase high side driver ground
13	VP	Positive PFC Output Voltage
16	ITRIP	Current protection pin for inverter
17	NU	Low Side Emitter Connection - Phase U
18	FLTEN	Bidirectional FAULT output and ENABLE input
19	NV	Low Side Emitter Connection - Phase V
20	HINU	Logic Input High Side Gate Driver - Phase U
21	NW	Low Side Emitter Connection - Phase W
22	HINV	Logic Input High Side Gate Driver - Phase V
23	HINW	Logic Input High Side Gate Driver - Phase W
24	LINU	Logic Input Low Side Gate Driver - Phase U
25	LINV	Logic Input Low Side Gate Driver - Phase V
26	LINW	Logic Input Low Side Gate Driver – Phase W
27	TH	Thermistor output
28	VDD	+15 V Main Supply
29	GND	Negative Main Supply

Note: Pins 3, 4, 7, 8, 11, 12, 14, 15 are not present.