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4 Key Steps to Design a NCL30288-Controlled LED Driver

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APPLICATION NOTE

This paper proposes the key steps to rapidly design a NCL30288-driver buck-boost converter to power an LED string. The process is illustrated by a practical 10-W, universal mains application:

- Maximum Output Power: 18 W
- Power Factor: 0.95 min
- Total Harmonic Distortion: 10% max
- Input Voltage Range: 90 to 265 V rms
- Output Voltage Range: 90 to 180 V dc
- Output Current: 100 mA ±2%
- Startup Time: < 500 ms

In applications where there is a need for insulation, one must design a flyback converter instead of a non-isolated buck-boost one. This application also discusses the few specificities of the design procedure in the case of an isolated LED driver.

INTRODUCTION

The NCL30288 is a TSOP−6 driver for power-factor corrected flyback and non-isolated buck-boost converters. The current-mode, quasi-resonant architecture optimizes the efficiency by turning on the MOSFET when the drain-source voltage is minimal (valley). At high line, the circuit delays the MOSFET turn-on until the second valley is detected to reduce switching losses. An internal proprietary circuitry controls the input current in such a way that a power factor as high as 0.99 is typically obtained together with an output current deviation below ±2%. In this application, there is no need for a secondary-side feedback driving an optocoupler. The circuit further contains a suite of powerful protections to ensure a robust LED driver design without the need for extra components or overdesign. Among them, one can list:

- *Cycle-by-Cycle Peak Current Limit:* when the current sense voltage exceeds the internal threshold (V_{ILIM}), the MOSFET immediately turns off (cycle-by-cycle current limitation).
- *Winding and Output Diode Short-circuit Protection (WODSCP):* an additional comparator stops the controller if the CS pin voltage exceeds (150% · V_{ILIM}) for 4 consecutive cycles. This feature can protect the converter if a winding or the output diode is shorted or simply if the transformer saturates.
- *Output Short-circuit Protection:* If the ZCD pin voltage remains low for a 90-ms time interval, the controller stops pulsating until 4 seconds have elapsed.
- *Open LED Protection:* if the V_{CC} pin voltage exceeds the OVP threshold (26.8 V typically), the controller shuts down and waits 4 seconds before restarting the switching operation (auto-recovery mode). In addition, a programmable OVP makes the NCL30288 enter the auto-recovery mode if the CS/ZCD pin voltage happens to exceed 4.5 V for 4 consecutive switching cycles. A 1-μs blanking time (after the ZCD blanking time) is implemented to reduce the risk of false detection on noise.
- *Floating/Short Pin Detection:* the circuit can detect most of these situations which helps pass safety tests.

NCL30288 DUTY RATIO LIMIT

The NCL30288 duty-ratio is internally limited to 60% at the top of the lowest line sinusoid. Practically, this leads the output voltage to fulfill below requirements:

- Non-isolated Converters:

$$V_{out} + V_f \leq \frac{3}{2} \cdot \sqrt{2} \left(V_{in,rms}\right)_{LL} \quad \text{(eq. 1)}$$

- Flyback Applications:

$$V_{out} + V_f \leq \frac{n_S}{n_P} \cdot \frac{3}{2} \cdot \sqrt{2} \left(V_{in,rms}\right)_{LL} \quad \text{(eq. 2)}$$

Where $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (85 or 90 V rms in general) and V_f is the output diode forward voltage (about 1 V). In the flyback case, the turns ratio provides some flexibility.

As an example, let's assume that we must design a 90- to 265-V rms, non-isolated buck-boost converter whose output can be as high as 150 V. In this case, Equation 1 condition is met since:

$$\frac{3}{2} \cdot \sqrt{2} \left(V_{in,rms}\right)_{LL} = \frac{3}{2} \cdot \sqrt{2} \cdot 90 \cong 191\ V \geq V_{out} + V_f \cong 150\ V \quad \text{(eq. 3)}$$

It would not be the case if the output voltage could reach 200 V since:

$$\frac{3}{2} \cdot \sqrt{2} \left(V_{in,rms}\right)_{LL} = \frac{3}{2} \cdot \sqrt{2} \cdot 90 \cong 191 \text{ V} < V_{out} + V_f \cong 200 \text{ V} \quad \text{(eq. 4)}$$

In such a case, the flyback architecture would be a better option since:

$$\frac{n_S}{n_P} \cdot \frac{3}{2} \cdot \sqrt{2} \left(V_{in,rms}\right)_{LL} \cong \frac{n_S}{n_P} \cdot 191 \geq V_{out} + V_f \cong 200 \text{ V} \quad \text{(eq. 5)}$$

If:

$$\frac{n_S}{n_P} \cdot 191 \geq 200 \text{ V} \quad \text{(eq. 6)}$$

That is, if:

$$\frac{n_S}{n_P} \geq 1.05 \quad \text{(eq. 7)}$$

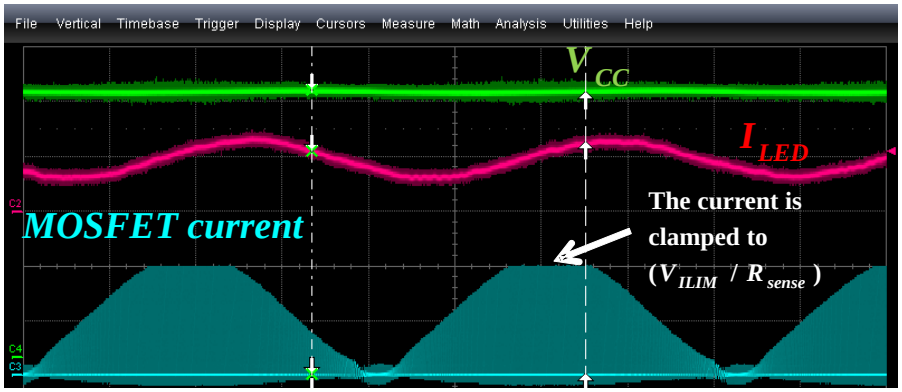


Figure 1. Current Over-Current Limitation (V_{ILIM} is the Cver-Current Threshold, R_{sense}, the Current Sense Resistor)

If the duty ratio limit is exceeded by your application, the LED current will be below its nominal value at the lowest line voltage but will meet the target when the input voltage level is sufficient to meet Equation 1 (for buck-boost converters) or Equation 2 (for flyback converters).

By the way, the typical symptom of the duty ratio limit effect is shown by Figure 1: the over-current limitation clamps the input current, causing the LED current to be less than expected.

LED DRIVER DIMENSIONING

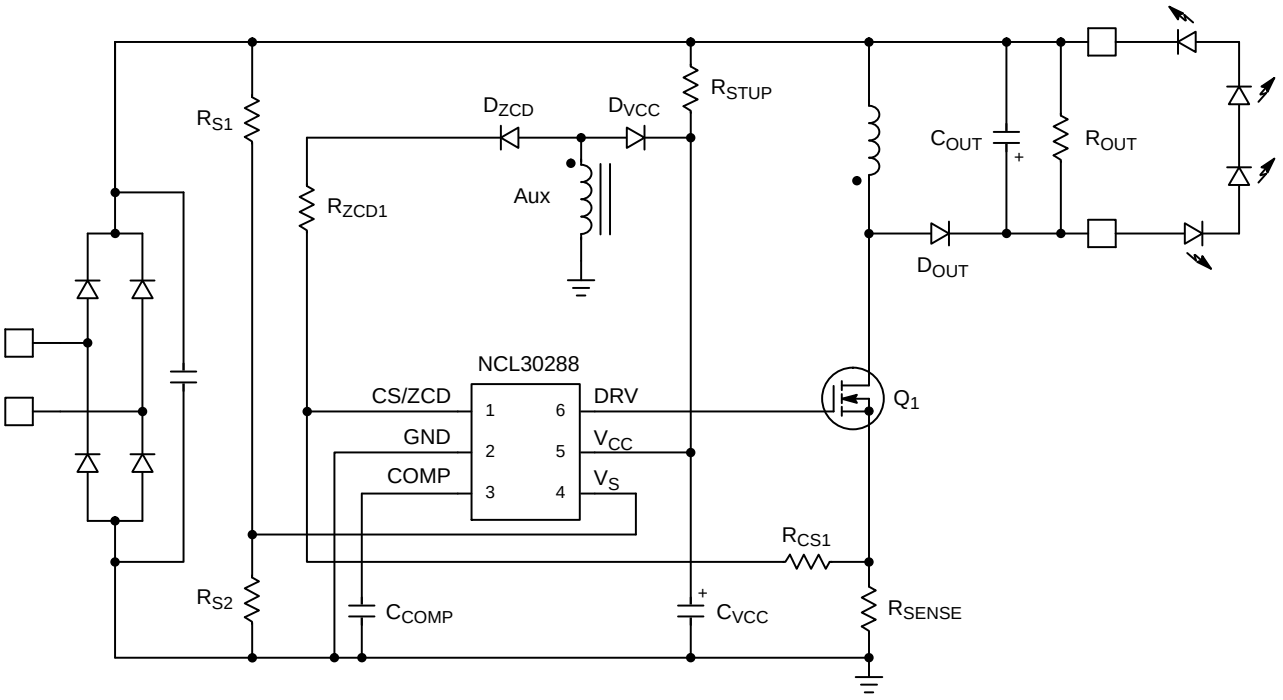


Figure 2. Basic Schematic − Buck-Boost LED Driver

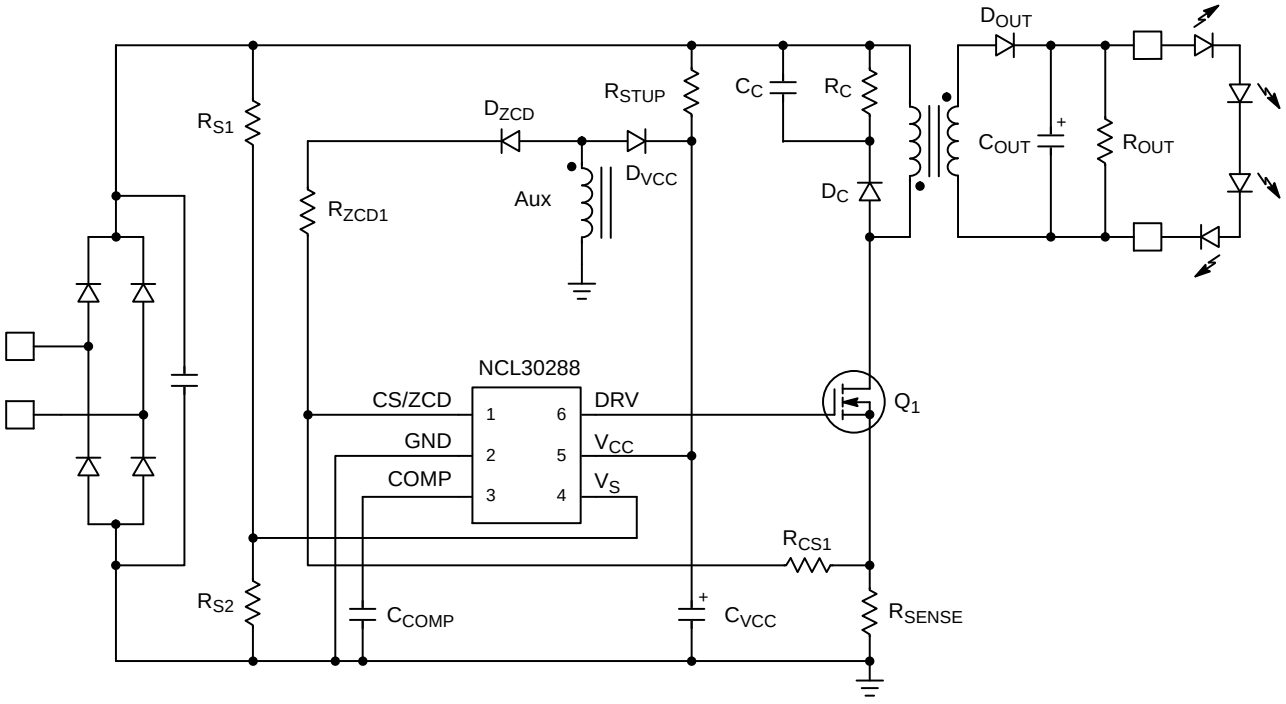


Figure 3. Basic Schematic − Flyback LED Driver

STEP 1: POWER COMPONENTS SELECTION

The power components dimensioning is not specific to the NCL30288 but common to traditional PF-corrected, quasi-resonant flyback or buck-boost converter. This chapter follows the methodology of application note AND9200/D [2].

Transformer Selection

Duty-ratio Considerations

As aforementioned, the NCL30288 duty ratio is internally limited to 60% at the top of the lowest line sinusoid. It is hence recommended to meet the following operating conditions:

- $V_{out} + V_f \le \frac{3\sqrt{2}}{2} \cdot \left(V_{in,rms}\right)_{LL}$ in the case of a non-isolated converter,
- $\frac{n_s}{n_p} \cdot \left(V_{out} + V_f\right) \le \frac{3\sqrt{2}}{2} \cdot \left(V_{in,rms}\right)_{LL}$ in the case of a flyback application.

Where $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (85 or 90 V rms in general), V_f is the output diode forward voltage, n_P is the primary winding number of turns and n_S is the secondary winding number of turns.

In the case of a non-isolated converter, the maximum output voltage must hence remain less than

$$\left(\frac{3\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{2} - V_f\right)$$

for optimal operation. If not, the output current will be slightly below target at the lowest line levels.

In the case of an isolated converter, the turns ratio provides some flexibility as the condition of using is met if:

$$\frac{n_P}{n_S} \le \frac{3}{2} \cdot \frac{\sqrt{2}\left(V_{in,rms}\right)_{LL}}{V_{out,max} + V_f} \qquad \text{(eq. 8)}$$

As an example, let's assume that we must design a 90 to 265 V rms. In the case of a non-isolated buck-boost converter, the output voltage should not exceed:

$$V_{out} \le \frac{3\sqrt{2}}{2} \cdot \left(V_{in,rms}\right)_{LL} - V_f \cong \frac{3\sqrt{2}}{2} \cdot \left(V_{in,rms}\right)_{LL} = \frac{3\sqrt{2}}{2} \cdot 90 \cong 191\ V \qquad \text{(eq. 9)}$$

In the flyback converter case, a higher output voltage can be obtained. For instance, if a maximum output voltage of 250 V is targeted, Equation 8 leads to the following constraint on the turns ratio (assuming V_f is 1 V):

$$\frac{n_P}{n_S} \le \frac{3}{2} \cdot \frac{\sqrt{2}\left(V_{in,rms}\right)_{LL}}{V_{out,max} + V_f} \cong \frac{3}{2} \cdot \frac{\sqrt{2} \cdot 90}{250 + 1} \cong 0.76 \qquad \text{(eq. 10)}$$

Selecting the Auxiliary Winding Number of Turns

An auxiliary winding is necessary for zero current detection and to provide the V_{CC} voltage. The output voltage of a LED driver generally exhibits a large range. The V_{CC} voltage provided by the auxiliary winding will vary similarly. The NCL30288 features a large V_{CC} range to address these variations. Practically, after start-up, the operating range is 9.4 V up to 25.5 V.[1]

The auxiliary winding number of turns can be selected so that the auxiliary voltage is slightly below $(V_{CC(OVP)})_{min}$ when the output voltage is at a maximum factoring in the 100/120-Hz ripple. Practically, this criterion turns into:

$$\frac{n_{AUX}}{n_S} \cdot \left(V_{out,max} + V_f\right) \le \left(V_{CC(OVP)}\right)_{min} + V_D \qquad \text{(eq. 11)}$$

Hence:

$$\frac{n_S}{n_{AUX}} \ge \frac{V_{out,max} + V_f}{\left(V_{CC(OVP)}\right)_{min} + V_D} \qquad \text{(eq. 12)}$$

Where V_f and V_D are the forward voltage of respectively, the output diode and of the diode providing V_{CC} from the auxiliary winding (D_{VCC} of Figure 2).

Taking some margin on the output voltage (200 V instead of 180 V to take into account the 100- or 120-Hz ripple), the above equation leads in our case to:

$$\frac{n_S}{n_{AUX}} \ge \frac{200 + 1}{25.5 + 0.65} \cong 7.7 \qquad \text{(eq. 13)}$$

Practically, we will select ($n_s = 8 \cdot n_{AUX}$).

In this case, V_{CC} will be in the range of

$$\left(\frac{V_{out,min} + V_f}{8} - V_D\right),$$

with some deviations due to the imperfect coupling. Note that at the lowest output voltage level (90 V), V_{CC} will be in the range of

$$\left(\frac{90 + 1}{8} - 0.65 \simeq 10.7\ V\right)$$

which is sufficient to properly feed the NCL30288.

Selecting the Secondary to Primary Transformer Turns Ratio (Flyback)

In general, N_{SP}, the primary to secondary transformer turns ratio ($N_{sp} = n_P / n_S$) [2] is selected as high as possible so that the input current stress is reduced. Now, N_{SP} cannot be too large for two reasons. First Equation 8 describes the limitation due to the NCL30288 duty ratio range. In addition, the higher N_{SP}, the larger the voltage reflected into the primary side during the off-time (see Figure 4). Hence, N_{SP} must be low enough to limit the voltage stress across the primary-side MOSFET. Indeed, the voltage to be sustained by the primary-side MOSFET and the output diode are:

1. $(V_{CC(OVP)})_{min}$ = 25.5 V is the threshold minimum value of the V_{CC} over-voltage protection. This safety feature protects the circuit if the LED string happens to be disconnected.
2. n_P denotes the primary number of turns, n_S, the secondary number of turns.

$$V_{DS,max} = \sqrt{2}\left(V_{in,rms}\right)_{max} + N_{SP}\left(V_{out} + V_f\right) + V_{Q-ov}$$

$$V_{Diode,max} = \frac{\sqrt{2}\left(V_{in,rms}\right)_{max}}{N_{SP}} + V_{out} + V_f + V_{D-ov} \quad \text{(eq. 14)}$$

Where:

- N_{SP} is the primary to secondary transformer turns ratio ($N_{sp} = n_p / n_s$).
- V_{Q-ov} is the MOSFET overvoltage caused by the leakage inductance reset (see Figure 4). This overshoot is limited by the clamping network consisting of D_C, C_C and R_C of Figure 2.
- V_{D-ov} is a similar overshoot that occurs across the output diode when the MOSFET turns on.

The clamping network is often designed so that V_{Q-ov} is between 50% and 100% of the reflected voltage:

$$V_{Q-ov} = k_c \cdot \frac{V_{out} + V_f}{N_{PS}} \text{ with } 0.5 \le k_c \le 1.0 \quad \text{(eq. 15)}$$

We can estimate the maximum voltage reached on the drain node, considering $V_{out(OVP)}$ level as the maximum output voltage:

$$V_{ds,max} = \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} + \frac{(1 + k_c)\left(V_{out(OVP)} + V_f\right)}{N_{PS}} \quad \text{(eq. 16)}$$

Some derating is generally requested. The typically-applied 15-% safety factor implies that the MOSFET voltage does not exceed 85% of its breakdown voltage. Hence:

$$V_{ds,max} = \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} + \frac{(1 + k_c)\left(V_{out(OVP)} + V_f\right)}{N_{PS}} \le 85\%\, V_{DSS} \quad \text{(eq. 17)}$$

Where V_{DSS} is the MOSFET breakdown voltage.

Finally:

$$\frac{n_P}{n_S} \le \frac{85\%\, V_{DSS} - \sqrt{2}\left(V_{in,rms}\right)_{HL}}{(1 + k_c)\left(V_{out(OVP)} + V_f\right)} \quad \text{(eq. 18)}$$

When selecting (n_P / n_S), recall that this ratio must also meet the Equation 8. So, it can be expressed as follows:

$$\frac{n_P}{n_S} \le \min\left[\frac{3}{2} \cdot \frac{\sqrt{2}\left(V_{in,rms}\right)_{LL}}{V_{out,max} + V_f}; \frac{85\%\, V_{DSS} - \sqrt{2}\left(V_{in,rms}\right)_{HL}}{(1 + k_c)\left(V_{out(OVP)} + V_f\right)}\right] \quad \text{(eq. 19)}$$

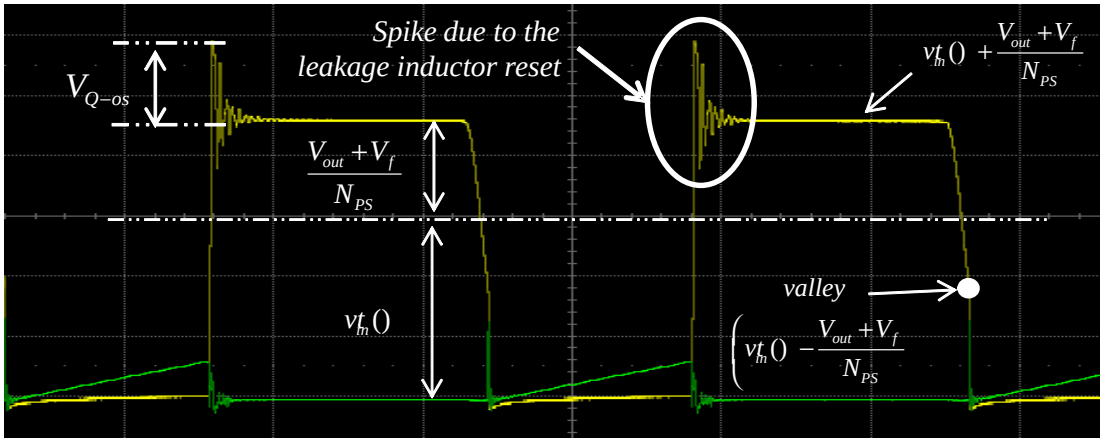


Figure 4. MOSFET Drain-source Voltage (Yellow Trace) and Current (Blue)

Selecting the Primary Inductance

Assuming a quasi−resonant operation and neglecting the small delay necessary for detecting the MOSFET drain-source valley, the primary inductance dictates the switching frequency as follows:

$$f_{SW}(t) = \frac{\left(V_{in,rms}\right)^2}{2\, L_p\, P_{in,avg}} \cdot \left[\frac{V_{out} + V_f}{\frac{n_S \cdot v_{in}(t)}{n_P} + V_{out} + V_f}\right]^2 \quad \text{(eq. 20)}$$

The switching frequency is a rising function of the rms line voltage. At a given line magnitude, the switching frequency is yet higher near the line zero crossing and decays as the line voltage rises due to the ($v_{in}(t)$) term.

Note that when high-line conditions are detected[3], the NCL30288 does not operate in quasi-resonant mode but delays the MOSFET turn on until the 2nd valley is detected (see Figure 5). This reduces the switching frequency upper range and optimizes the high-line efficiency.

3. The input voltage is sensed by the V_S pin for brown-out protection, feedforward and line range detection. High-line conditions are detected when the V_S pin voltage exceeds 2.0 V typically. See data sheet for more details.

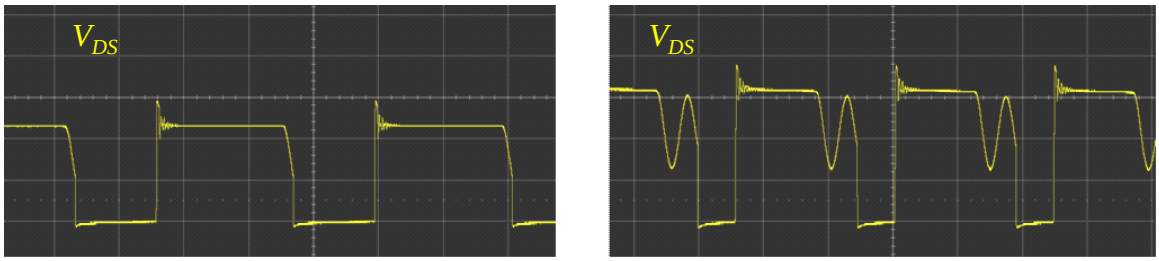


Figure 5. Quasi-resonant Mode in Low Line (Left), Turn On at Valley 2 when in High Line (Right)

The primary inductor will be selected with respect to the targeted switching frequency range, keeping in mind that:

- High switching frequency levels reduce the size of the storage elements.
- Conversely, increasing the switching frequency leads to more switching noise and losses. Also, EMI filtering is tougher since the switching generates higher EMI at the switching frequency and close harmonic levels. Most power supplies have to meet standards which apply to frequencies above 150 kHz. That is why SMPS designers often select F_{SW} = 130 kHz to keep the fundamental component below 150 kHz and then out of the regulation scope. Even more often, 65 kHz is also chosen to avoid damping harmonic 2.

As the rule of thumb, let us select L_P as follows:

- In wide-mains applications: choose L_P so that the switching frequency is below 130 kHz at the low-line range nominal voltage (typically 115 V rms) over a large part of the sinusoid. Practically, we can decide to meet this target starting from ($V_{in,pk}$ / 2) that is ($\sqrt{2} \cdot 115 / 2$) to the line peak. This arbitrary choice relies on the idea that for below this line voltage level the input current is relatively small and easier to filter. Check that at the high-line nominal voltage (230 V rms typically), the switching frequency stays below 130 kHz thanks to the valley-2 operation.
- Similarly, in a narrow mains operation case, select L_P so that the switching frequency is below 65 kHz at the nominal line voltage when ($v_{in}(t)$ = $V_{in,pk}$ / 2).

Our application is a wide-range one. Let us compute L_P so that at 115 V rms, the switching frequency is below $f_{sw,T}$ = 130 kHz:

$$L_p \geq \frac{\left(V_{in,rms}\right)^2}{2\, f_{SW,T}\, P_{in,avg}} \cdot \left(\frac{V_{out} + V_f}{\frac{n_S}{n_p} \cdot \frac{\sqrt{2} \cdot V_{in,rms}}{2} + V_{out} + V_f} \right)^2 \quad \text{(eq. 21)}$$

Which leads to:

$$L_p \geq \frac{115^2}{2 \cdot 130 \cdot 10^3 \cdot 20} \cdot \left(\frac{180 + 1}{\frac{1}{1} \cdot \frac{\sqrt{2} \cdot 115}{2} + 180 + 1} \right)^2 \quad \text{(eq. 22)}$$

$$\cong 1.2\ \text{mH}$$

Finally we have to consider the primary current magnitude constraints:

$$\left(I_{L,pk}\right)_{max} = 2\sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \left(1 + \frac{n_S \sqrt{2} \left(V_{in,rms}\right)_{LL}}{n_P \left(V_{out} + V_f\right)} \right) \quad \text{(eq. 23)}$$

$$\left(I_{L,pk}\right)_{max} = \frac{2}{\sqrt{3}} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \quad \text{(eq. 24)}$$

$$\cdot \sqrt{1 + \frac{16\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{3\pi \cdot \frac{n_P \left(V_{out} + V_f\right)}{n_S}} + \frac{6\pi \cdot \left(V_{in,rms}\right)_{LL}^2}{4 \cdot \left(\frac{n_P \left(V_{out} + V_f\right)}{n_S} \right)^2}}$$

In our application, Equation 23 and Equation 24 lead to:

$$\left(I_{L,pk}\right)_{max} = 2\sqrt{2} \cdot \frac{20}{90} \cdot \left(1 + \frac{\sqrt{2} \cdot 90}{180 + 1} \right) \cong 1.07\ \text{A} \quad \text{(eq. 25)}$$

$$\left(I_{L,pk}\right)_{max} = \frac{2}{\sqrt{3}} \cdot \frac{20}{90} \cdot \sqrt{1 + \frac{16\sqrt{2} \cdot 90}{3\pi \cdot 181} + \frac{6\pi \cdot 90^2}{4 \cdot 181^2}} \quad \text{(eq. 26)}$$

$$\cong 470\ \text{mA}$$

We selected transformer 750314731 from Wurth Elektronik with the following characteristics:

$$L_P = 1.25\ \text{mH},\ \frac{n_S}{(n_{AUX})} = 8.$$

Power Switches

MOSFET:

The voltage constraints on the MOSFET were expressed by Equation 14. In the buck-boost case, this equation simplifies as N_{SP} is 1 and that the turn-off overshoot (V_{Q-ov}) is small. Thus,

$$V_{DC,max} \cong \sqrt{2} \left(V_{in,rms}\right)_{max} + \left(V_{out} + V_f\right) \quad \text{(eq. 27)}$$

In application, the maximum drain-source voltage in nominal operation is:

$$V_{DC,max} \cong \sqrt{2} \cdot 265 + (180 + 1) \cong 555\ \text{V} \quad \text{(eq. 28)}$$

Conduction losses depend on the MOSFET rms current which can be computed with the following equation:

$$\left(I_{Q,rms}\right)_{max} = \frac{2}{\sqrt{3}} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \sqrt{1 + \frac{8\sqrt{2}\left(V_{in,rms}\right)_{LL}}{3\pi \cdot \frac{n_P\left(V_{out}+V_f\right)}{n_S}}} \quad \text{(eq. 29)}$$

A STU8N80K MOSFET is selected (IPAK, 800 V, 0.95 Ω).

Output Diode:

The voltage the output voltage must be able to face, has been discussed in the previous section and expressed by Equation 14. In our case, we have

$$V_{diode,max} \cong \sqrt{2}\left(V_{in,rms}\right)_{max} + V_{out,max} + V_f + V_{D-ov} \quad \text{(eq. 30)}$$

Which leads to:

$$V_{diode,max} \cong \sqrt{2} \cdot 265 + 180 + 1 + V_{D-ov} \quad \text{(eq. 31)}$$
$$\cong 555 + V_{D-ov}$$

Where V_{D-ov} is the overshoot across the output diode when the MOSFET turns on.

Losses are mainly produced by the average current flowing through the diode. This average is simply the LED current (0.1 A in our case).

A 800-V, 1-A SMA Ultrafast diode is selected (US1K from MCC).

Snubber

A snubber capacitor or a R, C network can be placed across the MOSFET and/or the output diode to reduce the dV/dt and lower the switching noise.

Clamping Network (Flyback Only)

When the MOSFET turns off, the magnetizing inductor energy is conveyed to the secondary side and charges the output. In contrast, the leakage inductance current cannot be transferred to the output and it must be diverted from the MOSFET. If not, the MOSFET drain-source voltage would rise to destructive levels. A clamping network is hence necessary. Such a circuit requires a diode, a resistor and a capacitor (D_C, R_C and C_C of Figure 3):

- The capacitor C_C absorbs the leakage inductance energy when the MOSFET turns off. This capacitor must sustain the voltage difference between the MOSFET drain and the input voltage rail. The voltage rating of this capacitor is typically the MOSFET breakdown voltage minus the highest input voltage, or higher.
- The resistor R_C loads C_C to ensure that the C_C voltage does not drift up but stabilize at a level which ensures a proper MOSFET protection (the MOSFET voltage is clamped to the input voltage + the C_C voltage by means of D_C).
- The diode D_C prevents C_C from discharging when the MOSFET turns on. This diode is generally a fast-recovery diode. A low-value resistor (R_0 of the "Flyback Option" tab in [5]) is inserted to limit the current spike which otherwise occurs when the MOSFET turning off, C_C abruptly charges. Do not oversize this series resistor. The leakage current flowing through it creates a voltage drop.
The MOSFET voltage is clamped to the C_C voltage ***PLUS*** the series resistor voltage. In our case, the maximum leakage current is (V_{ILIM} / R_{sense}) that is (1 V / 1.2 Ω ≅ 833 mA). For instance, a 22-Ω resistor would result in a maximum overshoot of (22 Ω · 0.833 ≅ 18 V).

Equation 16 gives the maximum voltage

$$\left(\sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} + \frac{(1 + k_c)\left(V_{out(OVP)} + V_f\right)}{N_{PS}}\right)$$

the MOSFET must sustain where:

$$\left(\frac{(1 + k_c)\left(V_{out(OVP)} + V_f\right)}{N_{PS}}\right)$$

is the maximum C_C voltage, k_C being the clamping network voltage coefficient (which defines the portion of the reflected voltage used to discharge the leakage inductor).

From this, we can deduce:

- $V_{DS,max}$ being the maximum acceptable MOSFET drain-source voltage considering the necessary derating factor (e.g., 700 V for a 800-V MOSFET), k_C must keep below:

$$k_{C,max} = \frac{N_{PS}\left(V_{DS,max} - \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}\right)}{V_{out(OVP)} + V_f} - 1 \quad \text{(eq. 32)}$$

  Where N_{PS} is the secondary to primary transformer turns ratio ($N_{PS} = n_S / n_P$).

  In practice, selecting k_c equal or slightly below $k_{c,max}$ is a good choice since this selection leads to the R_C smallest dissipation. Following calculations will be made with ($k_c = k_{c,max}$).
- The maximum energy to be consumed by R_C over a switching cycle is given by:

$$E_{R_C} = \frac{\left(\frac{\left(1+k_{c,max}\right)\left(V_{out(OVP)}+V_f\right)}{N_{PS}}\right)^2 \cdot T_{SW}}{R_C} \quad \text{(eq. 33)}$$

The energy absorbed by C_C because of the leakage inductance is:

$$E_{L_{leak}} = \frac{1}{2} L_{leak} \cdot I_{in,pk}^{2} \cdot \frac{\frac{(1+k_{c,max})\left(V_{out(OVP)}+V_f\right)}{N_{PS}}}{\frac{(1+k_{c,max})\left(V_{out(OVP)}+V_f\right)}{N_{PS}} - \frac{\left(V_{out(OVP)}+V_f\right)}{N_{PS}}} = \frac{1 + k_{c,max}}{2 \cdot k_{c,max}} \cdot L_{leak} \cdot I_{in,pk}^{2} \quad \text{(eq. 34)}$$

Where $I_{in,pk}$ is the peak MOSFET current obtained at the line sinusoid top.

The energy of Equation 33 must be equal or slightly higher than the leakage inductor energy defined in Equation 34. From this, we can deduce the following minimum R_C value:

$$R_C \le \frac{(1 + k_{c,max}) \cdot \left(\frac{\left(V_{out(OVP)}+V_f\right)}{N_{PS}}\right)^2}{\frac{1}{2 \cdot k_{c,max}} \cdot L_{leak} \cdot I_{in,pk}^{2} \cdot f_{SW}} \quad \text{(eq. 35)}$$

For $I_{in,pk}$, we can use the maximal value it can take when over-current protection trips, that is,(V_{ILIM} / R_{sense}) where V_{ILIM} is the over-current protection threshold and R_{sense}, the current sense resistor. Note however, this value is not very practical at very high line where the constant current loop limits it to a much lower value. Thus, using (V_{ILIM} / R_{sense}) may lead to an excessively low R_C and hence, a stronger and more dissipative clamp than needed. Also, the switching frequency term significantly influences R_C computation.

Now, following Equations 20 and 23, we can more precisely deduce the peak current and the switching frequency at the top of the input sinusoid when both the input and output voltages are maximal:

$$I_{in,pk} = 2\sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{HL}} \cdot \left(1 + \frac{n_S \sqrt{2}\left(V_{in,rms}\right)_{HL}}{n_P\left(V_{out(OVP)} + V_f\right)}\right) \quad \text{(eq. 36)}$$

$$f_{SW}(t) = \frac{\left(V_{in,rms}\right)_{HL}^{2}}{2\, L_p \left(P_{in,avg}\right)_{max}} \cdot \left(\frac{V_{out(OVP)} + V_f}{\frac{n_S \cdot \sqrt{2}\left(V_{in,rms}\right)_{HL}}{n_P} + V_{out(OVP)} + V_f}\right)^2 \quad \text{(eq. 37)}$$

And compute the term ($I_{in,pk}^2 \cdot f_{SW}$) of Equation 35 when both the input and output voltages are maximal. It comes:

$$I_{in,pk}^{2} \cdot f_{SW} = \frac{4 \cdot P_{in,avg}}{L_P} \quad \text{(eq. 38)}$$

Hence, Equation 35 simplifies as follows:

$$R_C \le \frac{n_P^{2}}{2 \cdot n_S^{2}} \cdot k_{c,max} \cdot (1 + k_{c,max}) \cdot \frac{L_P}{L_{leak}} \cdot \eta \cdot \left(\frac{V_{out(OVP)} + V_f}{I_{out}}\right) \quad \text{(eq. 39)}$$

The R_C losses are:

$$P_{R_C} \le \frac{\left((1 + k_{c,max}) \cdot \frac{\left(V_{out(OVP)}+V_f\right)}{N_{PS}}\right)^2}{R_C} \quad \text{(eq. 40)}$$

Select the C_C capacitor so that the time constant ($R_C \cdot C_C$) is large compared to a switching period, practically, in the range of 1 ms.

Refer to [2] for a practical example.

Output Capacitor

The power delivered by PFC converters exhibits a large ac component at twice the line frequency. The output capacitor partly compensates for it but yet, the output current exhibits some ripple inversely proportional to the capacitor value (C_{out}).

Below equation expresses the current ripple:

$$\frac{\left(\Delta I_{out}\right)_{pk-pk}}{I_{out,nom}} = \frac{2}{\sqrt{1 + \left(4\pi \cdot f_{line} \cdot R_{LED} \cdot C_{out}\right)^2}} \quad \text{(eq. 41)}$$

From Equation 41, if a maximum ratio (peak-to-peak ripple) over (dc value)

$$\left(\frac{\left(\Delta I_{out}\right)_{pk-pk}}{I_{out,nom}}\right)_{max}$$

is specified for the output current, the following minimum value for C_{out} can be deduced :

$$C_{out,min} = \frac{\sqrt{\left[\frac{2}{\left(\frac{\left(\Delta I_{out}\right)_{pk-pk}}{I_{out,nom}}\right)_{max}}\right]^2 - 1}}{4\pi \cdot f_{line,min} \cdot R_{LED,min}} \quad \text{(eq. 42)}$$

C_{out} must then be large enough to avoid an excessive current ripple which could reduce the LED reliability. The flicker index is commonly specified below 0.15. This requirement corresponds to a 100% peak-to-peak ripple in a PF-corrected LED driver with a sinusoidal output current shape.

This criterion (100% peak to peak ripple), leads to:

$$\left(\frac{\left(\Delta I_{out}\right)_{pk-pk}}{I_{out,nom}}\right)_{max} = 1 \qquad \text{(eq. 43)}$$

In our application the minimum LED dynamic resistance is estimated to be 100 Ω and the minimum line frequency is 50 Hz. In this case, the minimum output capacitor value is:

$$C_{out,min} = \frac{\sqrt{\left(\frac{2}{1}\right)^2 - 1}}{2 \cdot 100\pi \cdot 100} \cong 27\ \mu F \qquad \text{(eq. 44)}$$

$$\left(I_{C,rms}\right)_{max} = \sqrt{\left[\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{n_P}{n_S}\right)^2 \cdot \frac{\left(P_{in,avq}\right)^2_{max}}{V_{in,rms} \cdot \frac{n_P \cdot \left(V_{out}+V_f\right)}{n_S}} \cdot \left[1 + \frac{9\pi^2}{16\sqrt{2}} \cdot \frac{V_{in,rms}}{\frac{n_P \cdot \left(V_{out}+V_f\right)}{n_S}}\right]\right] - I_{out,nom}{}^2} \qquad \text{(eq. 45)}$$

Considering the highest output voltage (hence higher power – 20 W input) and the lowest line level as the worst case, Equation 45 leads in our case to:

$$\left(I_{C,rms}\right)_{max} = \sqrt{\left(\frac{32\sqrt{2}}{9\pi} \cdot \frac{20^2}{90 \cdot 181} \cdot \left(1 + \frac{9\pi^2}{16\sqrt{2}} \cdot \frac{90}{181}\right)\right) - 0.1^2} \cong 330\ mA \qquad \text{(eq. 46)}$$

It remains wise to check the output capacitor heating in the lab.

Two paralleled 18-μF/250 V are implemented.

Bulk Capacitor Heating:

It must also be checked that the ESR is low enough to prevent the rms current that flows through it, from overheating the bulk capacitor. This capacitor rms current can be estimated using the following expression:

STEP 2: DRIVING THE V_S AND COMP PINS

A portion of the input voltage rail is to be applied to the V_S pin. The circuit uses this information to protect the LED driver in too low mains conditions (brown-out protection) and to optimize the operation over the line voltage range (line-feedforward and line-range detection functions).

This V_S pin voltage also provides the sinusoidal reference necessary for input current shaping (Power Factor Correction). A proprietary averaging process internally modulates the V_S current reference to provide the target output current.

The averaging process uses an internal Operational Trans-conductance Amplifier (OTA) and the capacitor connected to the COMP pin. Typical COMP capacitance is 1 μF and should not be less than 470 nF to ensure stability. The COMP ripple does not affect the power factor performance since the NCL30288 digitally eliminates it.

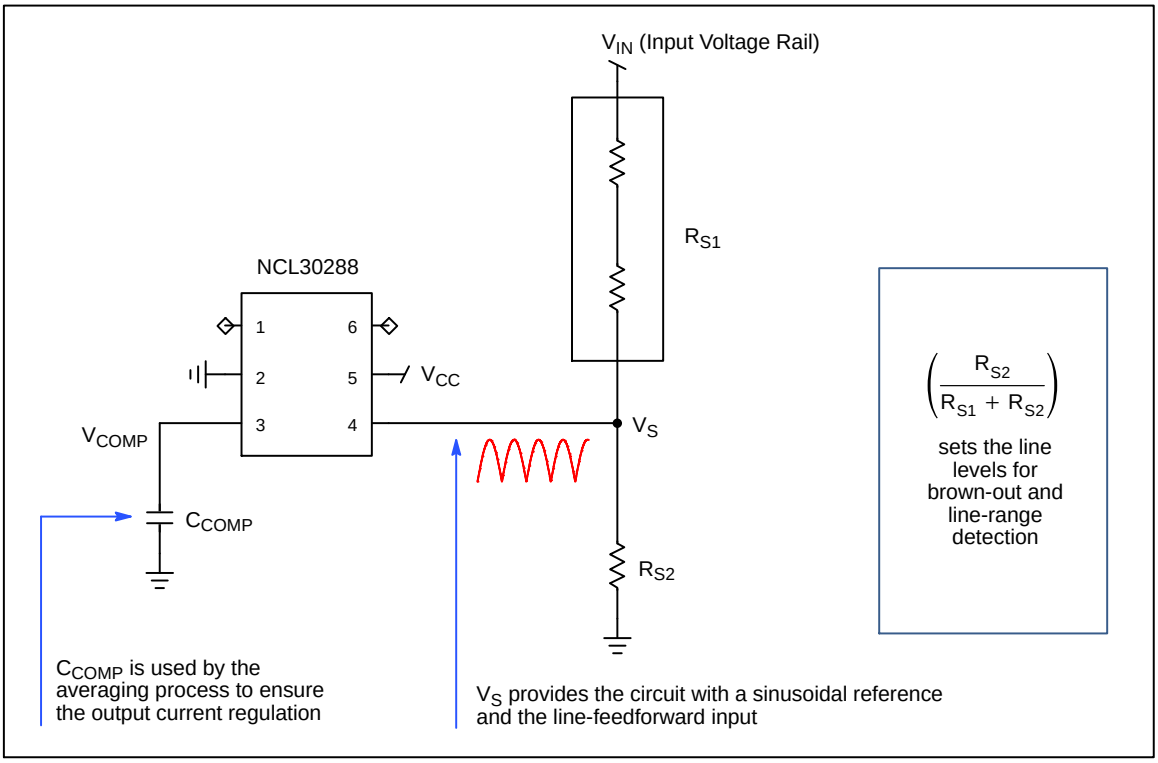


Figure 6. V_S and COMP Pin

Brown-Out Protection

The NCL30288 prevents operation when the line voltage is too low for proper operation. As shown by Figure 7, the circuit detects a brown-out situation if the V_S pin remains below the $V_{BO(off)}$ threshold (0.9 V typical) for more than the $t_{BO(blank)}$ blanking time (25 ms typically). In such a case, the controller stops operating. Operation resumes as soon as the V_S pin voltage exceeds $V_{BO(on)}$ (1.0 V typical) and V_{CC} is higher than $V_{CC(on)}$. To ease recovery, the circuit overrides the V_{CC} normal sequence (no need for V_{CC} cycling down below $V_{CC(off)}$). Instead, its consumption immediately reduces to $I_{CC(start)}$ so that V_{CC} rapidly charges up to $V_{CC(on)}$. Once done, the circuit re-starts operating.

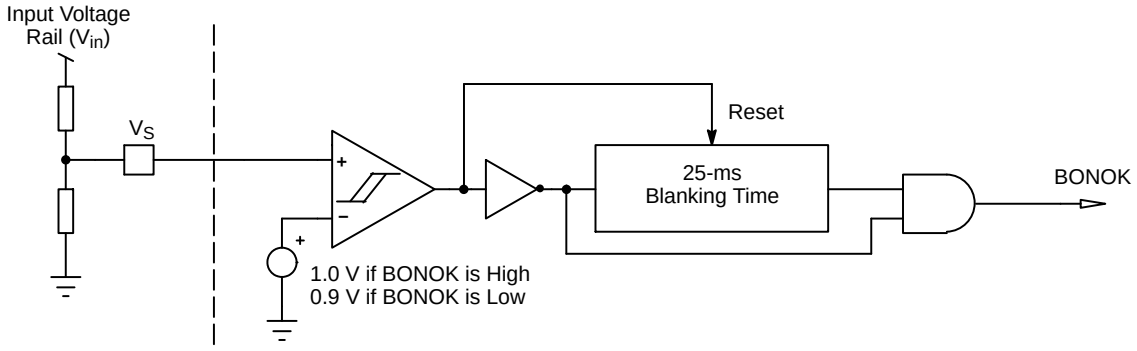


Figure 7. Brown-Out Protection Block

Input Voltage Sensing

A resistors divider (R_{S1} and R_{S2} of Figure 2 or Figure 6) provides pin 4 with the V_S signal. The scale-down factor is computed in accordance with the brown-out protection. If $(V_{in,rms})_{BOH}$ is the targeted minimum line rms voltage necessary for entering operation, R_{S1} and R_{S2} must comply with:

$$\frac{R_{S2}}{R_{S1} + R_{S2}} \cdot \sqrt{2}\left(V_{in,rms}\right)_{BOH} = V_{BO(on)} \qquad \text{(eq. 47)}$$

Where $V_{BO(on)}$ is the internal threshold (1 V typically) the V_S pin voltage must exceed to allow circuit operation.

In other words,

$$R_{S1} = R_{S2}\left(\frac{\sqrt{2}\left(V_{in,rms}\right)_{BOH}}{V_{BO(on)} - 1}\right) \qquad \text{(eq. 48)}$$

R_{S2} values ranging from 10 kΩ to 50 kΩ generally provide a good tradeoff between losses and noise immunity. In our application, we have selected 10 kΩ. Our system being supposed to enter operation when the line voltage exceeds 81 V rms:

$$R_{S1} = 10 \cdot 10^3 \cdot \left(\frac{\sqrt{2} \cdot 81}{1} - 1\right) \approx 1.1\ M\Omega \qquad \text{(eq. 49)}$$

It is generally recommended to place two (or more) resistors in series for sensing the high-voltage rail. In our case, we use 2 × 560-kΩ resistors for R_{S1}.

Line Range Detection

Similarly to the brown-out protection, the line range detection monitors the V_S peak voltage. As sketched by Figure 8, the NCL30288 detects:

- The low-line range if the V_S pin remains below the V_{LL} threshold (1.9 V typical) for more than the 25-ms blanking time.
- The high-line range as soon as the V_S pin voltage exceeds V_{HL} (2.0 V typical).

By the way, the line range detection thresholds are linked to the selected brown-out levels.

Let us assume that R_{S1} and R_{S2} of Figure 6 are selected for a brown-in level of 80 V rms (the circuit cannot start until the line voltage exceeds 80 V rms). In this case, (($V_{S,pk}$ = $V_{BO(on)} \cong 1$ V) @ 80 V rms) and the NCL30288 will detect:

- The high-line range when ($V_{S,pk} = V_{HL} \cong 2\ V_{BO(on)}$), that is, if $V_{in,rms}$ exceeds 160 V rms.
- The low-line range when ($V_{S,pk} < V_{LL} \cong 1.9\ V_{BO(on)}$), that is, if $V_{in,rms}$ goes below 152 V rms.

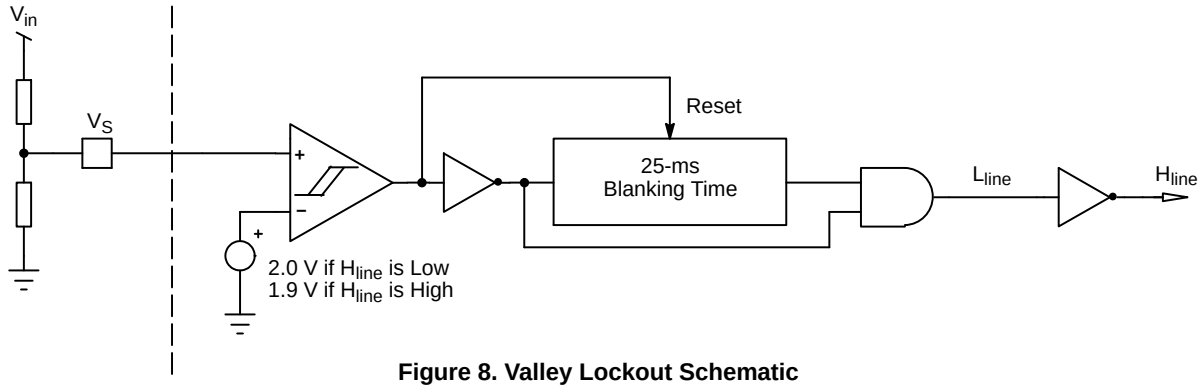
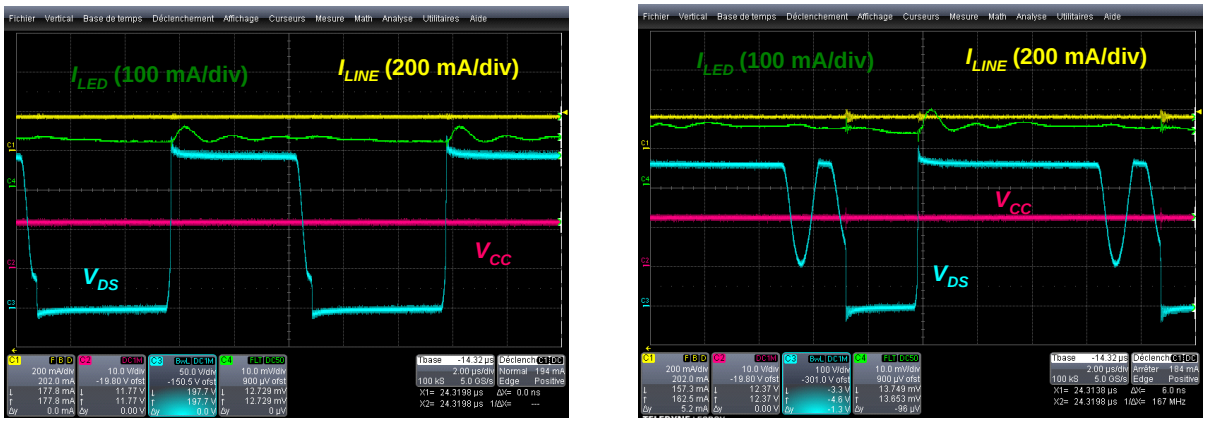


Figure 8. Valley Lockout Schematic

When the high-line range is detected, two changes in operation are performed:

- The NCL30288 transitions from quasi-resonant to valley-2 turn on operation (see Figure 9). In the low-line range, conduction losses are generally dominant. Adding a dead-time would further increase these losses. Hence, only a short dead-time is necessary to reach the MOSFET valley. In high-line conditions, switching losses generally are the most critical. It is thus efficient to skip one valley to lower the switching frequency. Hence, under normal operation, the NCL30288 optimizes the efficiency over the line range by turning on the MOSFET at the first valley in low-line conditions and at the second valley in the high-line case. This is illustrated by Figure 9 that sketches the MOSFET Drain-source voltage in both cases.



115 V rms 230 V rms

Figure 9. Quasi-resonant Mode in Low Line (Left), Turn On at Valley 2 when in High Line (Right)

- The gain of the averaging process is divided by two. This allows for an optimal resolution of the output current over the line range. Note that the change of gain causes a short discontinuity of operation at the very moment when the NCL30288 transitions from the low- to the high-line mode (typically when starting from a low-line mode condition, the line rms voltage exceeds 160 V rms) and at the very moment when the NCL30288 transitions from the high- to the low-line mode (typically when starting from a high-line mode condition, the line rms voltage goes below 152 V rms). This is because the provided output current differs from the target one until the COMP voltage has reached its new steady state value (see Figure 10). Note that it only occurs when the line magnitude is swept up or down out of the traditional mains range of interest.

Low-line Range is Detected High-line Range is Detected

Figure 10. Line Range Detection Events

Filtering the V_S Pin

An excessive high-frequency ripple on the V_S pin may alter the circuit operation. It is recommended to limit the high-frequency peak to peak ripple below 20% of the dc value.

Note however that too large a V_S capacitance should be avoided since:

- It would cause a phase shift which would degraded the power factor.
- In the case of an inductive, high-impedance EMI filter, this phase shift can increase the risk of EMI filter interactions.

Practically, only use a small capacitor to filter the switching ripple, hence creating a high-frequency pole. In our case, we implement C_3 = 470 pF (see Figure 18) leading to the following pole frequency:

$$\frac{1}{2\pi \left(R_5 + R_6\right) \parallel R_7 \cdot C_3} = \frac{1}{2\pi \left(560\ k + 560\ k\right) \parallel 10\ k \cdot 470\ p} \cong 34\ kHz \qquad \text{(eq. 50)}$$

If the EMI filter rings and more filtering is necessary, do not enlarge C_3 but rather add an R, C as shown in Figure 11. The role of this R, C is to offer more attenuation without increasing the phase shift at the EMI filter resonant frequency.

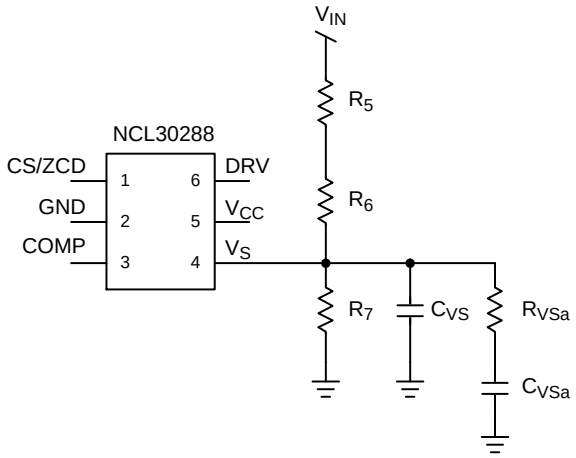


Figure 11. Filtering the V_S Pin

COMP Pin Capacitor

The COMP capacitance must be greater than 470 nF to ensure stability. Note that the 100- or 120-Hz ripple of the COMP pin is internally filtered out by a digital circuitry. Thus, it is not necessary to over dimension the COMP pin to optimize the power factor performance.

A 1-μF capacitor is generally a good choice.

Finally:

R_{S1}	R_{S2}	C_{COMP}	C_{VS}	R_{VSa}	C_{VSa}
1120 kΩ (two 560 kΩ placed in series)	10 kΩ	1 μF	470 pF	–	–

STEP 3: DRIVING THE CS/ZCD PIN

The CS/ZCD multi-functional pin is designed to monitor the primary peak current for protection and light control and the auxiliary winding voltage for zero current detection. In addition, the circuit compares the auxiliary winding voltage to an internal threshold (V_{OVP2} = 4.5 V typically) to detect a possible over-voltage condition (OVP2). Practically, if the CS/ZCD pin voltage exceeds V_{OVP2} (4.5 V typically) for more than 1 μs (after the ZCD blanking time), an OVP event is detected. If this happens for 4 consecutive switching cycles, an OVP fault is detected and the system enters auto-recovery mode. Finally, the NCL30288 CS/ZCD pin sources a current proportional to the V_S pin voltage for feedforward.

It is therefore important to properly dimension the external components driving the CS/ZCD pin which are shown by Figure 12.

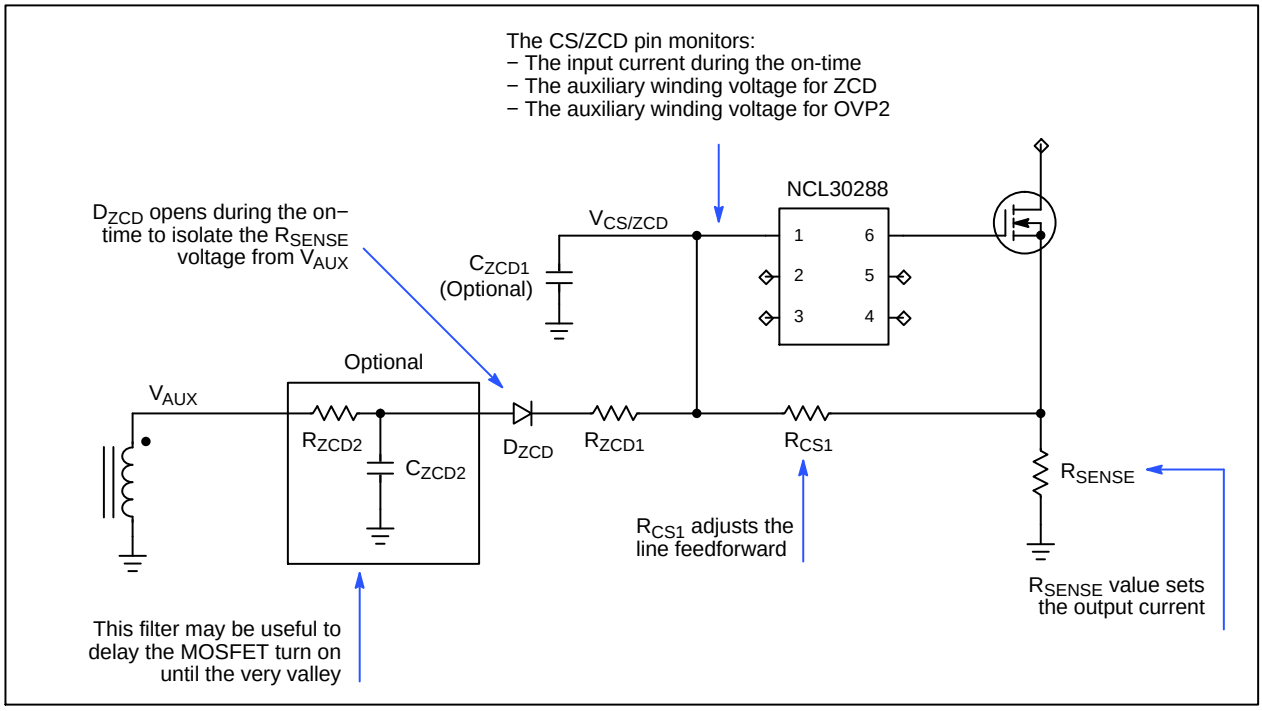


Figure 12. CS/ZCD Pin and Associated Functions

A typical waveform of the CS/ZCD pin voltage is shown in Figure 13.

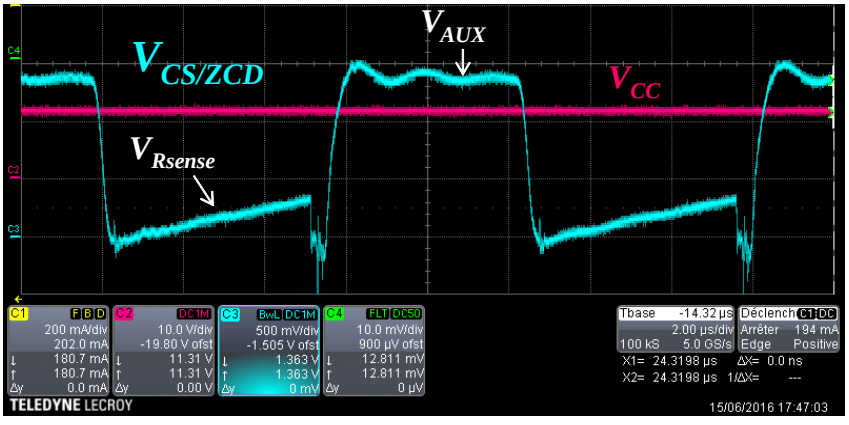


Figure 13. CS/ZCD Typical Waveform

Line Feedforward (LFF)

The NCL30288 computes the current setpoint ($V_{control}$) for power factor correction and proper regulation of the LED current. Now, the MOSFET cannot turn off at the very moment when the current-sense voltage exceeds $V_{control}$. There actually exists a propagation delay t_{prop} (Figure 14) for which the primary current keeps rising. As a result, the primary current does not exactly peak to the expected ($V_{control}$ / R_{sense}) value but to a higher level. The output current is hence also affected. Optimal regulation performance requires the peak current increase caused by t_{prop} to be compensated.

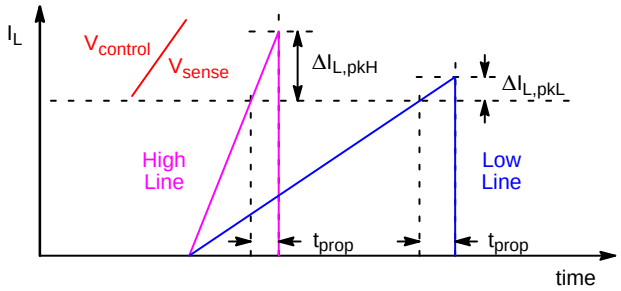


Figure 14. Propagation Delay Effect on Peak Current

The NCL30288 compensates for the propagation delay by sourcing a current proportional to the V_S pin voltage out of the CS pin during the on-time. Placing a resistor R_{CS1} between the CS pin and the sense resistor, the following offset is hence obtained:

$$V_{CS(offset)} = K_{LFF} \cdot v_s(t) \cdot R_{CS1} \qquad \text{(eq. 51)}$$

Where the V_S pin voltage $v_S(t)$ equates:

$$v_s(t) = \frac{R_{S2}}{R_{S1} + R_{S2}} \cdot v_{in}(t) \qquad \text{(eq. 52)}$$

Since the CS pin offset must compensate for

$$\left(R_{sense} \cdot \Delta I_{L,pk} = \frac{R_{sense} \cdot v_{in}(t) \cdot t_{prop}}{L_p} \right),$$

the offset resistor value can be computed as follows:

$$V_{CS(offset)} = \frac{R_{sense} \cdot v_{in}(t) \cdot t_{prop}}{L_p} \qquad \text{(eq. 53)}$$

Substitution of Equation 51 into Equation 53 leads to the following R_{LFF} expression:

$$R_{SC1} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \cdot \frac{t_{prop} R_{sense}}{L_P K_{LFF}} \qquad \text{(eq. 54)}$$

Where:

- K_{LFF} is the V_S pin voltage to CS pin current conversion ratio. Its typical value is 10.9 μS.
- R_{S1} and R_{S2} are the input voltage sensing resistors (see Figure 2).

Parameter t_{prop} consists of the controller internal delay (about 50 ns) and of the MOSFET turning off time. Thus, it varies with respect to the chosen MOSFET and the way it is driven (value of the gate resistors in particular). However, we can calculate R_{CS1}, using t_{prop} = 200 ns as a starting point and fine tune the LFF resistor value on the bench: R_{CS1} must be increased (more feedforward is needed) if the output current is a rising function of the line magnitude. Conversely, reduce R_{CS1} if the output current drops as the line voltage rises. R_{CS1} is optimal when the output current characteristic is nearly flat over the line voltage range.

Using Equation 54, we can obtain the following R_{LFF} starting value:

$$R_{SC1} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \cdot \frac{t_{prop} R_{sense}}{L_P K_{LFF}} = \left(1 + \frac{1120}{10}\right) \cdot \frac{200\,n \cdot 1}{1250\,\mu \cdot 11\,\mu} \cong 1.64\,k\Omega \qquad \text{(eq. 55)}$$

After lab verification, (R_{CS1} = 1.8 kΩ) was implemented.

Important Note: As indicated in the NCL30288 data sheet, R_{CS1} must be selected higher than 500 Ω. If not, the circuit may improperly detect that the CS pin is grounded.

Current Sense Resistor (R_{SENSE}) Selection

As explained in the data sheet, the output current is regulated to equal the following $I_{out,nom}$ nominal output current:

$$I_{out,nom} = \frac{V_{REF}}{2N_{PS} \cdot R_{SENSE}} \qquad \text{(eq. 56)}$$

Where:

- N_{PS} is the secondary to primary transformer turns ratio $N_{PS} = n_S / n_P$
- R_{SENSE} is the current sense resistor (see Figure 2)
- V_{REF} is the internal voltage reference (V_{REF} = 200 mV, typically).

In the case of a flyback converter, once the transformer is designed, N_{PS} is known and the only current sense resistor dictates the output current level. With non-isolated LED drivers, N_{PS} is 1.

Hence:

- Buck-boost LED driver:

$$R_{SENSE} = \frac{V_{REF}}{2 \cdot I_{out,nom}} \quad \text{(eq. 57)}$$

- Flyback LED driver:

$$R_{SENSE} = \frac{n_P}{n_S} \cdot \frac{V_{REF}}{2 \cdot I_{out,nom}} \quad \text{(eq. 58)}$$

The power dissipated by R_{sense} can be computed by the following equation:

- Buck-boost LED driver:

$$P_{R_{SENSE}} = \frac{4}{3} R_{SENSE} \left(\frac{P_{in,avg}}{V_{in,rms}}\right)^2 \left(1 + \frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot V_{out}}\right) \quad \text{(eq. 59)}$$

- Flyback LED driver:

$$P_{R_{SENSE}} = \frac{4}{3} R_{SENSE} \left(\frac{P_{in,avg}}{V_{in,rms}}\right)^2 \left[1 + \frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot \frac{n_P \cdot V_{out}}{n_S}}\right] \quad \text{(eq. 60)}$$

In our application:

- N_{PS} = 1 (buck-boost LED driver)
- $I_{out,nom}$ = 100 mA
- $(P_{in,avg})_{max}$ =20 W (assuming 90% efficiency)
- $(V_{in,rms})_{LL}$ = 90 V rms
- $V_{out,min}$ = 90 V dc

Hence:

$$R_{SENSE} = \frac{200 \cdot 10^{-3}}{2 \cdot 100 \cdot 10^{-3}} = 1\ \Omega \quad \text{(eq. 61)}$$

And:

$$P_{R_{SENSE}} = \frac{4}{3} \cdot 1 \cdot \left(\frac{20}{90}\right)^2 \left(1 + \frac{8\sqrt{2} \cdot 90}{3\pi \cdot 90}\right) \cong 150\ \text{mW} \quad \text{(eq. 62)}$$

Two 2 Ω resistors are placed in parallel.

Adjusting the OVP2 Protection

The NCL30288 features an over-voltage protection (OVP) which trips when V_{CC} exceeds the $V_{CC(OVP)}$ threshold (26.8 V typically). In addition to this non-programmable OVP, the OVP2 function provides an adjustable over-voltage protection by monitoring the auxiliary winding voltage (V_{AUX}) during the demagnetization phase. The OVP2 relies on the fact that the V_{AUX} voltage is substantially proportional to the output voltage during the demagnetization time:

$$V_{AUX} = \frac{n_{AUX}}{n_S} \cdot (V_{out} + V_f) \quad \text{(eq. 63)}$$

Where V_f is the output diode forward diode.

Hence, *during the demagnetization time*, the CS/ZCD pin voltage is:

$$V_{CS/ZCD} \cong \frac{R_{CS1}}{R_{CS1} + R_{ZCD1} + R_{ZCD2}} \cdot \left(\frac{n_{AUX}}{n_S}(V_{out} + V_f) - V_{D_{ZCD}}\right) \quad \text{(eq. 64)}$$

Where D_{ZCD}, R_{CS1}, R_{ZCD1} and R_{ZCD2} are the components shown in Figure 12 and V_{DZCD} is the forward diode of D_{ZCD}.

An internal flag is asserted when the CS/ZCD pin voltage exceeds V_{OVP2} (4.5 V typically) for about 1 μs, that is, when the output voltage exceeds the following OVP2 output level ($V_{OUT,OVP2}$):

$$V_{OUT,OVP2} = \left(\frac{n_S}{n_{AUX}}\left(\left(\frac{R_{CS1} + R_{ZCD1} + R_{ZCD2}}{R_{CS1}} \cdot V_{OVP2}\right) + V_{D_{ZCD}}\right)\right) - V_f \quad \text{(eq. 65)}$$

Hence, the sum (R_{ZCD1}+R_{ZCD2}) can be expressed as follows:

$$R_{ZCD1} + R_{ZCD2} = R_{CS1} \cdot \left(\left(\frac{n_{AUX}}{n_S} \cdot \frac{V_{OUT,OVP2} + V_f}{V_{OVP2}}\right) - \frac{V_{D_{ZCD}}}{V_{OVP2}} - 1\right) \quad \text{(eq. 66)}$$

If the flag is asserted for 4 consecutive switching cycles, an over-voltage fault is detected and like in the case of the other major fault situations (V_{CC} OVP, AUX or output short circuit protection and winding or output diode short circuit protection), the circuit enters the auto-recovery mode. Practically, the circuit grounds the COMP pin and stops generating DRV pulses for the auto-recovery 4-s delay. When this time has elapsed, the circuit recovers operation as soon as the V_{CC} voltage has exceeded the start-up threshold ($V_{CC(on)}$). The auto-recovery operation of Figure 15, was obtained by opening the LED driver. We can see that the LED driver stops operating until the 4-s timer has elapsed. At that moment, it resumes operation until a new OVP2 fault is detected. The LED driver recovers normal operation when the LED string is properly connected.

Figure 15. Auto-recovery Mode in Over-voltage Condition (Open LED String)

For instance, if we target 200 V as the output OVP2 level, Equation 66 leads to:

$$R_{ZCD1} + R_{ZCD2} = 1.8\,k \cdot \left(\left(\frac{1}{8} \cdot \frac{200 + 1}{4.5}\right) - \frac{1}{4.5} - 1\right) \quad \text{(eq. 67)}$$

$$= 7.9\,k\Omega$$

Note that when the drive turns low, the ZCD comparator is blanked at the off-time beginning for $t_{ZCD(blank1)}$, that is, 1.5 µs, typically[4]. In addition, OVP2 trips only if the CS/ZCD pin voltage exceeds the OVP2 threshold for more than 1 µs typically. Thus, the demagnetization phase must last for more than 2.5 µs typically (3.5 µs in worst case) to ensure OVP2 can properly trigger.

Diode D_{ZCD}

The diode D_{ZCD} which isolates the R_{SENSE} voltage from the auxiliary winding voltage during the on-time (see Figure 12) is a low current diode. It must be able to block the negative V_{AUX} voltage during the on-time

$$\left(-\frac{n_{AUX}}{n_P} \cdot v_{in}(t)\right)$$

Considering the worst case (highest line level), the diode reverse voltage must be higher than the following $V_{R,min}$ value:

$$V_{R,min} = \frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} \quad \text{(eq. 68)}$$

Where $(V_{in,rms})_{HL}$ is the highest line level rms voltage.

In our application, this leads to:

$$V_{R,min} = \frac{1}{8} \cdot \sqrt{2} \cdot 256 \cong 47\,V \quad \text{(eq. 69)}$$

However, the auxiliary winding voltage generally exhibits large negative spikes which must be taken into account. In general because of these spikes, it is recommended to at least double the Equation 69 value. In our application, a MMSD103 is selected. This is a 250-V, 200-mA, SOD−123 diode offering a safe margin.

Filtering the CS/ZCD Pin

The CS/ZCD pin is designed to monitor two different signals depending on the phase of the switching cycle:

- The R_{SENSE} voltage during the on-time
- The auxiliary winding voltage during the off-time

Adding a large capacitor on the pin would normally contribute in mixing the two signals by the inertia it brings. However, the NCL30288 allows for implementing capacitors (C_{CS} of Figure 12) up to 100 pF. This is because the circuit carefully manages the transitions on-time to off-time and on-time to on-time, in order to avoid any mix of these two sensed signals. In particular, it grounds the CS/ZCD pin at the beginning of each phase:

4. This ZCD blanking time is longer ($t_{ZCD(blank2)}$ = 3 µs typically) when the NCL30288 enters operation (cold startup, restart after a failure to startup at the first attempt or operation recovery after a fault) and keeps this value until the ZCD signal is enough to be detected by the ZCD comparator.

- *On-time to Off-time Transition:*
  When the drive turns low, the CS/ZCD pin is grounded for 325 ns (time T_1 of the parametric table). This cleans up the pin from any on-time residual voltage in particular if the CS/ZCD pin is filtered by a capacitor. In addition, the ZCD comparator is blanked at the off-time beginning for $t_{ZCD(blank1)}$, that is, 1.5 μs, typically[5].
- *Off-time to On-time Transition:*
  Similarly, the CS/ZCD is grounded for the 275-ns leading edge blanking time to in this case, avoid that a residual ZCD voltage alters the current sense block operation.

Now, a CS/ZCD pin filter (R_{CS1}, C_{CS}) increases the MOSFET turning-off delay, causing the output current rise (I_{out} higher than expected value). Thus, once R_{CS1} has been chosen, it is important to keep the value of C_{CS} as small as possible to have an optimal output current regulation. C_{CS} should be in the range of 10−100 pF.

If the CS/ZCD pin voltage needs to be delayed for valley detection, it is better to rely on the (R_{ZCD2}, C_{ZCD2}) network of Figure 12.

For in our application, the ZCD resistor is split in two resistors meeting Equation 67: R_{ZCD1} = 1.8 kΩ and R_{ZCD2} = 6.2 kΩ, so that adding C_{ZCD2} = 22 pF (see Figure 12), the delay necessary for valley detection is obtained.

5. This ZCD blanking time is longer ($t_{ZCD(blank2)}$ = 3 μs typically) when the NCL30288 enters operation (cold startup, restart after a failure to startup at the first attempt or operation recovery after a fault) and keeps this value until the ZCD signal is enough to be detected by the ZCD comparator.

Finally:

D_{ZCD}	R_{ZCD1}	R_{ZCD2}	C_{ZCD2}	R_{SENSE}	R_{CS1}	C_{CS}
MMSD103	1.8 kΩ	6.2 kΩ	22 pF	1 Ω (two 2-Ω resistors in parallel)	1.8 kΩ	–

STEP 4: AUXILIARY WINDING AND V_{CC} MANAGEMENT

The methodology detailed [2] can be re-used.

A simplified method is proposed here in which we arbitrary select 6.8 μF as the V_{CC} capacitance. This value proves to provide good V_{CC} cycle durations when associated with the recommended 1-μF COMP pin capacitor.

Selecting the V_{CC} Capacitor

As aforementioned, V_{VCC} = 6.8 μF is selected.

Startup Circuitry

When off (that is until V_{CC} has reached the 18-V start-up level), the NCL30288 consumes a very low current (13 μA typically, 30 μA maximum). Thus, high-impedance, low dissipation, resistors can be used to charge the V_{CC} capacitor at start-up.

Note however, that faults like a V_{CC} over-voltage condition lead the LED driver to stop switching and refrain from resuming operation until a 4-s delay is elapsed. A low duty ratio burst mode of operation is hence obtained as long as the fault is present. V_{CC} cycles up and down in such a case. For this time, the (off-mode) consumption is slightly higher (75 μA max.). It is hence recommended to have the startup current ($I_{startup}$ *of Figure 16) above 75 μA. If not,* V_{CC} *may collapse and the circuit reset before the 4-s delay has elapsed.*

As detailed in application note AND9131/D [3], the startup resistor $R_{startup}$ can either be connected to the bulk rail or to half-wave (Figure 16). Connecting the startup resistor to the half-wave reduces the power dissipated in the startup resistor.

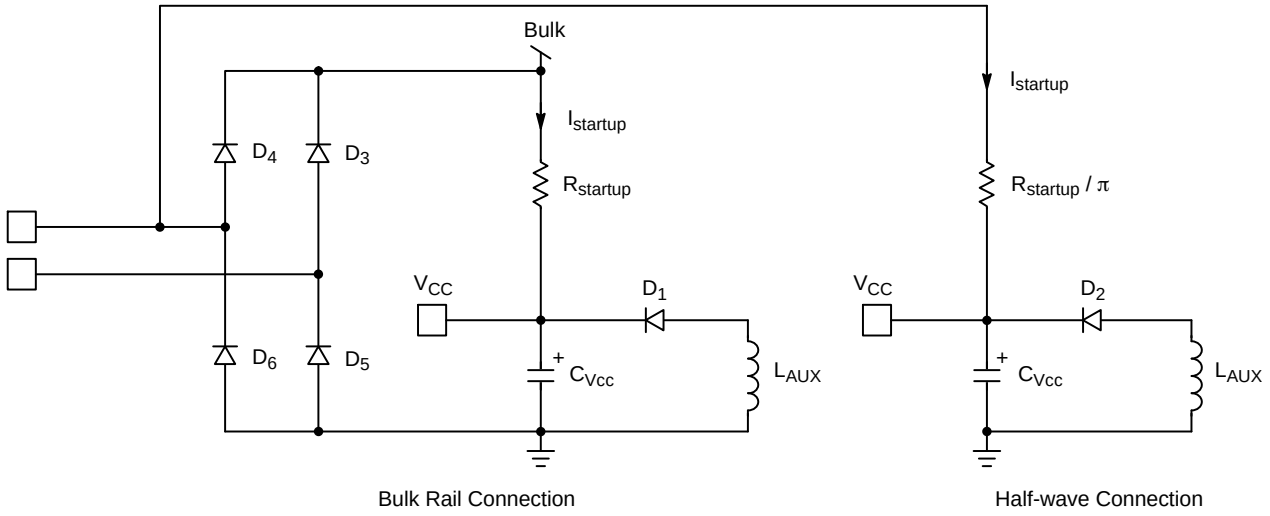


Figure 16. The Startup Resistor can be Connected to the Bulk Rail or to the Half-Wave

Computing the Startup Resistor

As a rule of thumb, the startup resistor is selected so that the V_{CC} capacitor charges up to the $V_{CC(on)}$ threshold (startup level, 18 V typically) within half the target startup time. It is assumed that the remaining half the target startup time will be necessary to have light starting from the moment when the LED driver enters operation.

Thus, the necessary startup current is:

$$I_{startup} = \frac{C_{VCC} \cdot V_{CC(on)}}{\frac{t_{startup}}{2}} = \frac{2 \cdot C_{VCC} \cdot V_{CC(on)}}{t_{startup}} \quad \text{(eq. 70)}$$

In our case, $t_{startup}$ = 500 ms, C_{VCC} = 6.8 μF and using the $V_{CC(on)}$ maximum limit (20 V), it comes:

$$I_{startup} = \frac{2 \cdot 6.8\,\mu \cdot 20}{500\,m} = 544\ \mu A \quad \text{(eq. 71)}$$

As discussed in the precedent paragraph, two types of connections can provide the startup current.

Bulk connection

For the start-up time, the bulk rail sees the line peak voltage (the input voltage becomes a rectified sinusoid when the LED driver starts to operate), the following formula gives the $R_{startup}$ value:

$$R_{startup} = \frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{I_{startup}} \quad \text{(eq. 72)}$$

Where:

- $I_{startup}$ is the desired startup current
- $(V_{in,rms})_{LL}$ is the lowest line rms voltage (90 V rms in our case)

The maximum power dissipated by the startup resistor connected to the bulk rail is:

$$P_{startup} = \frac{\left(\sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} - V_{CC}\right)^2}{R_{startup}} = \frac{2 \cdot \left(V_{in,rms}\right)_{HL}^2}{R_{startup}} \quad \text{(eq. 73)}$$

Where $(V_{in,rms})_{HL}$ is the highest line rms voltage.

Half-wave Connection

If the resistor is connected to the half-wave:

$$R_{startup1/2} = \frac{\frac{\sqrt{2}\cdot\left(V_{in,rms}\right)_{HL}}{\pi}}{I_{startup}} = \frac{R_{startup}}{\pi} \quad \text{(eq. 74)}$$

The maximum power dissipated by the startup resistor connected to the half-wave is thus:

$$P_{startup1/2} = \frac{\left(\frac{\sqrt{2}\cdot\left(V_{in,rms}\right)_{HL}}{\pi} - V_{cc}\right)^2}{R_{startup1/2}} \quad \text{(eq. 75)}$$

$$= \frac{2}{\pi^2}\cdot\frac{\left(V_{in,rms}\right)_{HL}^2}{\frac{R_{startup}}{\pi}} = \frac{2}{\pi}\cdot\frac{\left(V_{in,rms}\right)_{HL}^2}{R_{startup}}$$

In Our Application:

We selected the full-wave configuration. Since we have computed that the startup current had to be 544 μA or more, we can deduce:

$$R_{startup} \le \frac{\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}}{I_{startup}} = \frac{90\sqrt{2}}{544\ \mu} \cong 234\ k\Omega \quad \text{(eq. 76)}$$

A 224-kΩ startup resistor is selected by placing four 56-kΩ resistors in series.

The power dissipated for the startup resistor at maximum input voltage is:

$$P_{startup} = \frac{2\cdot 265^2}{224\ k} = 627\ mW \quad \text{(eq. 77)}$$

Clamping V_{CC}

When short startup times are specified, the startup current can be large at the highest line levels. For instance, in our example, it can reach 1.7 mA at very high line. It can thus happen that in fault conditions where the NCL30288 consumes less than 1.55 mA (see I_{CC1} parameter of the data sheet), the startup resistors provide more current than absorbed by the circuit. As a result, the V_{CC} voltage rises leading the circuit to be latched off by the $V_{CC(OVP)}$ protection or even worse, to be damaged because of an excessive V_{CC} voltage. That is why it is recommended to clamp V_{CC} using a resistor in series with a Zener diode (R_{15} and ZD_1 of Figure 18). *Implementing a simple Zener diode (without a series resistor) is NOT a recommended option* since it would firmly clamp both the V_{CC} and auxiliary voltages. This would alter the LED driver operation and disable both the OVP2 and $V_{CC(OVP)}$ protections. As a result, the LED driver would not be protected if the LED string happens to open.

Select a Zener diode which reverse Zener voltage is just above the NCL30288 $V_{CC(on)}$ maximum value (20 V). In our application, we choose a 22-V Zener diode. The series resistance should be in the range of few kΩ to limit the current drawn by the Zener diode at the highest V_{CC} levels. It must however be low enough to be able to absorb the startup current excess without triggering the $V_{CC(OVP)}$ protection. Since the circuit consumes at least 1.15 mA in fault mode (I_{CC1} minimum value – see data sheet) and the minimum threshold of the $V_{CC(OVP)}$ protection is 25.5 V, it comes:

$$R_Z \le \frac{\left(V_{CC(OVP)}\right)_{min} - V_Z}{\left(I_{start}\right)_{max} - \left(I_{CC1}\right)_{min}} = \frac{25.5 - 22}{1.7\ m - 1.15\ m} \cong 6.4\ k\Omega \quad \text{(eq. 78)}$$

Where R_Z is the resistor in series with the Zener diode.

We select a 2.2-kΩ resistor.

Another option could have consisted of inhibiting the startup current at high V_{CC} levels. See Figure 17b. A high-voltage transistor is inserted between the startup resistors and the V_{CC} pin. It is turned off when V_{CC} exceeds the ($V_Z - V_f - V_{be}$) where V_{be} is the bipolar transistor base-emitter voltage, V_f is the forward voltage of the diode placed in series with the transistor emitter and V_Z is the Zener voltage of the Zener diode which drives the transistor base. This second option is more expensive (a high-voltage transistor is required) but can save the startup dissipation if the circuit operates at a V_{CC} level high enough to disable the transistor.

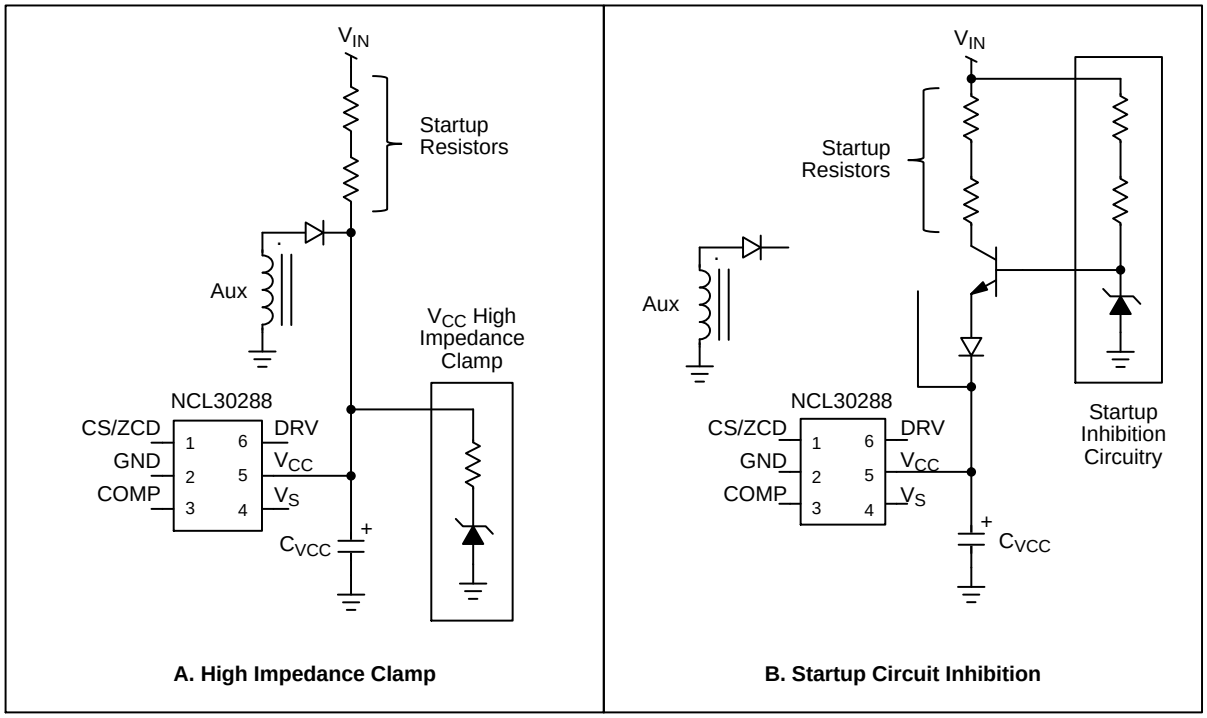


Figure 17. Preventing Excessive V_{CC} Levels

V_{CC} Refueling Diode (D_{AUX})

In nominal operation, the auxiliary winding provides the V_{CC} voltage as shown by Figure 2. The auxiliary winding number of turns (n_{AUX}) is computed in the inductor/transformer section of the "Step 1" paragraph. Note that during the on-time, diode D_{AUX} of Figure 2 rectifies the auxiliary voltage to provide V_{CC}. Hence, neglecting the turn on spike, D_{AUX} must be able to sustain:

$$V_{D_{AUX}} = V_{CC} + \left(\frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}\right) \quad \text{(eq. 79)}$$

The V_{CC} highest value is the maximum voltage the $V_{CC(OVP)}$ threshold can take (28.5 V). Therefore:

$$V_{D_{AUX}} = \left(V_{CC(OVP)}\right)_{max} + \left(\frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}\right) \quad \text{(eq. 80)}$$

In our case:

$$V_{D_{AUX}} = \left(V_{CC(OVP)}\right)_{max} + \left(\frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}\right) \cong 28.5 + \left(\frac{1}{8} \cdot \sqrt{2} \cdot 265\right) \cong 75\ V \quad \text{(eq. 81)}$$

Due to the turn on spike, some significant headroom is necessary. Selecting a diode exhibiting at least twice the computed V_{RRM} value seems a good practice.

A MMSD103, 250-V, 200-mA, SOD−123 diode is implemented in our application.

Finally:

C_{VCC}	$R_{startup}$	$R_{startup1/2}$	D_{AUX}	R_Z	ZD_1
6.8 µF/35 V	four 56-kΩ, 1/4 W resistors in series	N/A	MMSD103	2.2 kΩ	22 V

CONCLUSIONS

This paper summarizes the key steps when dimensioning a LED driver controlled by the NCL30288. The proposed approach being systematic, it can be easily applied to another application. In addition, an Excel Spreadsheet is available that further eases your design by automatically computing the main components of your application according to the described method [5].

The process has been illustrated by the example of an 18-W, wide-mains application. Evaluation board NCL30288LED1GEVB demonstrates such a high PF buck-boost LED driver in a typical T8 outline. [4] details the specification, theory of operation, testing and construction of this demonstration board. Implementation details (BOM, GERBER files, …) can be found on our web site [6].

More details on the circuit operation can be found in its data sheet [1].

DETAILED SCHEMATIC

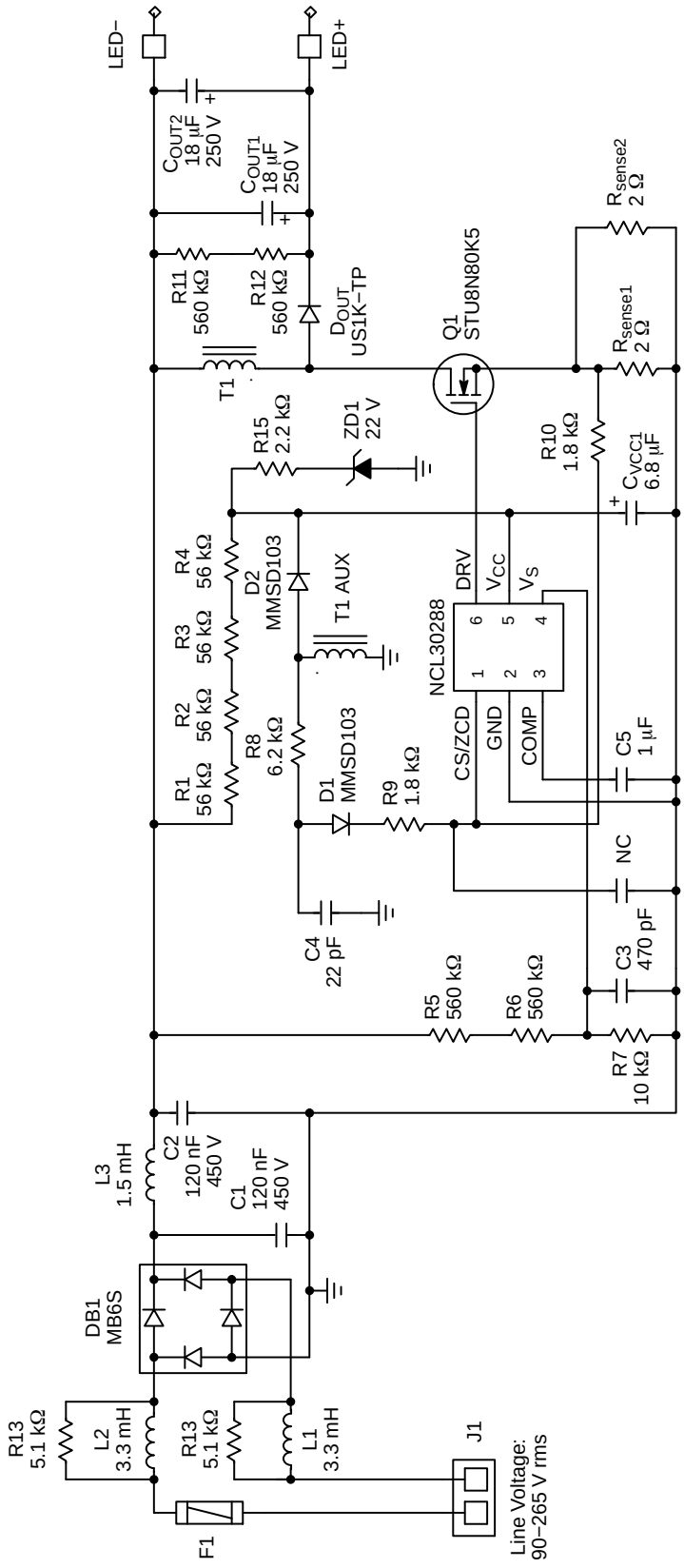


Figure 18. Detailed Application Schematic of the 18-W, Universal Mains LED Driver

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[3] Stéphanie CANNENTERRE, Application note AND9131/D, “Designing a LED Driver with the NCL30080/81/82/83”, http://www.onsemi.com/pub_link/Collateral/AND9131−D.PDF

[4] Jim YOUNG, “NCL30288LED1GEVB 18 W High Power Factor LED Driver − Evaluation Board User Manual”, http://www.onsemi.com/PowerSolutions/supportDoc.do?type=boards&rpn=NCL30288

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[6] NCL30288LED1GEVB Evaluation Board Documents, http://www.onsemi.com/PowerSolutions/supportDoc.do?type=boards&rpn=NCL30288

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