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Designing a NCL30185-Controlled LED Driver

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APPLICATION NOTE

Description

This paper proposes the key steps to rapidly design a NCL30185-driven flyback converter to power an LED string. The process is illustrated by a practical 10-W, universal mains application:

- Maximum Output Power: 10 W
- Input Voltage Range: 90 to 265 V rms
- Output Voltage Range: 12 to 20 V dc
- Output Current: 500 mA
- 3-Step Dimming: 70%/25%/5%

Introduction

The NCL30185 is a driver for power-factor corrected flyback, non-isolated buck-boost and SEPIC converters. An internal proprietary circuitry controls the input current in such a way that a power factor as high as 0.99 and an output current deviation below ±2% are typically obtained without the need for a secondary-side feedback. The current-mode, quasi-resonant architecture optimizes the efficiency by turning on the MOSFET when the drain-source voltage is minimal (valley). At high line, the circuit delays the MOSFET turn on until the second valley is detected to reduce the switching losses (see Figure 1). The 3-step dimming function decreases the output current from 100% to 70%, 70% to 25%, 25% to 5% or increases it back from 5% to 100% whenever a short brown-out event is detected. The step-dimming function is reset (maximum current is provided) if the brown-out event lasts for more than 3 s typically. Valley lockout and frequency fold-back capabilities maintain high-efficiency performance in dimmed conditions.

Pin−to−pin compatible to the NCL30085, the NCL30185 provides the same benefits with in addition, an increased resolution of the digital current−control algorithm for a 75% reduction in the LED current quantization ripple.

In addition, the circuit contains a suite of powerful protections to ensure a robust LED driver design without the need for extra components or overdesign. Among them, one can list:

- *Over Temperature Thermal Fold-back:* connecting a NTC to the SD pin allows for gradual reduction of the LED current down to 50% of its nominal value when the temperature is excessive. If the current reduction does not prevent the temperature from reaching a second level, the controller stops operating (SD pin OTP).
- *Over Voltage Protection:* A Zener diode can further be used on the SD pin to provide an adjustable OVP protection (SD pin OVP).
- *Cycle-by-Cycle Peak Current Limit:* when the current sense voltage exceeds the internal threshold (V_{ILIM}), the MOSFET immediately turns off (cycle-by-cycle current limitation).
- *Winding and Output Diode Short-Circuit Protection (WODSCP):* an additional comparator stops the controller if the CS pin voltage exceeds (150% · V_{ILIM}) for 4 consecutive cycles. This feature can protect the converter if a winding or the output diode is shorted or simply if the transformer saturates.
- *Output Short-Circuit Protection:* If the ZCD pin voltage remains low for a 90-ms time interval, the controller stops pulsating until 4 seconds have elapsed.
- *Open LED Protection:* if the V_{CC} pin voltage exceeds the OVP threshold, the controller shuts down and waits 4 seconds before restarting switching operation.
- *Floating/Short Pin Detection:* the circuit can detect most of these situations which helps pass safety tests. Note that the NCL30185 incorporates the same protection features as the NCL30085 for which [2] reports the behavior under safety tests in the application discussed in this document.

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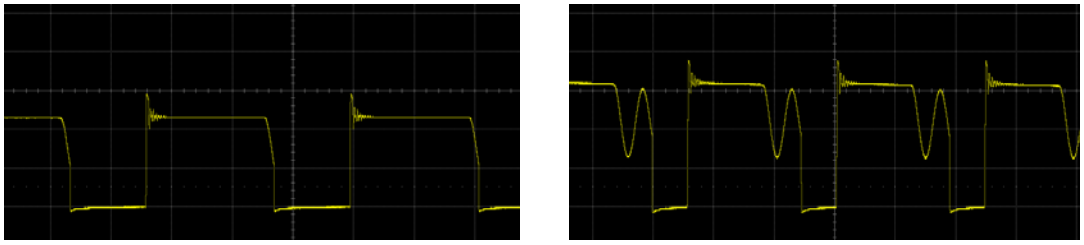


Figure 1. Quasi-Resonant Mode in Low Line (Left), Turn On at Valley 2 when in High Line (Right)

PRELIMINARY REMARKS

Two NCL30185 Versions

There exist two NCL30185 versions. As summarized by Table 1, they differ in their respective protection mode. When the Winding and Output Diode Short Circuit Protection (WOD_SCP) or the Output and Auxiliary Winding Short Circuit Protection (AUX_SCP) triggers, the A version latches-off while the NCL30185B enters the auto-recovery mode. Similarly, the SD over-temperature and over-voltage protections (SD pin OTP and SD pin OVP) are latching-off in the NCL30185A and auto-recovery in the NCL30185B.

Table 1. PROTECTION MODES

	AUX_SCP	WOD_SCP	SD Pin OTP	SD Pin OVP
NCL30185A	Latching Off	Latching Off	Latching Off	Latching Off
NCL30185B	Auto-Recovery	Auto-Recovery	Auto-Recovery	Auto-Recovery

In the case of a latching-off fault, the circuit stops pulsing until the LED driver is unplugged and V_{CC} drops below $V_{CC(reset)}$ (5 V typically). At that moment, the fault is cleared and the circuit can resume operation. In the auto-recovery case, the circuit cannot generate DRV pulses for the auto-recovery 4-s delay. The circuit recovers operation when this time has elapsed.

Duty-Ratio Limitation

The NCL30185A/B duty-ratio is internally limited to 50% at the top of the lowest line sinusoid. Output current regulation will then be optimal as long as the lowest line peak voltage is higher than the inductor demagnetization voltage, i.e.,:

- If $\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} \geq V_{out} + V_f\right)$ with non-isolated converters,
- If $\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} \geq \frac{n_p}{n_s}\left(V_{out} + V_f\right)\right)$ in flyback applications,

where $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (85 or 90 V rms in general) and (V_f) is the output diode forward voltage.

Table 2. NCL30185 CONDITIONS OF USING

	Output Voltage Range for Non-Isolated Converters (Note 1)	**Output Voltage Range for Flyback Converters** (Note 1)
NCL30188A (Note 2)	$V_{out} + V_f \leq \sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$	$V_{out} + V_f \leq \frac{n_s}{n_p}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$
NCL30188BA	$V_{out} + V_f \leq \sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$	$V_{out} + V_f \leq \frac{n_s}{n_p}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$

1. $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (e.g., 85 V rms), (V_f), the output diode forward voltage.
2. Please contact local sales representative for availability.

As an example, let's assume that we must design a 90 to 265 V rms, non-isolated buck-boost converter. For optimal control accuracy, the LED driver output voltage should not exceed:

$$V_{out,max} = \sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} - V_f \cong \cong \sqrt{2}\cdot 90 - 1 \cong 126\ V \quad \text{(eq. 1)}$$

If the duty-ratio limitation is exceeded by your application, the LED current will be below its nominal value at the lowest line voltage but will meet the target when the input voltage level is sufficient. By the way, a symptom of the duty-ratio limitation effect can be observed as shown by Figure 2 where the input current is clamped by the over-current protection during normal load conditions.

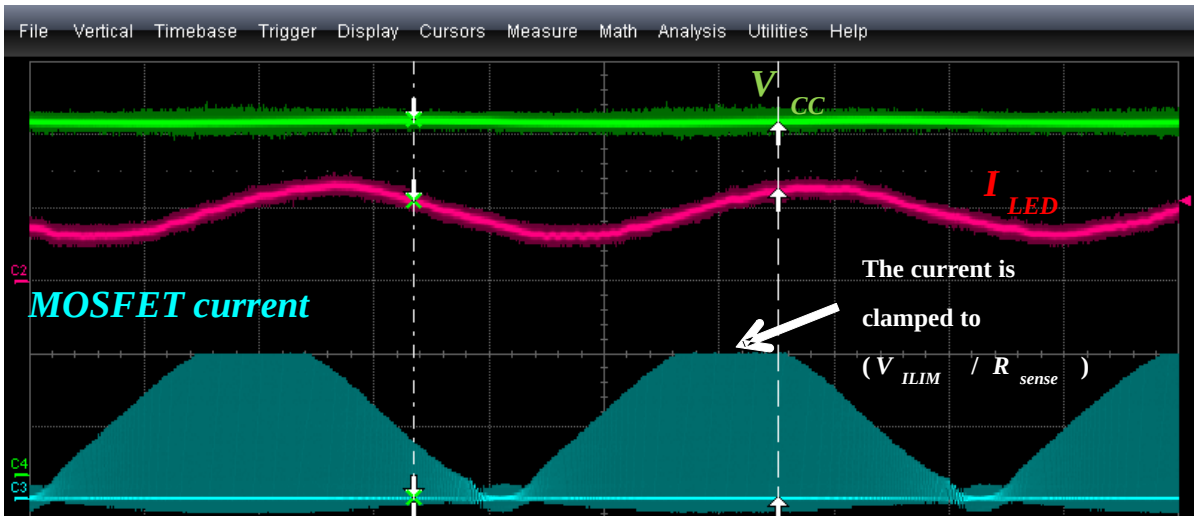


Figure 2. Current Over-Current Limitation
(V_{ILIM} is Over-Current Threshold, R_{SENSE} the Current Sense Resistor)

Our application of interest is a flyback converter. Note that in this case, turns ratio provides some flexibility which can help meet the condition of using.

LED DRIVER DIMENSIONING

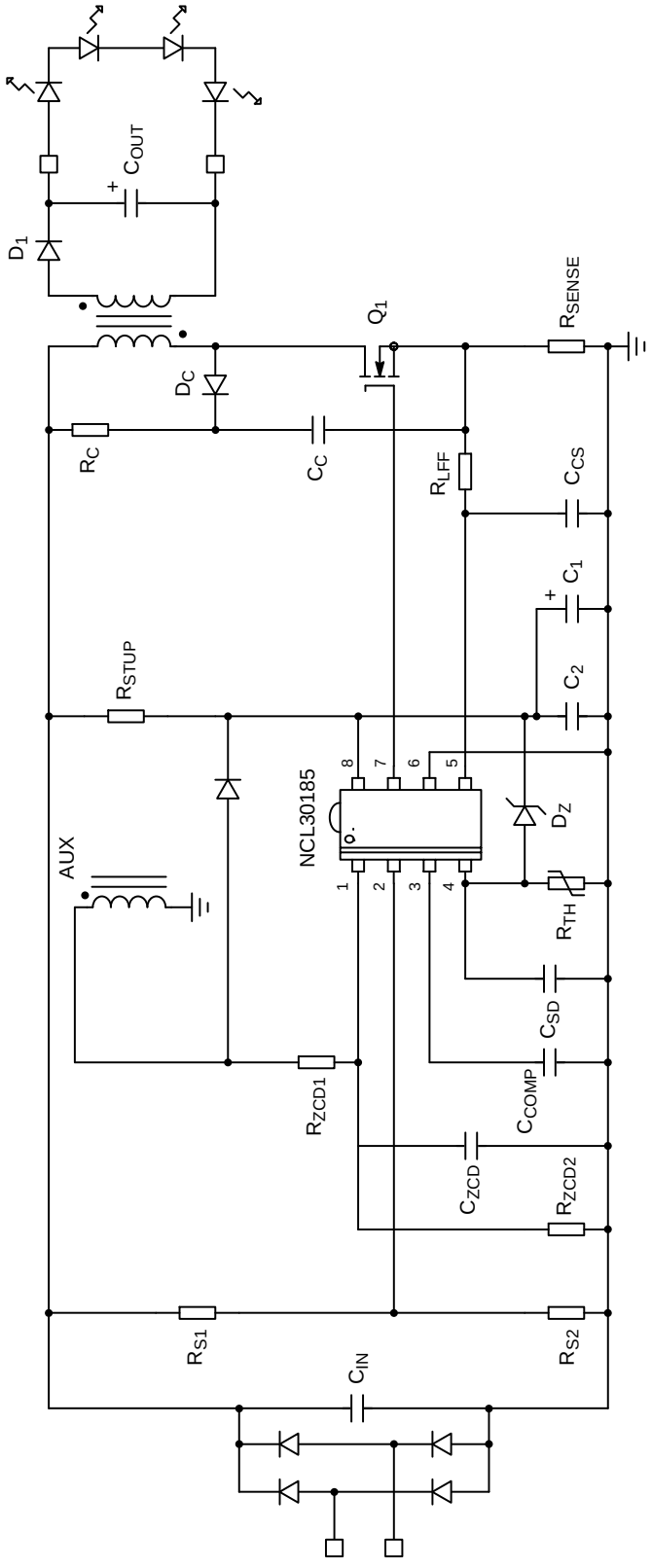


Figure 3. Basic Schematic

LED DRIVER DESIGN STEPS

AND9451 [1] details the design procedure of a LED driver controlled by the NCL30188. The same process is valid for the NCL30185 apart from a few specificities.

This application note will not re-discuss the AND9451 procedure but only provide below summary of the key design steps. NCL30185 specificities will be covered in the next chapter.

Note that if provided equations must help provide a good starting point, bench validation remains necessary!

SUMMARY OF KEY DESIGN STEPS

Table 3. DESIGN STEPS TABLE

Step	Components	Formula	Comments
Step 1: Power Components Selection	Transformer: Auxiliary Winding Number of Turns	$n_{AUX} \le n_s \cdot \frac{\left(V_{CC(OVP)}\right)_{min} + V_f}{V_{out(OVP)} + V_f}$	If a Zener diode is connected between the V_{CC} rail and the SD pin protection for OVP protection, $V_{CC(OVP)}$ is to be replaced by the (V_Z + 2.5). $V_{out(OVP)}$ is the output voltage when the V_{CC} or SD pin OVP trips ($V_{out(OVP)}$ can be viewed as the possible maximum value of the output voltage)
	MOSFET Turn Off Overshoot	$V_{Q-ov} = k_c \cdot \frac{n_p}{n_s} \cdot \left(V_{out} + V_f\right)$	The MOSFET turn-off overshoot due to the leakage inductor reset is expressed as a function of the reflected voltage (see Figure 4)
	MOSFET Turn Off Overshoot Coefficient	$0.5 \le k_c \le 1.0$	A low k_c reduces the MOSFET voltage stress but requires more losses to be dissipated in the clamping network. As a rule of thumb, take k_c between 0.5 and 1.0.
	Transformer: secondary winding number of turns	$\frac{n_p}{n_s} < \frac{\alpha V_{DSS} - \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}}{(1 + k_c) \cdot \left(V_{out(OVP)} + V_f\right)}$	V_{DSS} is the MOSFET breakdown voltage, α designates the derating factor (85% typically)
	Transformer: primary inductance	$L_p \ge \frac{\left(V_{in,rms}\right)^2}{2 f_{sw,T} P_{in,avg}} \cdot \left(\frac{\frac{n_p}{n_s}\left(V_{out} + V_f\right)}{\beta V_{in,pk} + \frac{n_p}{n_s}\left(V_{out} + V_f\right)} \right)^2$	If the primary inductor is selected equal to the proposed expression, the switching frequency will be below $f_{sw,T}$ when the line instantaneous voltage is between ($\beta \cdot V_{in,pk}$) and $V_{in,pk}$ where ($\beta \le 1$). For instance, one can force the full-load frequency range at the 115-V rms nominal voltage to be around 65 kHz for instance, by practically opting for (β = 50%) and ($f_{sw,T}$ = 65 kHz)
	Clamping Network Resistor Value	$R_c \le \frac{2 \cdot k_c}{N_{PS}} \cdot \left(V_{out(OVP)} + V_f\right) \cdot \frac{\frac{1+k_c}{N_{PS}} \cdot \left(V_{out(OVP)} + V_f\right) + \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}}{L_{leak} \cdot \left(\frac{V_{ILIM}}{R_{sense}}\right)^2 \cdot f_{SW,HL}}$	V_{ILIM} is the NCL30185 internal threshold for over-current limitation (1 V typically). $(V_{in,rms})_{HL}$ and $f_{sw,HL}$ are the rms input voltage and the switching frequency at the line highest level.
	Clamping Network Resistor Losses	$P_{R_c} \le \frac{\left(\frac{n_p}{n_s} \cdot (1 + k_c) \cdot \left(V_{out(OVP)} + V_f\right)\right)^2}{R_C}$	$V_{out(OVP)}$ is the output voltage when the V_{CC} or SD pin OVP trips ($V_{out(OVP)}$ can be viewed as the possible maximum value of the output voltage)

Table 3. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
	Clamping Network Capacitor	$C_C \cong \frac{1\ ms}{R_C}$	
	Maximum Primary Inductor Peak Current	$\left(I_{L,pk}\right)_{max} = 2\sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \left(1 + \frac{n_s \cdot \sqrt{2}\left(V_{in,rms}\right)_{LL}}{n_p \cdot \left(V_{out} + V_f\right)}\right)$	
	Maximum Primary Inductor rms Current	$\left(I_{L,rms}\right)_{max} = \frac{2 \cdot \left(P_{in,avg}\right)_{max}}{\sqrt{3} \cdot \left(V_{in,rms}\right)_{LL}} \cdot \cdot \sqrt{1 + \frac{16 \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{3\pi \cdot \frac{V_{out}+V_f}{N_{PS}}} + \frac{6\pi \cdot \left(V_{in,rms}\right)_{LL}^2}{4 \cdot \left(\frac{V_{out}+V_f}{N_{PS}}\right)^2}}$	N_{PS} is the turns ratio $N_{PS} = n_s / n_p$
	MOSFET rms Current	$\left(I_{Q,rms}\right)_{max} = \frac{2}{\sqrt{3}} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \sqrt{1 + \frac{8\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{3\pi \cdot \frac{V_{out}+V_f}{N_{PS}}}}$	
	Maximum MOSFET Drain-Source Voltage	$V_{ds,max} = \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} + \frac{(1 + k_c) \cdot \left(V_{out(OVP)} + V_f\right)}{\frac{n_s}{n_p}}$	
	Maximum Output Diode Voltage	$V_{diode,max} = \left(\frac{n_s}{n_p} \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{max}\right) + V_{out} + V_f + V_{D-ov}$	V_{D-ov} is the output diode overshoot that occurs when the MOSFET turns on.
	Output Diode Average Current	$I_{diode,avg} = I_{out}$	
	Output Diode Rms Current	$\left(I_{D,rms}\right)_{max} = = \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{n_p}{n_s}\right)^2 \cdot \frac{\left(P_{in,avg}\right)_{max}^2}{V_{in,rms} \cdot \frac{V_{out}+V_f}{N_{PS}}} \cdot \left[1 + \frac{9\pi^2}{12\sqrt{2}} \cdot \frac{V_{in,rms}}{\frac{V_{out}+V_f}{N_{PS}}}\right]}$	
	Minimum Output Capacitor Value	$C_{out,min} = \frac{\sqrt{\left[\frac{2}{\frac{\left(\Delta I_{out}\right)_{pk-pk}}{I_{out,nom}}}\right]^2 - 1}}{4\pi \cdot f_{line,min} \cdot R_{LED,min}}$	$I_{out,nom}$ is the nominal output current, $R_{LED,min}$, the minimum LED series resistor, and $(\Delta I_{out})_{pk-pk}$, the output current targeted peak-to-peak ripple.
	Output Capacitor Rms Current	$\left(I_{D,rms}\right)_{max} = = \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{n_p}{n_s}\right)^2 \cdot \frac{\left(P_{in,avg}\right)_{max}^2}{V_{in,rms} \cdot \frac{V_{out}+V_f}{N_{PS}}} \cdot \left[1 + \frac{9\pi^2}{12\sqrt{2}} \cdot \frac{V_{in,rms}}{\frac{V_{out}+V_f}{N_{PS}}}\right] - I_{out,nom}^2}$	

Table 3. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
Step 2: Output Current Setting	Current Sense Resistor	$R_{sense} = \frac{n_p}{n_s} \cdot \frac{V_{REF}}{2 \cdot I_{out,nom}}$	V_{REF} is the 250-mV internal reference
	COMP Capacitor	1 μF or More	
	V_{SENSE} Resistors	$R_{S1} = R_{S2} \cdot \left(\frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{BOH}}{V_{BO(on)}} - 1 \right)$	$(V_{in,rms})_{BOH}$ is the minimum line rms voltage for entering operation. $V_{BO(on)}$ is the Brown-Out protection internal threshold (1 V typically).
	Feedforward Resistor	$R_{LFF} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \cdot \frac{t_{prop} \cdot R_{sense}}{L_p \cdot K_{LFF}}$	T_{prop} is the total propagation delay between the instant when the MOSFET current reaches the setpoint and the effective MOSFET turn off. You can take 250 ns or 300 ns as a starting value. K_{FLL} is an internal ratio (20 μS typically)
	Current Sense Capacitor	Few pF	No capacitor is normally necessary. 10 to 22 pF can be placed in case of noisy signals.
Step 3: SD Pin Management	SD Pin OVP Threshold	$\left(V_{CC}\right)_{SD,OVP} = V_Z + V_{OVP}$	V_{OVP} is the SD pin OVP internal threshold (2.5 V typically)
	SD Pin Capacitor	< 4.7 nF	A filtering capacitor can be placed across the pin and ground. This capacitor must be less than 4.7 nF. If not, a false OTP detection may occur (see data sheet).
	SD Pin NTC		See Figure 5
Step 4: Auxiliary Winding and V_{CC}	V_{CC} Capacitor Minimum Value	$\left(C_{Vcc}\right)_{min} \cong \frac{n_s \cdot C_{out}}{n_{aux}} \cdot \frac{\left(I_{CC2} + Q_g \cdot f_{sw}\right)}{I_{out}} \cdot \frac{\left(V_{CC(off)}\right)_{max}}{\left(V_{CC(HYS)}\right)_{min}}$ or $\left(C_{Vcc}\right)_{min} \cong 1.175 \cdot \frac{n_s \cdot C_{out}}{n_{aux}} \cdot \frac{\left(I_{CC2} + Q_g \cdot f_{sw}\right)}{I_{out}}$	$(I_{CC2} + Q_g \cdot f_{sw})$ is an estimation of the circuit consumption (I_{CC2} is 4 mA max, Q_g is the MOSFET gate charge and f_{sw} is the switching frequency). $(((V_{CC(off)})_{max} / (V_{CC(HYS)})_{min}) = 1.175)$ is the ratio of the maximum value of the V_{CC} voltage necessary to maintain operation (9.4 V) over the minimum UVLO hysteresis (8 V).
	Required Start-up Current	$I_{startup} = \frac{\left(V_{CC(on)}\right)_{max} \cdot C_{Vcc}}{t_{startup}} + \left(I_{CC(start)}\right)_{max}$ $I_{startup} = \frac{20 \cdot C_{Vcc}}{t_{startup}} + 30\ \mu A$	$(V_{CC(off)})_{max}$ is the maximum value of the VCC voltage necessary to enter operation (20 V), $(I_{CC(start)})_{max}$ is the maximum circuit consumption before entering operation (30 μA), $t_{startup}$ is the targeted start-up time.
	Start-up Resistor Value	Half-Wave Connection: $R_{startup1/2} = \frac{\left(V_{in,rms}\right)_{LL} \cdot \sqrt{2}}{\frac{\pi}{I_{startup}}}$ Bulk Connection: $R_{startup} = \frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{I_{startup}}$	See Figure 6

Table 3. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
	Start-up Resistor Losses	Half-Wave Connection: $P_{startup1/2} = \frac{\left(\frac{\sqrt{2}\cdot\left(V_{in,rms}\right)_{HL}}{\pi} - V_{CC}\right)^2}{R_{startup1/2}} \le \frac{2}{\pi^2}\cdot\frac{\left(V_{in,rms}\right)^2_{HL}}{R_{startup1/2}}$ Bulk Connection: $P_{startup1/2} = \frac{\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{HL} - V_{CC}\right)^2}{R_{startup}} \le \frac{2\cdot\left(V_{in,rms}\right)^2_{HL}}{R_{startup}}$	
	Upper ZCD Resistor	$R_{ZCD1} \ge \frac{V_{CC(OVP)max} + V_f}{I_{ZCD,dmg}}$ And: $R_{ZCD1} \ge \frac{n_{aux}}{n_p}\cdot\frac{\sqrt{2}\cdot\left(V_{in,rms}\right)_{HL}}{I_{ZCD,on}}$	$I_{ZCD,dmg}$ is the maximum current that can be injected in the ZCD pin (5 mA), $I_{ZCD,on}$ is the maximum current which can be extracted from the ZCD pin (2 mA).
	Bottom ZCD Resistor	$R_{ZCD2} \le \frac{5\ V}{V_{CC(OVP)} + V_f - 5\ V}\cdot R_{ZCD1}$	R_{ZCD2} serves to maintain the ZCD pin voltage below 5 V for optimal operation.
	ZCD Pin Capacitor	10 or 22 pF	

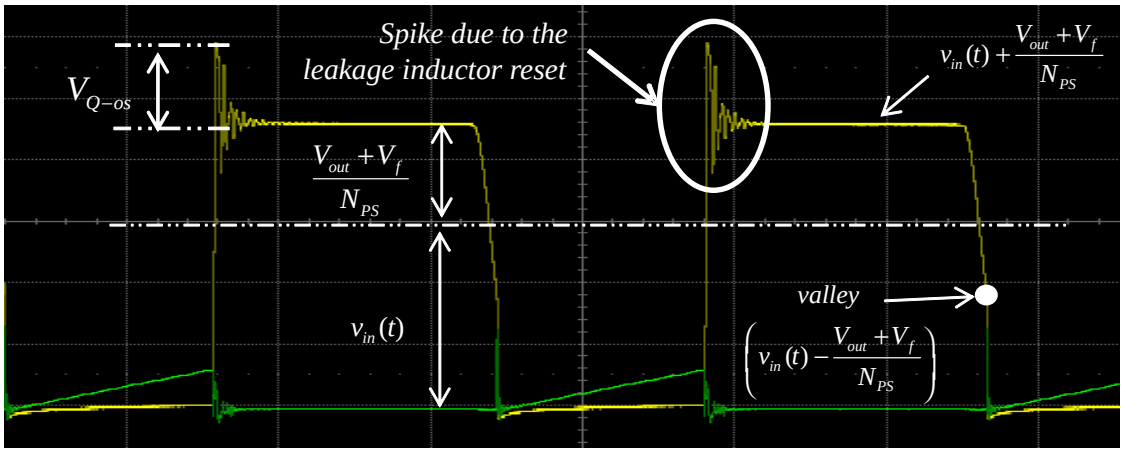


Figure 4. MOSFET Drain-Source Voltage (Yellow Trace) and Current (Green)

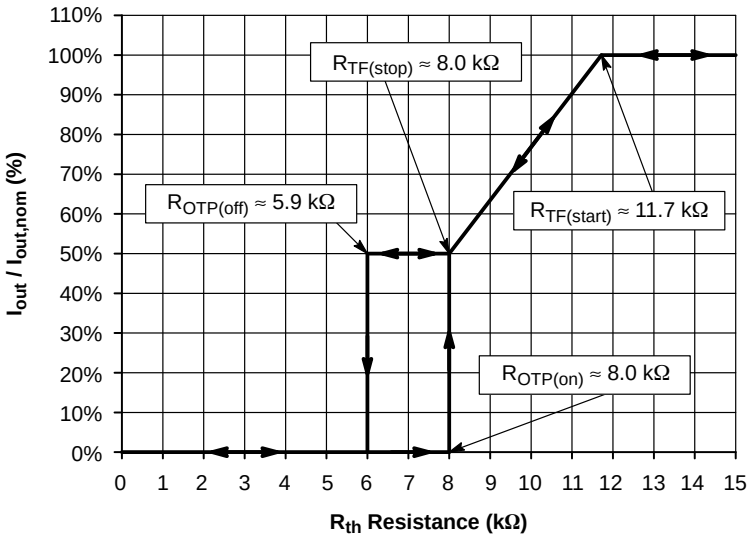


Figure 5. Thermal Foldback Characteristics and Over-Temperature Protection

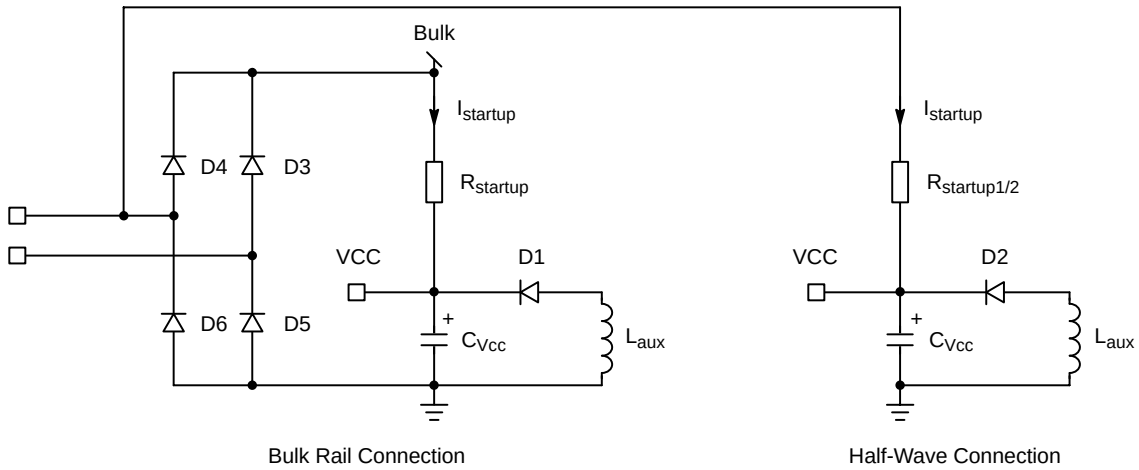


Figure 6. The Start-Up Resistor can be Connected to the Bulk Rail or to the Half-Wave

NCL30185 SPECIFIC ASPECTS

The step-dimming function decreases the output current from 100% to 5% of its nominal value in 3 discrete steps. Practically, the output current is reduced down to the next level whenever a brown-out event is detected*. Once the lower level is reached (5% of the nominal current), a brown-out event makes it return to its nominal level. As sketched by Figure 7, the step-dimming state is immediately reset if a brown-out fault is detected for more than the $T_{step\text{-}reset}$ time (3 s typically). The step-dimming state is also reset if V_{CC} drops below $V_{CC(reset)}$ (5 V typically).

*The NCL30185 detects a brown-out event whenever the V_S pin voltage remains below $V_{BO(off)}$ (0.9 V typically) for more than the *tBO*(*blank*) blanking time (25 ms typically). In this case, the circuit stops operation until the V_S pin voltage exceeds $V_{BO(on)}$ (1.0 V typically).

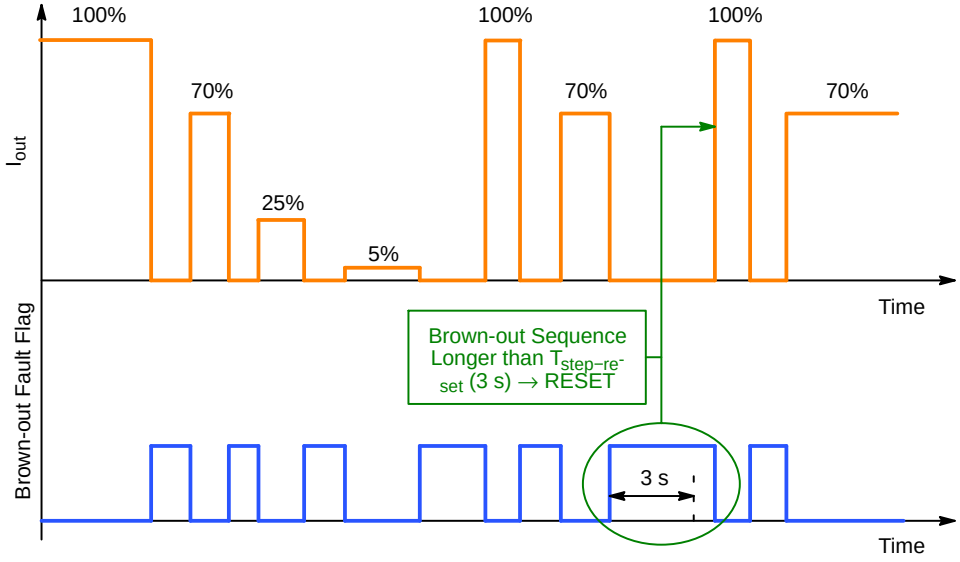


Figure 7. Step Dimming Operation

V_{CC} Circuitry Considerations

V_{CC} must keep above $V_{CC(off)}$ until the BO Event is Detected

V_{CC} must remain above its minimum operating voltage ($V_{CC(off)}$ − 8.8 V typically) until the NCL30185 detects a "step-diming brown-out event". If not, the circuit will not detect a step change but will simply enter the start-up mode and resume operation with the same LED current level. Proper step dimming operation hence requires that V_{CC} remains above $V_{CC(off)}$ for the BO blanking time. If this condition must be met for all steps, the worst case generally occurs at step 4 since the V_{CC} voltage is at its lowest level (see Figure 8).

Assuming that $V_{CC\text{-}step4}$ is the V_{CC} voltage at the lightest load, this requirement leads to:

$$C_{VCC,min} \cdot \frac{V_{CC-step4} - \left(V_{CC(off)}\right)_{max}}{I_{CC}} = \left(t_{BO(blank)}\right)_{max} \quad \text{(eq. 2)}$$

Or:

$$C_{VCC,min} = \frac{I_{CC} \cdot \left(t_{BO(blank)}\right)_{max}}{V_{CC-step4} - \left(V_{CC(off)}\right)_{max}} \quad \text{(eq. 3)}$$

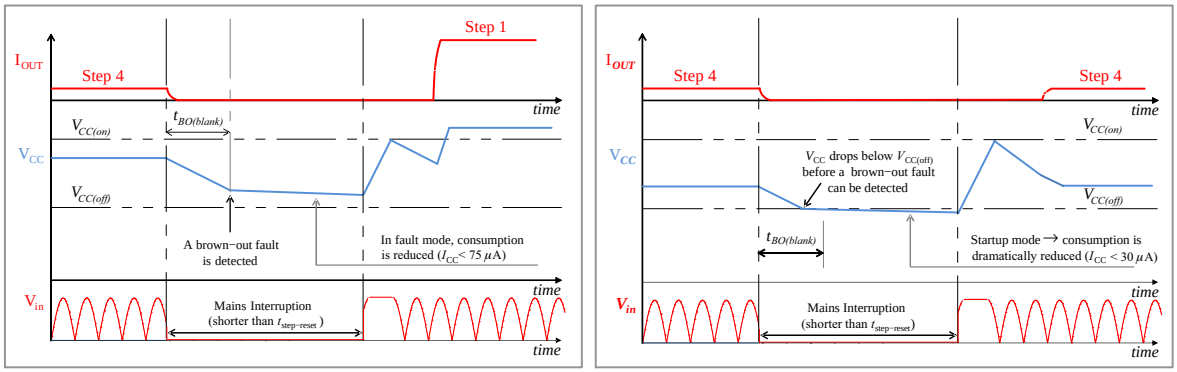


Figure 8. Proper Transition from Step 4 to Step 1 (Left) and Failure to Change the Step (Right)

At the lowest step, the switching frequency is dramatically reduced to about 25 kHz (frequency foldback). Thus, the MOSFET gate-charge contribution in the circuit consumption is generally very limited. I_{CC} can hence be approximated by I_{CC3} of the data sheet (4.5 mA maximum).

Finally, assuming that $V_{CC-step4}$ is 12.5 V:

$$C_{VCC,min} \geq \frac{4.5\ m \cdot 35\ m}{12.5 - 9.4} \cong 51\ \mu F \qquad \text{(eq. 4)}$$

V_{CC} must keep above $V_{CC(reset)}$ until the Target Resetting Time has Elapsed

The step-dimming state is reset if V_{CC} crosses $V_{CC(reset)}$ (5 V typically). Hence, for proper step-dimming operation, one must ensure that V_{CC} remains above $V_{CC(reset)}$ for any brown-out sequence not intended to return to the full-light state (shorter than the 3-s $T_{step-reset}$ time).

To help meet this requirement, the consumption is particularly reduced in fault mode ($I_{CC(sFault)}$ is 75 μA maximum) so that the V_{CC} voltage slowly decays for step-dimming brown-out events.

Assuming that V_{CC} is just above the minimum operating voltage ($V_{CC(off),max}$ = 9.4 V) when a 2.4-s step-dimming event occurs ($(t_{step-reset})_{min}$ = 2.4 s), the worst-case, necessary V_{CC} capacitor not to reset the circuit, is:

$$C_{VCC,min} = \frac{I_{CC(sFault)} \cdot \left(t_{step-reset}\right)_{min}}{V_{CC(off)max} - V_{CC(reset)max}} = \qquad \text{(eq. 5)}$$

$$= \frac{75\ \mu A \cdot 2.4\ s}{9.4 - 6.0} \cong 53\ \mu F$$

A 53-μF would hence ensure proper step-dimming operation with a good margin**.

** $C_{VCC,min}$ highly depends on the V_{CC} minimum voltage V_{CC} when the step-dimming event occurs. In our calculation, this minimum value (generally obtained at the lowest load step – 5%) is assumed to be just above the minimum voltage for operation. This is a worst-case. Also, in some applications, the step-dimming state may have to be stored for only 1.5 or 2.0 s.

Split V_{CC} Configuration

The two above required leads to a minimal V_{CC} capacitance to be implemented. However not to degrade the LED driver start-up, the V_{CC} capacitor should be limited to the value sufficient for nominal operation that is, $C_{VCC,min}$ of the design steps table (Table 3). To make this possible, it is recommended to implement the split V_{CC} configuration illustrated by Figure 9, where a minimized V_{CC} capacitor C_{VCC} ensures a fast start-up while a larger C_{tank} capacitor provides the necessary storage capability for step dimming.

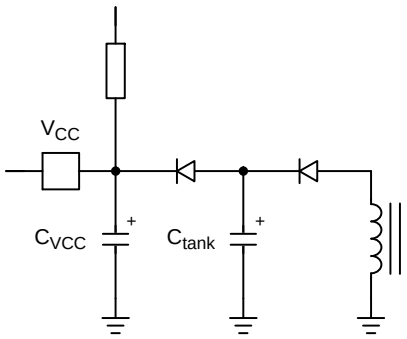


Figure 9. Split V_{CC} Configuration

In our application, we implement: C_{VCC} = 10 μF / 35 V and C_{tank} = 47 μF / 35 V.

EXPERIMENTAL DATA

Application Schematic

The application of Figure 10 has been used to obtain below experimental data.

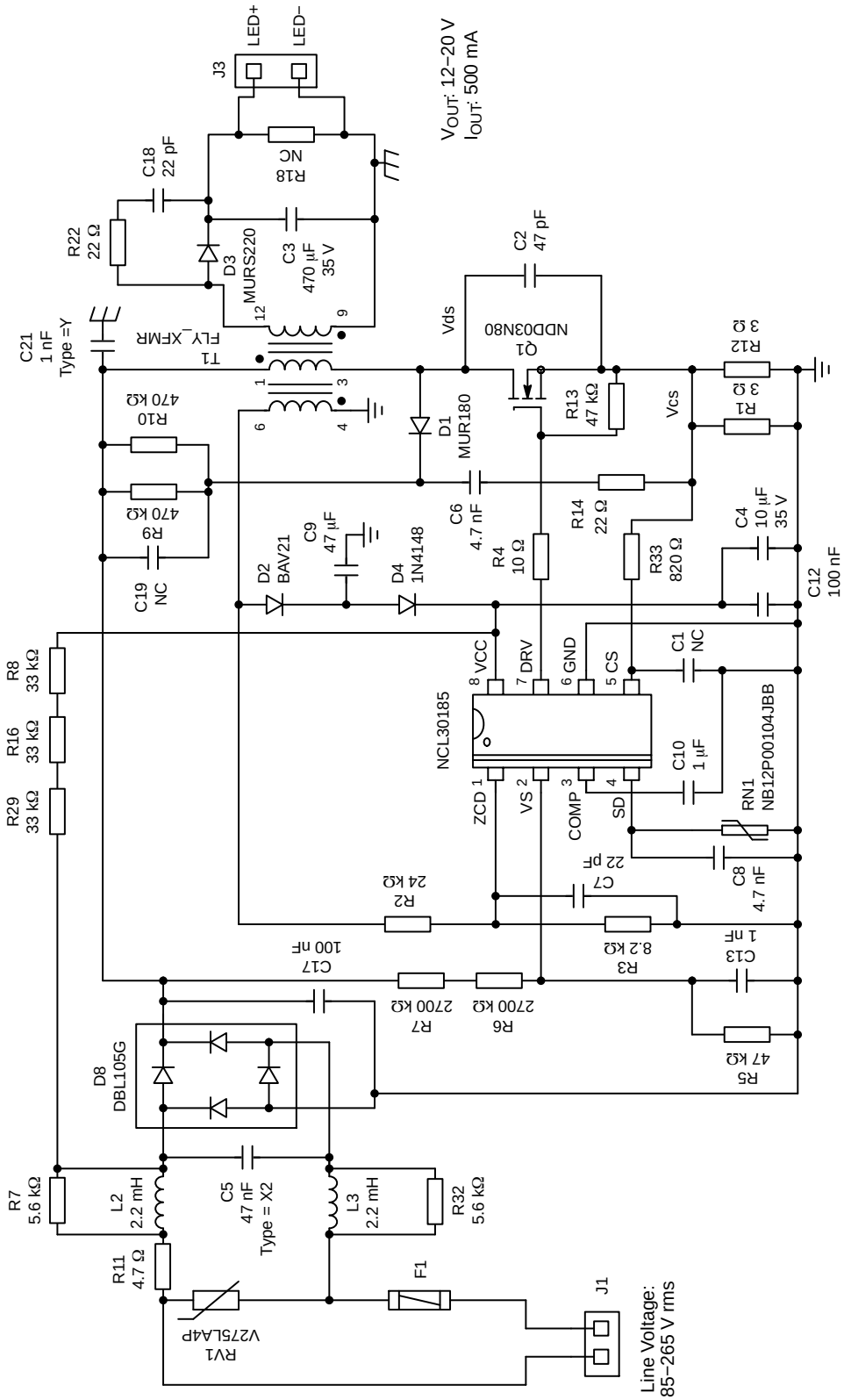


Figure 10. Application Schematic

Main Waveforms

Figure 11 provides some of the key waveforms. We can note that the line current is properly shaped for the three highest steps. At the lowest step, the power demand is too small to discharge the input filtering capacitor (C_{17} of Figure 10) near the line zero crossing. Hence, as attested by the current sense voltage (green trace of Figure 11), the input voltage and hence the line current cannot be sinusoidal.

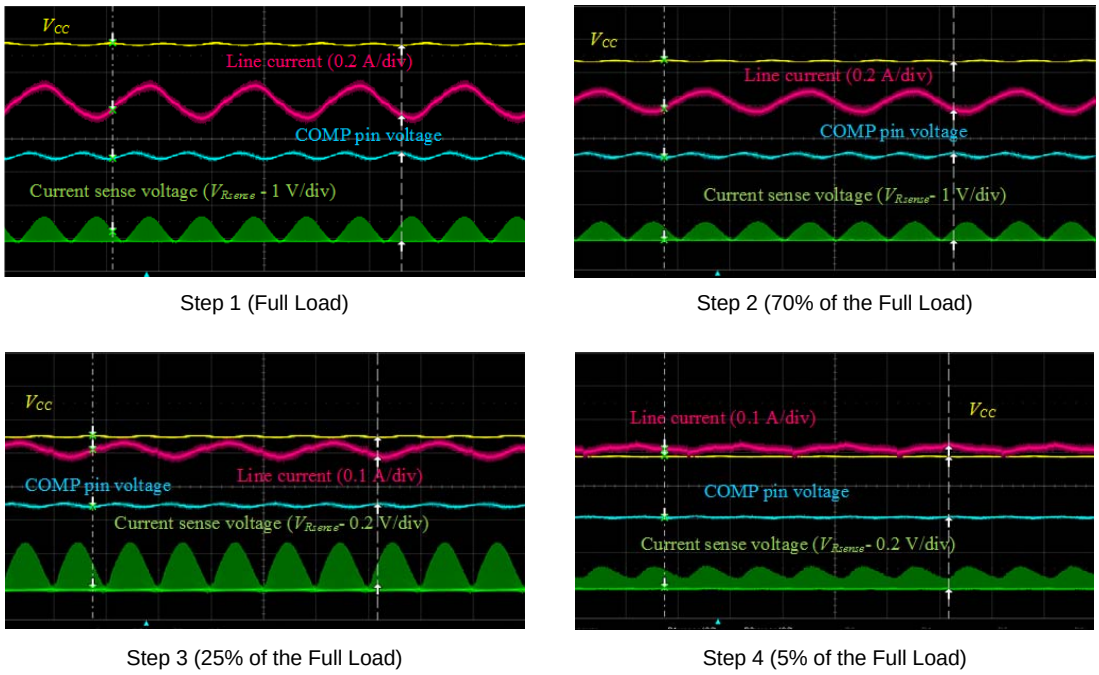
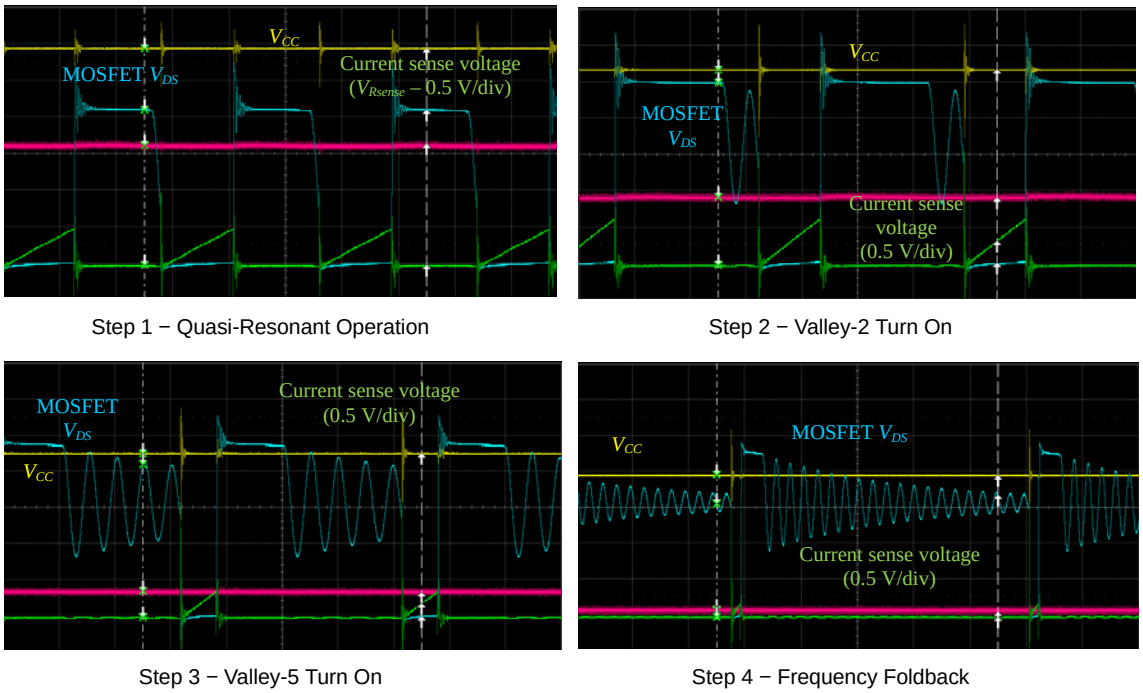


Figure 11. Main Waveforms @ 115 V rms / 60 Hz

Valley Lockout and Frequency Foldback

The NCL30185 implements a current-mode, quasi-resonant architecture which optimizes the efficiency over a wide load range, by turning on the MOSFET when its drain-source voltage is minimal (valley). When the second or third dimming step is engaged, the circuit changes valleys to reduce the switching losses. For stable operation, the valley at which the MOSFET switches on remains locked until the dimming step is changed. At the third dimming step, the circuit operates at the 5th valley (6th valley) in low-line (high-line) conditions. Step-4 switching frequency is further decreased by having the 5th valley (low line) or the 6th valley (high line) followed by an additional dead-time. This extra dead-time is typically 40 μs.

It is worth noting that high frequency operation would lead to small current levels in light-load conditions. Hence, valley lockout and frequency foldback not only optimize efficiency and reduce the power supply pollution (valley turn-on reduces noise and low-frequency operation helps pass EMI standard) but also contribute in maintaining a relatively high MOSFET peak current even at the least dimming step. This ensures a robust and accurate output current control in all steps.



Step 1 − Quasi-Resonant Operation

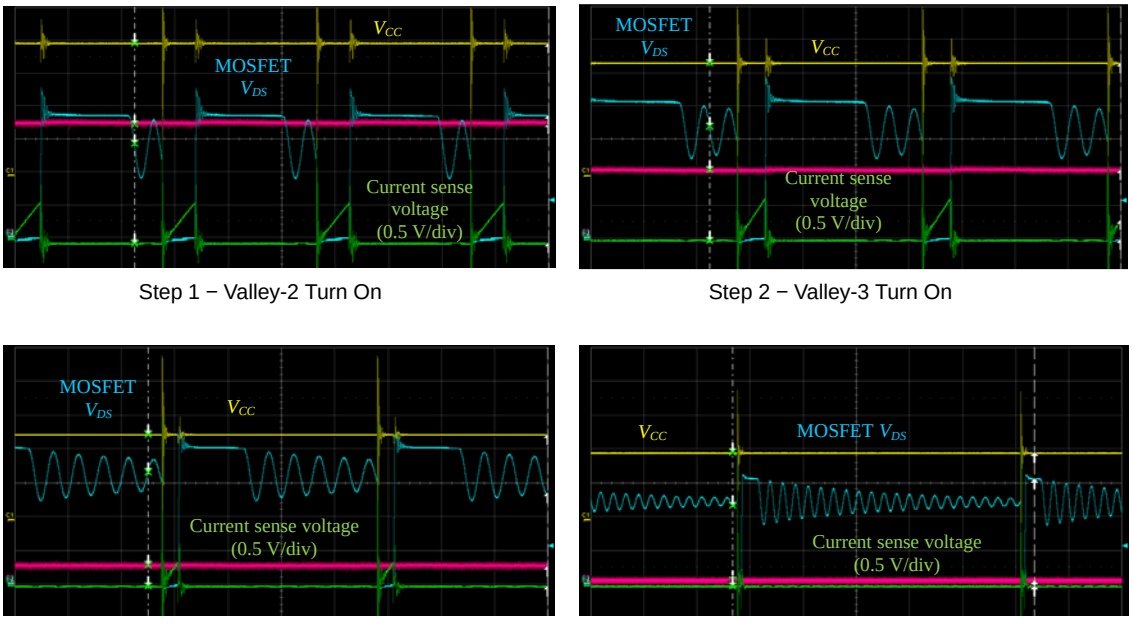
Step 2 − Valley-2 Turn On

Step 3 − Valley-5 Turn On

Step 4 − Frequency Foldback

Figure 12. The NCL30185 Low-Line Operation (115 V rms / 60 Hz)

The NCL30185 detects high-line conditions when the V_S pin voltage exceeds 2.4 V typically and remains in this state until the V_S pin voltage happens to drop below 2.3 V for 25 ms (typical values). In high-line conditions, switching losses generally are particularly critical. It is thus efficient to skip an additional valley to lower the switching frequency. At full load for instance, the NCL30185 turns on the MOSFET at the first valley in low-line conditions and at the second valley in high-line ones as shown by Figure 1. This helps operate with a strong current sense signal for a robust and accurate control even in the least-load cases.



Step 1 − Valley-2 Turn On

Step 2 − Valley-3 Turn On

Step 3 − Valley-6 Turn On

Step 4 − Frequency Foldback

Figure 13. The NCL30185 High-Line Operation (230 V rms / 50 Hz)

Output Current Control

Figure 14 shows the output current as a percentage of its nominal value. We can see that its characteristic is very flat with respect to the temperature. Thermal Foldback starts at about 80°C. As a result, the output current linearly decays to reach 50% of its step-dimming value at 95°C. The circuit stops operating (Over Temperature Protection) at 105°C. Operation can recover when the temperature drops down to 85°C. To obtain this characteristic, thermistor NB12P00104JBB manufactured by AVX, was connected to the SD pin.

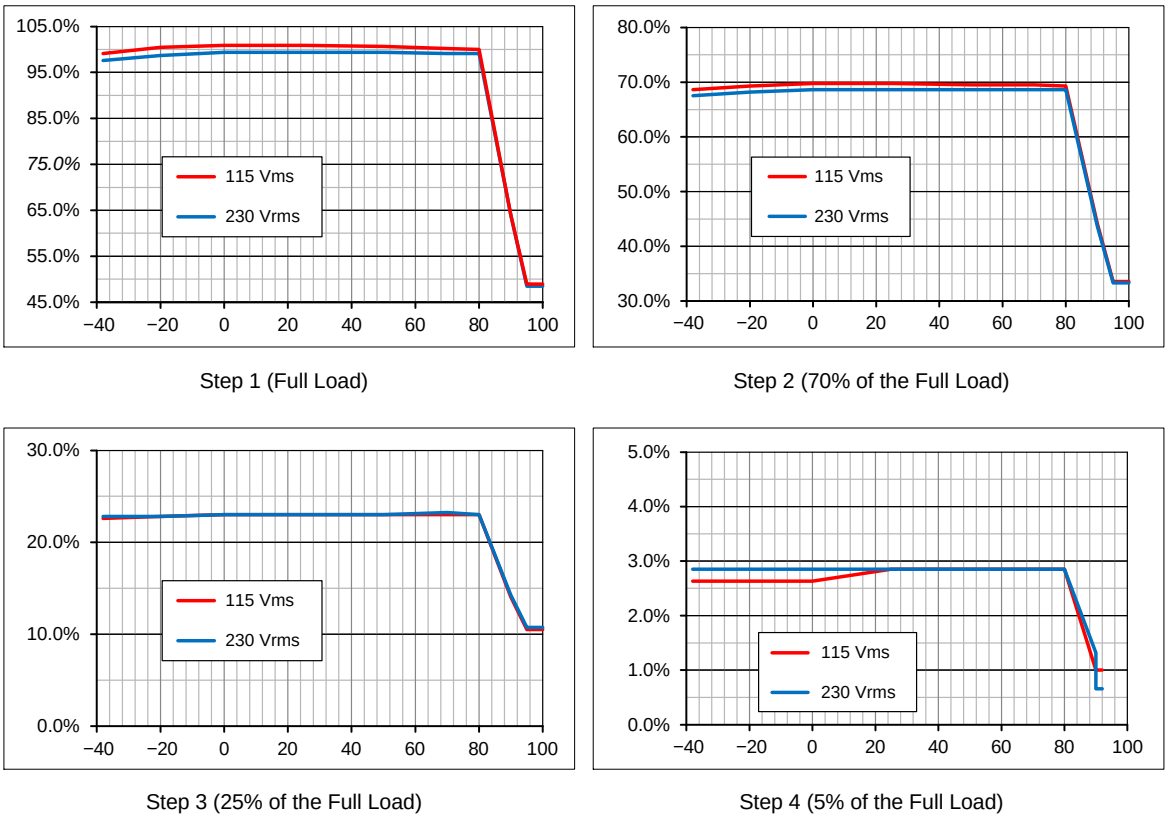


Figure 14. ($(I_{out} / I_{out,nom})$ (%)) vs. Temperature at the Four Different Dimming Steps

The LED current nicely matches the step-1 and step-2 target (100% and 70% of the nominal current). It is slightly below the expected level at steps 3 and 4 where the traditional sources of deviations discussed in [1] can have a more significant influence.

For instance, it is good remind that the LED driver controls the total current provided by the converter, i.e., the LED current plus the V_{CC} current and that hence, the actual output current is:

$$I_{out,nom} = \frac{N_P \cdot V_{REF}}{2 \cdot N_S \cdot R_{sense}} - \frac{N_{Aux}}{N_S} \cdot I_{CC} \qquad \text{(eq. 6)}$$

Also, if the current sense resistor is inductive, the LED current will be affected since the parasitic inductor causes the following offset on the CS pin voltage:

$$\left(\frac{I_{R_{sense}}}{L_P} \cdot v_{in}(t) \right)$$

where l_{Rsense} is the R_{sense} parasitic inductance.

Note that the application was developed re-using the NCL30188-driven, no-dimming board designed to full-light operation described in [1]. If needed, specific actions could be engaged to mitigate aforementioned effects and optimize lowest steps operation.

Power Factor Performance

Figure 15 shows the power factor measured at full load at two different line magnitudes (115 V rms and 230 V rms). No thermistor was connected to the SD pin (no thermal foldback) for this measurement. The power factor is extremely stable over the considered temperature range (from −40°C to 90°C).

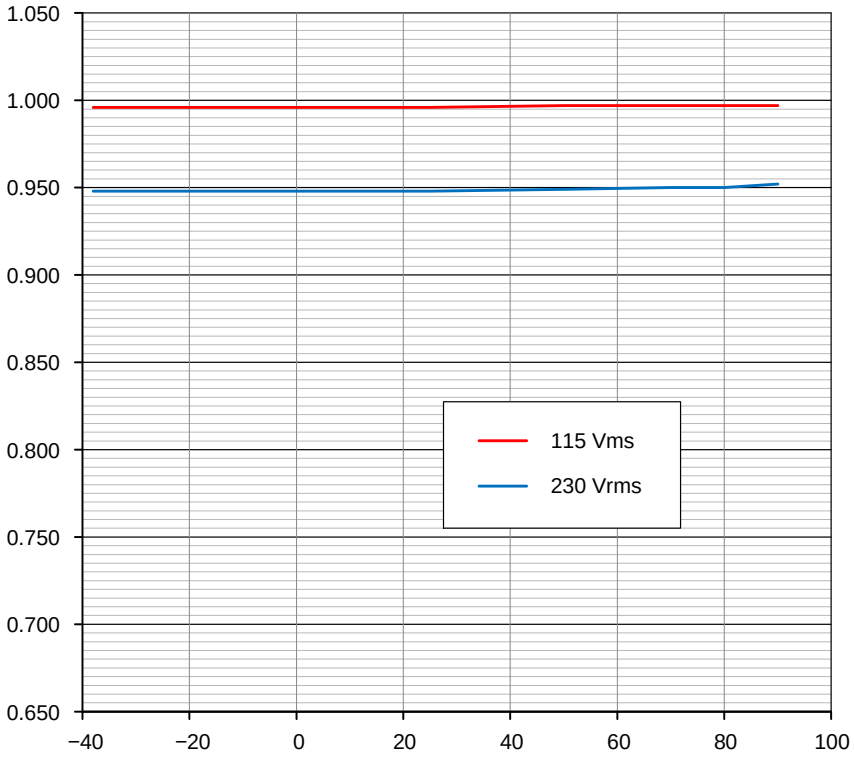


Figure 15. Power Factor (Step 1) vs. Temperature (No Thermistor on the SD Pin)

Safety Performance

The NCL30185 incorporates the same large suite of protections as the NCL30085 and in particular, the capability to face shorted /open situations of the LED string or an output diode failure. Some experimental data on the circuit under such faults can be found in [1].

REFERENCES

[1] Joel TURCHI, “4 Key Steps to Design a NCL30188-Controlled LED Driver”, Application Note AND9451/D.

[2] Joel TURCHI, “NCL30088 and NCL30085 Safety Tests Consideration”, Application Note AND9204/D.

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