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Methods to Identify Shoot Through in Fast Switching VRM Applications

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APPLICATION NOTE

Introduction

A voltage regulator module (VRM) is a DCDC converter that powers a microprocessor, usually converting 12 V to 1.2 V. For VRM applications, synchronous buck converter has been the topology of choice for decades due to circuit simplicity and high efficiency. The major switching component in VRM is low voltage MOSFETs.

Due to the latest technology developments, MOSFET switching losses has been significantly reduced, allowing VRM switching frequency to increase significantly. Currently, VRM application switching frequency at 600 kHz, with a push forwards 1 MHz in the future. The significantly reduction in switching loss has allowed MOSFET to switching faster, dramatically increasing the dv/dt of the switching loop. In modern VRM designs the dv/dt can be as high as 12 V/ns. Modern fast switching MOSFETs also experience high di/dt. The di/dt of the switching loop can be as high as 10 A/ns. High dv/dt and di/dt cause significant interaction between device and circuit parasitics. In some situations these interactions cause shoot, which is very harmful for both efficiency and reliability. Methods to reduce shoot through loss are identified by Alan Elbanhawy in [1].

While circuit susceptibility to cross conduction has been identified, these circuit conditions have primarily been analyzed mathematically [2]. This application note focuses primarily on experimental identification of shoot through.

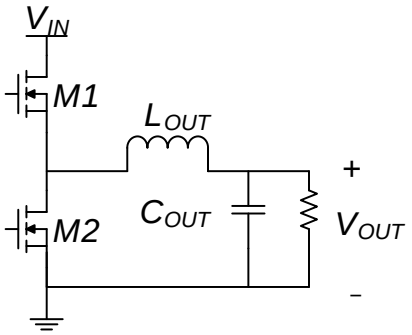

Figure 1. A synchronous buck converter used in VRM

Difficulties Identifying Shoot Through

Shoot through is difficult to identify unless it is so serious that the efficiency of the synchronous buck converter is significantly decreased or damage occurs to the MOSFETs. It is difficult to identify shoot through due to the following:

It is impossible to measure the gate−source voltage of MOSFET channel oxide directly for HS or LS.

The Vgs seen at the die level cannot be directly measured due to the die packaging. The closest measurement points are located at the package pin. Parasitic inductance of gate and source pins and parasitic gate resistance of silicon die are included in measurements. With interactions of package inductance and parasitic gate resistance, it is really difficult to know whether gate−source voltage on silicon channel is higher than threshold voltage or not.

It is impossible to measure current in switching loop due to the compact circuit design.

For VRM, the synchronous buck converter is optimized for high frequency switching and the switching loop parasitic inductance is minimized to 1nH~2nH. Any current measurement component added to the circuit will significantly change the parasitic inductance and will result in inaccurate measurements.

Because the measurements internal to the package cannot be made, clues to the presence of shoot through must be deciphered from the external gate and switching node waveforms.

Shoot Through Types and Mechanisms

Three types of shoot through have been identified based on the cause. Overall, there are three types of shoot through. Type #1: Driver caused shoot through, Type #2: Ringing of gate driving circuit caused shoot through, and Type #3: fast turn−on/off caused shoot through. Definitions of three types of shoot through and their reasons are listed in Table 1.

Historically, shoot through has not been as significantly due to the slower switching capability of the MOSFETs. Slower MOSFET turn−on and turn−off minimizes interactions with circuit parasitics and means longer deadtime. However, modern fast switching MOSFETs have significantly increased the MOSFET turn−on and turn−off speed, resulting a significant increase in dv/dt and di/dt.

Table 1. Summary of three types of shoot through

Type of shoot through	Definitions	Circuit Reasons	Design Requirements
Type #1: Driver caused shoot through	Dead time is too short. Driver turns−on one MOSFET before the other turns−off	Not enough deadtime to cover both turn−on and turn−off time	Deadtime is usually minimized for fast switching MOSFETs, but must be longer than low side turn−off time
Type #2: ringing of Gate driving circuit caused shoot through	Damping ratio of driving circuit is not large enough. Ringing in gate driving circuit causes VGS higher than VTH.	Damping ratio of gate driving circuit $\frac{R_G}{2}\sqrt{\frac{C_{ISS}}{L_G}}$ is not large enough to damping gate ringing	Gate driving resistance is usually designed to be low to achieve fast switching. However, it must be large enough to damping gate ringing. This mechanism apply to both high side MOSFET and low side MOSFET
Type #3: fast turn−on/off caused shoot through	Caused by fast switching dv/dt and di/dt of main circuit. Transient response of main switching circuit causes VGS higher than VTH	The high dv/dt and di/dt in main switching circuit caused CGS charged above VTH	This mechanism apply only to high side MOSFET turn−on/off intervals. Three sub−cases: 1. dv/dt charge CGS above VTH 2. di/dt charge CGS above VTH 3. dv/dt turn−on interval BJT

For fast switching MOSFETs, dv/dt and di/dt causes high voltage on the gate that may be comparable with threshold voltage of MOSFET, especially for low threshold devices. In addition to faster turn−on and turn−off times, the deadtime between HS and LS MOSFETs has significantly decreased. A 15 ns deadtime is common in modern VRM design, and is too short a time to settle down the circuit parasitics interactions. Shoot through occurs during high side turn−on and high side turn−off. However, shoot through at HS turn−off is not as severe. The total input energy is limited due to the HS turn−off.

Type 1: Driver Caused Shoot Through

Driver caused shoot through is the least common type due to adaptive dead time control technique of driver [3]. However, PCB layout can interfere with the adaptive deadtime control when long traces or large gate resistance is presented. The driver sees a different voltage than what is presented at the MOSFET pins.

Type 2: Ringing of Gate Driving Circuit Caused Shoot Through

The MOSFET internal gate resistance dampens any ringing seen on the gate. However, in modern fast switching MOSFETs, the Rg has been significantly reduced, making it more susceptible to turn−on. Care must be taken to adjust the external Rg and boost strap resistance to ensure that the gate driving circuit tis well damped.

Type 3: Fast turn−on/off Caused Shoot Through

The third case is becoming more prevalent in VRM applications due to the fast switching MOSFETs. A faster turn−on and turn−off makes the MOSFET more susceptible to di/dt and dv/dt. When dv/dt induced turn−on occurs, the MOSFET is turned on through the gate oxide or the internal BJT turns on through pn junction at source side. Dv/dt caused turn−on of the interval BJT will be analyzed in a separate article.

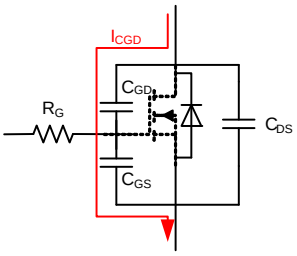

Figure 2. dv/dt caused turn−on through gate oxide

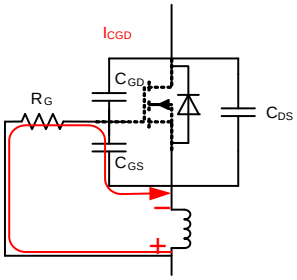

Figure 3. di/dt caused turn−on through gate oxide

The physics of dv/dt and di/dt caused MOSFET turn−on through gate oxide is shown in Figure 2 and Figure 3. As shown in Figure 2, dv/dt causes a current flow through C_{GD} by $I_{CGD}=C_{GD}*dv/dt$. Since the gate driving path of the MOSFET is a high impedance path comparing to the path from gate to source through C_{GS}, the majority of the current flowing through C_{GD} will flow through C_{GS}. As a result, dv/dt on drain side causes a gate bounce on C_{GS}. As can be seen in Figure 2 and Figure 3, C_{GD} and C_{GS} form a voltage divider. As long as V_{DS} remains below $V_{TH}*(C_{GS}+C_{GD})/C_{GD}$, gate bounce on C_{GS} is guaranteed to remain below the threshold voltage of the device. Taking into nonlinearity of C_{GS} and C_{GD}, the criteria to prevent dv/dt caused shoot through is $Q_{CGD}(V_{DS})<Q_{CGS}(V_{TH})$. Here, $Q_{CGD}(V_{DS})$ is the charge to charge C_{GD} from zero voltage to voltage V_{DS}, $Q_{CGS}(V_{TH})$ is the charge to charge C_{GS} from zero voltage to threshold voltage.

The Impact of di/dt depends on the amount of parasitic inductance. In VRM, the Ls of HS is a common source inductance. Due to di/dt, voltage on common source inductance charges C_{GS} when this voltage drives a current flowing positively through gate driving path. This positive gate driving current charges C_{GS} and may cause shoot through too. This process is shown in Figure 3. In order to reduce di/dt caused shoot through, the common source inductance of the low side MOSFET must be minimized.

METHOD 1: IDENTIFY SHOOT THROUGH BY VOLTAGE WAVEFORMS

Customers commonly ask for insights about their circuits, providing only the MOSFET gate and driving waveforms. It can be difficult to obtain the full details of the application circuit.

Fortunately, shoot through can be identified by analyzing the phase node, high side gate and low side gate waveforms. Figure 4 and Figure 5 show the standard phase node and low side gate waveforms without shoot through. The high side turn−on transient can be divided into five distinct intervals and these five intervals happen in sequence. Turn−on intervals:

Low side gate turn−off interval ①: During this interval, gate voltage of low side gate drop to zero volts.

Deadtime interval ②: Low side diode conducts. During this interval, phase node voltage drop from about −50 mili−volts (or less) to about −0.7 V, which is the pn junction voltage of regular diode.

Di/dt dominates interval ③: Current of high side MOSFET increases from zero to load current. Di/dt that lift phase node voltage a little along with the parasitic inductance from phase node to ground. This interval can be identified by a small step in phase node voltage before phase node voltage increase rapidly to input voltage.

Dv/dt dominates interval ④: This interval corresponds to the rapid increase in phase node voltage from initial step (the step in interval ③) to input voltage.

Natural ringing interval ⑤: High side is fully on and low side is fully off, ringing caused by switching loop inductance and low side output capacitance continues until been totally damped.

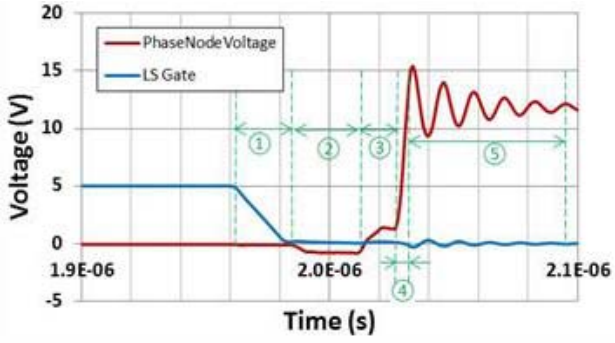

Figure 4. Standard phase node waveforms and transient time sequence during HS turn−on

The typical transient of high side turn−off can be divided into three intervals.

Dv/dt and di/dt interval ①: High side MOSFET turn−off, the voltage on high side MOSFET increases from zero volt to input voltage. During this interval, phase node voltage drops from input voltage to zero volts. Due to large output capacitance of low side MOSFET in VRM application, voltage reduction on low side MOSFET bypass a large portion of load current, which results in high side current reduces at the same time with phase node voltage reduces.

Di/dt dominates interval ②: Current of high side MOSFET decreases from high current to zero current. During this interval, current of high side MOSFET completely switches to low side MOSFET, which results a di/dt that pull phase node voltage below zero volt with the parasitic inductance from phase node to ground. This interval can be identified by a small step below zero volts in phase node voltage before phase node voltage is clamped to −0.7 V.

Deadtime interval and ringing interval ③: After high side is fully turned−off, diode of low side MOSFET is conducting. During this interval, phase node voltage is clamped to −0.7 V. After this interval, low side MOSFET will turn−on and phase node voltage will be around −50 mili−Volts or less.

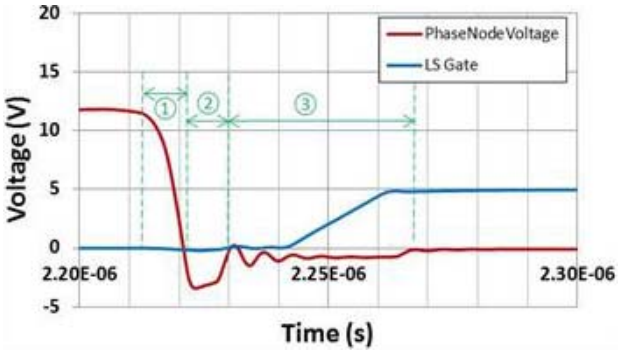

Figure 5. Standard phase node waveforms and transient time sequence during HS turn−off

Based on understanding about switching transient, as shown in Figure 4 and Figure 5, switching transient with shoot through could be identified through waveform diagnostics.

Methods to identify shoot through are explained in the following sections. (One substantial requirement for phase node waveform that can be used to identify shoot through is that measurement must be clear and clean without too much noise and measurement error. In order to have clear and clean phase node waveform and gate waveforms, the measurement ground must be the same ground of input capacitance. Also, the probing loop must be as small as possible.)

Waveform Signatures of Type 1

The phase node waveforms without shoot through are smooth ringing waveform. Phase node waveform should be standard step response of second order system with a small initial step (caused by di/dt on loop inductance). However, the gate overlay shoot through caused un−smoothness in waveform at interval ④ and ⑤. Without shoot through, the phase node waveforms are sinusoidal with a smoothing. Shoot through distorts the phase node waveforms, causing a clipping/flattering of the first peak.

Major empirical signatures:

Phase node voltage with distortion that is obviously different from step response of second order system is observed at interval ④ and ⑤ when high side turn−on, as waveforms signatures exemplified by Figure 6.

Phase node waveform does not rise/fall linearly, this means shoot thought caused by gate overlay, as waveform signatures exemplified by Figure 6 and Figure 7.

These are two major criteria to identify gate overlay shoot through by waveform.

Supporting signatures: No diode conduction (which means phase node voltage goes −0.7 V before/after high side MOSFET turn−on/off) should be observed in phase node waveform if gate overlay shoot through happens. If −0.7 V is observed in phase node waveforms, it means not gate overlay shoot through happened in that switching transient.

Supporting signatures: compare high side and low side gate voltage waveform and check the deadtime between them. If the deadtime is sufficiently long, no gate overlay shoot through happens in circuit. Specifically, if deadtime is about 20 ns or less, it has a chance to have gate overlay shoot through. If deadtime is longer than 20 ns, it has less change to have gate overlay shoot through.

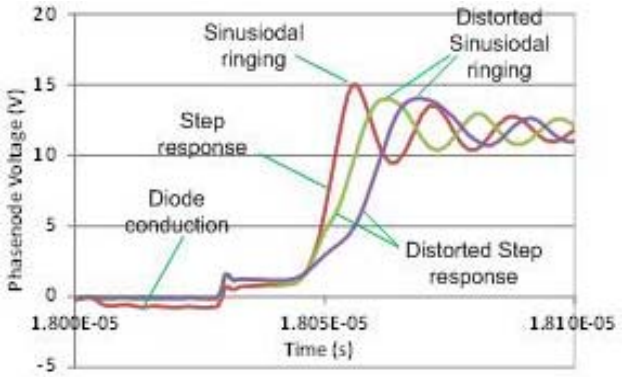

Figure 6. Phase node waveforms at turn−on transient with/without gate overlay shoot through red: no shoot through, green: with shoot through, purple: with severe shoot through

Overall, to identify shoot through due to gate overlay, the waveform of phase node rise/fall linearly is the key. If un−linearly rise/fall is captured, it means gate overlay shoot through happens. Besides this feature, phase node ringing waveforms also could be used to identify gate overlay shoot through during turn−on interval. Phase node ringing cannot be used to identify gate overlay shoot through during high side turn−off interval.

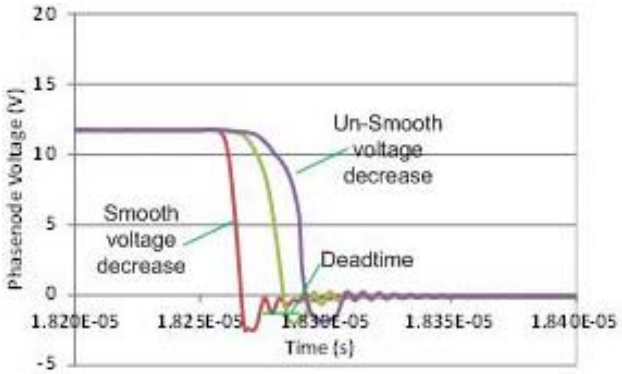

Figure 7. Phase node waveforms at turn−off transient with/without gate overlay shoot through red: no shoot through, green: with shoot through, purple: with severe shoot through

Waveform Signatures of Type 2

Gate ringing caused shoot through is easy to identify by waveforms. This is because gate voltage is easy to measure.

Major signature: gate waveform should be a decaying ringing waveform. If gate waveform is trimmed about the level of threshold voltage, as exemplified in Figure 8 and Figure 9, it means a shoot through caused by gate ringing.

Supporting signature: phase node waveform has some distortion in sinusoidal ringing waveform.

This method is direct waveform method and direct experiment method. No special experiment is needed to identify gate ringing caused shoot through since it is so easy to measure directly.

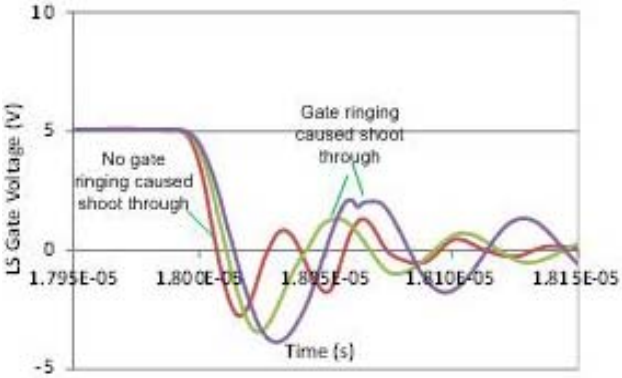

Figure 8. Low side gate−source waveforms at high side turn−on transient with/without gate ringing shoot through red: no shoot through, green: with shoot through, purple: with severe shoot through

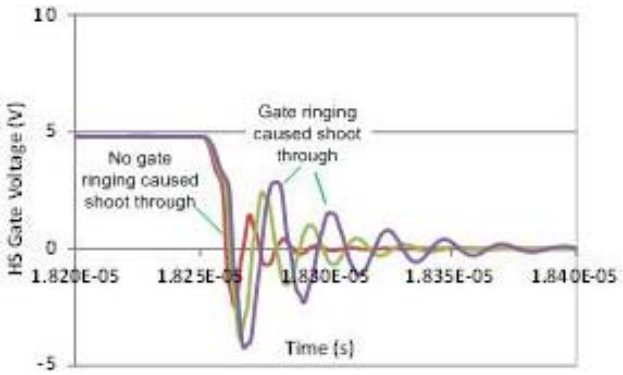

Figure 9. High side gate−source waveforms at high side turn−off transient with/without gate ringing shoot through red: no shoot through, green: with shoot through, purple: with severe shoot through

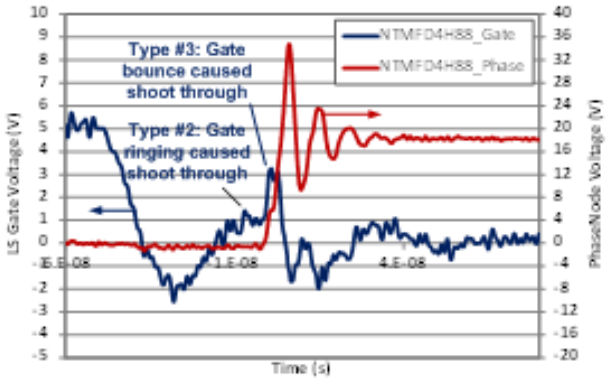

Figure 10. Low side gate−source waveforms at high side turn−on transient with gate bounce shoot through

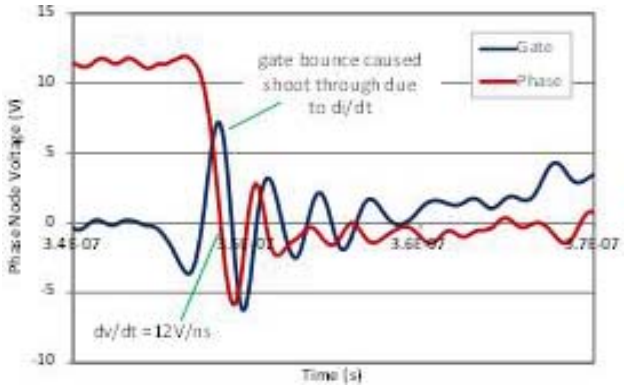

Figure 11. Low side gate−source waveforms at high side turn−off transient with gate bounce shoot through

Waveform Signatures of Type 3

When high side MOSFET is turning−on, both dv/dt and di/dt could cause shoot through during this interval. Gate bounce caused shoot through during high side turn−on transient could be identified by the following characteristics:

Major empirical signature: when high side is turning−on, if shoot through happens in phase node voltage rising interval, it means a dv/dt caused shoot through. If the shoot through happens during high side current increasing interval, it is di/dt caused shoot through. As is exemplified by blue line in Figure 10.

Supporting identification: distorted voltage rising waveforms is observed in phase node or non−sinusoidal ringing is observed in the phase node waveforms, as exemplified by red line (rising with a sharp spike) in Figure 10.

When high side MOSFET is turning−off, dv/dt is not a problem since it is negative. However, di/dt could cause shoot through during this interval. Di/dt caused shoot through during high side turn−off interval could be identified by the following characteristics:

Major identification: phase node waveform decreases with slope higher than it should be. Normally the negative dv/dt is around 5 V/ns. If the phase node voltage drops higher than 5 V/ns, it is skeptical to di/dt caused shoot through, as exemplified by the red line in Figure 11. The negative dv/dt is as high as 12 V/ns in Figure 11, which is highly suspectable.

Supporting identification: when high side is turning−off, if a spike on gate−source voltage of low side MOSFET goes to threshold voltage before or during phase node voltage decreasing interval, shoot through happens, as exemplified by the blue line in Figure 11.

Additional Waveform Signatures

Each type of shoot through rarely cause shoot through problem individually. On the real application board, each type of shoot through physics elevates gate bounce a little bit, which may results in severe shoot through all together. This feature can be observed in Figure 10. Obviously, in Figure 10, shoot through happens when high side MOSFET is turning−on. This shoot through happens because of the combination of both type #2 shoot through and type#3 shoot through. Due to gate ringing of low side MOSFET, gate source voltage is ringing to about 1 V at the moment when high side is turning−on. When high side is turning−on, the high dv/dt inject current through CGD, as explained in Figure 2. As a result of both effects, VGS of low side MOSFET is charged to 3 V, which is way higher than threshold voltage of low side MOSFET (the real gate−source voltage, which is internal gate−source voltage on channel oxide, is around threshold voltage).

The signature of low side gate−source waveform for shoot through when high side is turning on is that gate−source voltage is trimmed around threshold voltage level, as shown in Figure 12. This is because shoot through during high side turning−on tends to turn−off the low side MOSFET, which function as a feedback to maintain low side gate−source voltage flat. The signature of low side gate−source waveform for shoot through when high side is turning off is that gate−source voltage is ringing significantly above threshold voltage level, as shown in Figure 13. This is because the shoot through during high side turning−off causes high current in power switching loop and tends to turn−off high side faster, which results in really fast switching off of high side MOSFET.

The shoot through signature of phase node waveform can be seen as waveform distortion. As shown in Figure 14, there is a slightly distortion in phase node ringing, which could be contributed by shoot through. Also, as shown in Figure 15, phase node voltage rises with multiple slopes, which indicates that shoot through happens in circuit.

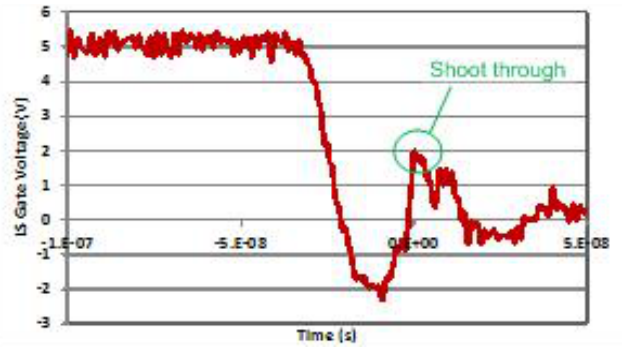

Figure 12. Shoot through signature of low side gate−source voltage when high side is turning on

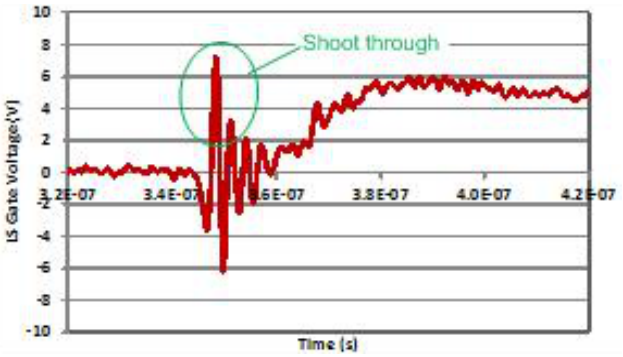

Figure 13. Shoot through signature of low side gate−source voltage when high side is turning off

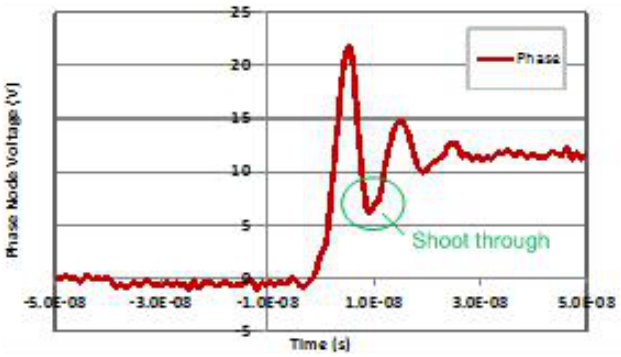

Figure 14. Shoot through signature of phase node during phase node ringing interval after high side is turned on

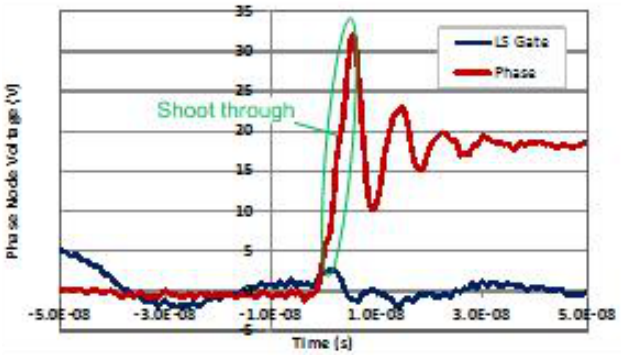

Figure 15. Shoot through signature during phase node rising interval when high side is turning on

METHOD 2: IDENTIFY SHOOT THROUGH BY CIRCUIT MODIFICATION

In some cases, due to measurement noise and difficulties, it is hard to identify shoot through simply by waveforms of phase node. In these cases, experiments with modified circuit could help identify shoot through.

Below are three circuit modification methods to identify shoo through.

Experiment method #1: change drivers with longer deadtime. With longer deadtime, the chance of all three kinds of shoot through would be reduced. If the efficiency is higher with longer deadtime driver, shoot through happened in original circuit.

Experiment method #2 [4]: Use gate voltage shifter and achieve negative gate bias, then plot loss vs negative bias, see efficiency variation. This method is valid for all three kinds of shoot through.

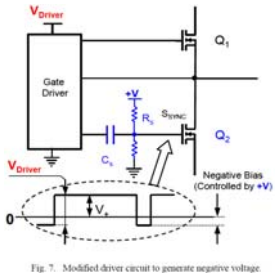

Fig. 7. Modified driver circuit to generate negative voltage.

Figure 16. Experiment Circuit

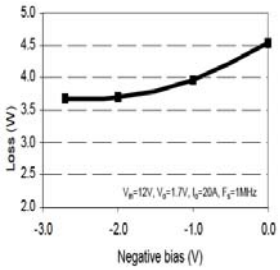

Figure 17. Efficiency Variation

As shown in Figure 16 and Figure 17, gate voltage will be pulled down to a negative voltage. This bi−voltage driver help reduce all three kinds of shoot though. Compare efficiency as various negative driver voltages, shoot through can be identified. If efficiency is higher as negative gate voltage increases, shoot through happens in circuit.

Experiment method #3: Short gate of low side MOSFET to ground and then compare phase node waveforms without shorting low side gate. Comparing phase node waveform of buck circuit and synchronous buck converter, if obvious difference is observed in phase node waveform of synchronous buck circuit, shoot through happens in circuit.

Conclusion

Shoot through in VRM are categorized into three groups. Reasons for each kind of shoot through are presented. Two major methods, waveforms diagnostics and circuit modification, are presented to identify shoot through in VRM.

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