1. Product synopsis

This application handbook is intended to provide practical guidelines for the STK57FU394A-E use.

The STK57FU394A-E is Intelligent Power Module (IPM) based upon ONs Insulated Metal Substrate Technology (IMST) for 3-phase motor drives which contain the PFC circuitry, the main power circuitry and the supporting control circuitry.

The key functions are outlined below:

- Highly integrated device containing all High Voltage (HV) control from HV-DC to 3-phase outputs in a single small SIP module.
- Output stage uses IGBT/FRD technology and implements Under Voltage Protection (UVP) and Over Current Protection (OCP) with a Fault Detection output flag. Internal boost diodes are provided for high side gate boost drive.
- Option of a combined or individual shunt resistor per phase for OCP.
- Externally accessible embedded thermistor for substrate temperature measurement.
- All control inputs and status outputs are at low voltage levels directly compatible with microcontrollers.
- Single control power supply due to internal bootstrap circuit for high side pre-driver circuit.
- Mounting points are available on SIP package.

A simplified block diagram of a motor control system is shown in Figure 1.

![Motor Control System Block Diagram](image-url)
2. Product description

Table 1 gives an overview of the device, for a detailed description of the packages refer to Chapter 6.

<table>
<thead>
<tr>
<th>Device</th>
<th>STK57FU394A-E</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>SIP2A – horizontal pins</td>
</tr>
<tr>
<td>Voltage (VCEmax.)</td>
<td>600V</td>
</tr>
<tr>
<td>Current (Ic)</td>
<td>15A</td>
</tr>
<tr>
<td>Peak current (Ic)</td>
<td>30A</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>2000V</td>
</tr>
<tr>
<td>Shunt resistor</td>
<td>triple shunts / external</td>
</tr>
</tbody>
</table>

Table 1. Device Overview

The high side drive is used with a bootstrap circuit to generate the higher voltage needed for gate drive. The Boost diodes are internal to the part and sourced from VDD (15V). There is an internal level shift circuit for the high side drive signals allowing all control signals to be driven directly from Vss levels common with the control circuit such as the microcontroller without requiring external level shift such as opto isolators.

Figure 2. Equivalent circuits
3. Performance test guidelines

The following Chapter gives performance test method shown in Figures 3 to 7.

3.1. Switching time definition and performance test method

Figure 3. Switching time definition

Figure 4. Evaluation circuit (Inductive load)

Figure 5. Switching loss circuit
Figure 6. R.B.SOA circuit

Figure 7. S.C.SOA circuit
3.2. Thermistor characteristics

The thermistor is built-in between TH and VSS. This is used to sense the temperature of the internal module. Its characteristic is outlined below.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Min</th>
<th>Typ.</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance</td>
<td>( R_{25} )</td>
<td>Tc=25°C</td>
<td>99</td>
<td>100</td>
<td>101</td>
<td>kΩ</td>
</tr>
<tr>
<td>Resistance</td>
<td>( R_{100} )</td>
<td>Tc=100°C</td>
<td>5.18</td>
<td>5.38</td>
<td>5.60</td>
<td>kΩ</td>
</tr>
<tr>
<td>B-Constant(25-50°C)</td>
<td>B</td>
<td></td>
<td>4208</td>
<td>4250</td>
<td>4293</td>
<td>K</td>
</tr>
<tr>
<td>Temperature Range</td>
<td></td>
<td></td>
<td>-40</td>
<td>+125</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

*Table 2. NTC Thermistor value*

\( R_{25} \) is the value of the built-in NTC thermistor at \( T_c=25°C \). The resistance value is \( 100\,\text{kΩ} \pm 1\% \) and the value of the B-Constant (25-50°C) is \( 4250\,\text{K} \pm 1\% \). The resistance value \( R(t) \) depended on the temperature is calculated by the following formula.

\[
R(t) = R_{25} \times e^{B \left( \frac{1}{T - 298} \right)}
\]

* The constant \( T \) is the absolute temperature value.

The result in the NTC values over temperatures

*Figure 8. typical NTC value over temperature*
4. Protective functions and operation sequence

This chapter describes the protection features.

- Over current protection
- Short circuit protection
- Under voltage lockout (UVLO) protection
- Cross conduction prevention

4.1. Over current protection (OCP)

STK57FU394A-E module utilizes an external shunt resistor for the OCP functionality. As shown in Figure 9, the emitters of all three lower side IGBTs brought out to module pins. An external OCP circuitry consists of the shunt resistor and an RC filter network.

![Figure 9. Over-current protection circuit setting](image)

The OCP function is implemented by comparing the ITRIP(PFCTRIP) input voltage with an internal reference voltage of 0.49V (typ) for inverter part, -0.31V (typ) for PFC part. In case the voltage on this terminal i.e. across the shunt resistor exceeds the trip level an OCP fault is triggered.

Note: The current value of the OCP needs to be set by correctly sizing the external shunt resistor to less than 2x of the modules rated current.

In case of an OCP event all internal gate drive signal for the IGBTs become inactive and the fault signal output (FLTEN) is activated (low).

A RC filter is used on the ITRIP(PFCTRIP) input to prevent an erroneous OCP detection due to normal switching noise or recovery diode current. The time constant of that RC filter should be set to a value between 1.5μs to 2μs. In any case the time constant must be shorter than the IGBTs short current safe operating area (SCSOA). Please refer to data sheet for SCFOA. The resulting OCP level due to the filter time constant is shown in Figure 10.
For optimal performance all traces around the shunt resistor need to be kept as short as possible.

Figure 11 shows the sequence of events in case of an OCP event.
4.2. Under Voltage Lockout Protection

The UVLO protection is designed to prevent unexpected operating behavior as described in Table 3. Both High-side and Low-side have UV protecting function. However the fault signal output only corresponds to the Low-side UVLO Protection. During the UVLO state the fault output is continuously driven (low).

<table>
<thead>
<tr>
<th>VDD Voltage (typ. Value)</th>
<th>Operation behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 12.5 V</td>
<td>As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.</td>
</tr>
<tr>
<td>12.5 V – 13.5 V</td>
<td>IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.</td>
</tr>
<tr>
<td>13.5 V – 16.5 V</td>
<td>Recommended conditions</td>
</tr>
<tr>
<td>16.5 V – 20.0 V</td>
<td>IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk.</td>
</tr>
<tr>
<td>&gt; 20.0 V</td>
<td>Control circuit is destroyed. Absolute max. rating is 20 V.</td>
</tr>
</tbody>
</table>

Table 3. Module operation according to control supply voltage

The sequence of events in case of a low side UVLO event (IGBTs turned off and active fault output) is shown in Figure 12. Figure 13 shows the same for a high side UVLO (IGBTs turned off and no fault output).

![Figure 12. Low side UVLO timing chart](image-url)
4.3. Cross conduction prevention

The STK57FU394A-E module implement a cross conduction prevention logic at the pre-driver to avoid simultaneous drive of the low- and high-side IGBTs as shown in Figure 14.

In case of both high and low side drive inputs are active (high) the logic prevents both gates from being driven – a corresponding timing diagram can be found in Figure 15 below.
Even so cross conduction on the IGBTs due to incorrect external driving signals is prevented by the circuitry the driving signals (HIN and LIN) need to include a “dead time”. This period where both inputs are inactive between either one becoming active is required due to the internal delays within the IGBTs.

Figure 16 shows the delay from the HIN-input via the internal HVG to high side IGBT, the similar path for the low side and the resulting minimum dead time which is equal to the potential shoot through period:
5. PCB design and mounting guidelines

This chapter provides guidelines for an optimized design and PCB layout as well as module mounting recommendations to appropriately handle and assemble the IPM.

5.1. Application (schematic) design

The following figure 17 gives an overview of the external circuitry’s functionality when designing with the STK57FU394A-E module.

5.2. Pin by pin design and usage notes

This section provides pin by pin PCB layout recommendations and usage notes. For a complete list of module pins refer to the datasheet or Chapter 6.

VCC

These pins are connected with the main DC power supply. The applied voltage is up to the Vcc level. Overvoltage on these pins could be generated by voltage spikes during switching at the floating inductance of the wiring. To avoid this behavior the wire traces need to be as short as possible to reduce the floating inductance. In addition a snubber capacitor needs to be placed as close as possible to these pins to stabilize the voltage and absorb voltage surges.

UN, VN, WN

100Ω

100nF/25V

100μF/25V

Vz < 18V

Figure 17. Application circuit
-VCC  This pin is connected with the emitters of IGBTs for PFC.

PFC  This is the Rectified AC Voltage input pin.

U, V, W  These are the output pins for connecting the 3-phase motor. They share the same GND potential with each of the high side control power supplies. Therefore they are also used to connect the GND of the bootstrap capacitors. These bootstrap capacitors should be placed as close to the module as possible.

VDD, VSS  These pins connect with the circuitry of the internal protection and pre-drivers for the low-side power elements and also with the control power supply of the logic circuitry. Voltage to input these terminals is monitored by the under voltage protection circuit. The VSS terminal is the reference voltage for the control inputs signals.

VB1, VB2, VB3  The VBx pins are internally connected to the positive supply of the high-side drivers. The supply needs to be floating and electrically isolated. The boot-strap circuit shown in Figure 18 forms this power supply individually for every phase. Due to integrated boot resistor and diode (RB & DB) only an external boot capacitor (CB) is required.

CB is charged when the following two conditions are met.

1. Low-side signal is input
2. Motor terminal voltage is low level

The capacitor is discharged while the high-side driver is activated.

Thus CB needs to be selected taking the maximum on time of the high side and the switching frequency into account.

![Diagram](image.png)

*Figure 18. Boot Strap Circuit*

The voltages on the high side drivers are individually monitored by the under voltage protection circuit. In case an UVP event is detected on a phase its operation is stopped.

Typically a CB value of less or equal 47μF (±20%) is used. In case the CB value needs to be higher, an external resistor (of apx. 20Ω or less) should be used in series with the capacitor to avoid high currents which can cause malfunction of the IPM.
HIN1, LIN1
HIN2, LIN2
HIN3, LIN3
PFCIN

These pins are the control inputs for the power stages. The inputs on HIN1/HIN2/HIN3 control the high-side transistors of U/V/W, the inputs on LIN1/LIN2/LIN3 control the low-side transistors of U/V/W, and the input on PFCIN controls the transistors of PFC respectively. The input are active high and the input thresholds VIH and VIL are 5V compatible to allow direct control with a microcontroller system.

Simultaneous activation of both low and high side is prevented internally to avoid shoot through at the power stage. However, due to IGBT switching delays the control signals must include a dead-time.

The equivalent input stage circuit is shown in Figure 19.

![Figure 19. Internal Input Circuit](image)

For fail safe operation the control inputs are internally tied to VSS via a 33kΩ (typ) resistor. To avoid switching captured by external wiring to influence the module behavior an additional external low-ohmic pull-down resistor with a value of 2.2kΩ-3.3kΩ should be used.

The output might not respond when the width of the input pulse is less than 1µs (both ON and OFF).

FLTEN

This pin serves both as an enable input and an active low fault output (open-drain). It is used to indicate an internal fault condition of the module and also can be used to disable the module operation. The pre-driver operates when the voltage of this pin is at 2.5V or more, and stops at 0.8V or less. The I/O structure is shown in Figure 20.

The internal sink current IoSD during an active fault is nominal 2mA @ 0.1V. Depending on the interface supply voltage the external pull-up resistor (RP) needs to be selected as shown below.

For the commonly used supplies VP:

\[
\begin{align*}
VP = 15V & \rightarrow RP \geq 20k\Omega \\
VP = 5V & \rightarrow RP \geq 6.8k\Omega
\end{align*}
\]

![Figure 20. FLTEN Connection](image)
For a detailed description of the fault operation refer to Chapter 4.

Note: The Fault signal does not permanently continue to latch. After the protection event ended and the fault clear time(min. 1ms) passed, the module's operation is automatically re-started. Therefore the input needs to be driven low externally as soon as a fault is detected.

**ITRIP**

These pins are used to enable an OCP function. The ITRIP is for inverter part, the PFCTRIP is for PFC part. When the voltage of these pins exceeds a reference voltage, the OCP function operates. For details of the OCP operation refer to Chapter 4.

**TH**

An internal thermistor to sense the substrate temperature is connected between TH and VSS. By connecting an external pull-up resistor to arbitrary voltage and measuring the midpoint voltage, the module temperature can be monitored. Please refer to heading 3.2 for details of the thermistor.

Note: This is the only means to monitor the substrate temperature indirectly.

5.3. **Heat sink mounting and torque**

If a heat sink is used, insufficiently secure or inappropriate mounting can lead to a failure of the heat sink to dissipate heat adequately. This can lead to an inability of the device to provide its inherent performance, a serious reduction in reliability, or even destruction, burst and burn of the device due to overheating.

The following general points should be observed when mounting IPM on a heat sink:

1. Verify the following points related to the heat sink:
   - There must be no burrs on aluminum or copper heat sinks.
   - Screw holes must be countersunk.
   - There must be no unevenness in the heat sink surface that contacts IPM.
   - There must be no contamination on the heat sink surface that contacts IPM.

2. Highly thermal conductive silicone grease needs to be applied to the whole back (aluminum substrate side) uniformly, and mount IPM on a heat sink. Upon re-mounting apply silicone grease(100um to 200um) again uniformly.

3. For an intimate contact between the IPM and the heat sink, the mounting screws should be tightened gradually and sequentially while a left/right balance in pressure is maintained. Either a bind head screw or a truss head screw is recommended. Please do not use tapping screw. We recommend using a flat washer in order to prevent slack. The standard heat sink mounting condition of an STK57FU394A-E is as follows.
Table 4. heat sink mounting

<table>
<thead>
<tr>
<th>Item</th>
<th>Recommended Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch</td>
<td>56.0 ± 0.1mm (Please refer to package outline diagram)</td>
</tr>
<tr>
<td>Screw</td>
<td>diameter : M3&lt;br&gt; Bind machine screw, Truss machine screw, Pan machine screw</td>
</tr>
<tr>
<td>Washer</td>
<td>Plane washer&lt;br&gt; The size is D:7mm, d:3.2mm and t:0.5mm (Fig.22) JIS B 1256</td>
</tr>
<tr>
<td>Heat sink</td>
<td>Material : Copper or Aluminum&lt;br&gt; Warpage (the surface that contacts IPM) : -50 ~ 100 μm&lt;br&gt; Screw holes must be countersunk.&lt;br&gt; No contamination on the heat sink surface that contacts IPM.</td>
</tr>
<tr>
<td>Torque</td>
<td>Final tightening : 0.6 ~ 0.9Nm&lt;br&gt; Temporary tightening : 20 ~ 30 % of final tightening</td>
</tr>
<tr>
<td>Grease</td>
<td>Silicone grease&lt;br&gt; Thickness : 100 ~ 200 μm&lt;br&gt; Uniformly apply silicone grease to whole back. (Fig.23)</td>
</tr>
</tbody>
</table>

Figure 21. Mount IPM on a heat sink

Figure 22. Size of washer

Figure 23. About uniformly application

Steps to mount an IPM on a heat sink
1st: Temporarily tighten maintaining a left/right balance.
2nd: Finally tighten maintaining a left/right balance.
5.4. Mounting and PCB considerations

In designs in which the printed circuit board and the heat sink are mounted to the chassis independently, use a mechanical design which avoids a gap between IPM and the heat sink, or which avoids stress to the lead frame of IPM by an assembly that a moving IPM is forcibly fixed to the heat sink with a screw.

![Figure 24. Fix to Heat Sink](image)

Maintain a separation distance of at least 1.5 mm between the IPM case and the printed circuit board. In particular, avoid mounting techniques in which the IPM substrate or case directly contacts the printed circuit board.

Do not mount IPM with a tilted orientation. This can result in stress being applied to the lead frame and IPM substrate could short out tracks on the printed circuit board. Always mount the IPM vertically. If stress is given by compulsory correction of a lead frame after the mounting, a lead frame may drop out. Be careful of this point.

![Image showing correct and incorrect mounting](image)

When designing the PCB layout take care that the bent part portion of the lead frame pins does not short-circuit to VIA holes or tracks on the PCB.
Since the use of sockets to mount IPM can result in poor contact with IPM leads, we strongly recommend making direct connections to PCB.

IPMs are flame retardant. However, under certain conditions, it may burn, and poisonous gas may be generated or it may explode. Therefore, the mounting structure of the IPM should also be flame retardant.

Mounting on a Printed Circuit Board

1. Align the lead frame with the holes in the printed circuit board and do not use excessive force when inserting the pins into the printed circuit board. To avoid bending the lead frames, do not try to force pins into the printed circuit board unreasonably.
2. Do not insert IPM into printed circuit board with an incorrect orientation, i.e. be sure to prevent reverse insertion. IPM may be destroyed, exploded, burned or suffer a reduction in their operating lifetime by this mistake.
3. Do not bend the lead frame.

5.5. Cleaning

IPM has a structure that is unable to withstand cleaning. As a basic policy, do not clean independent IPM or printed circuit boards on which an IPM is mounted.
6. Package Outline

The package of STK57FU394A-E is SIP2A. (Single-inline-package)

6.1. Package outline and dimension

![Package Outline Diagram]

- **note1:** No.1 pin identification mark
- **note2:** Model number
- **note3:** Lot code

* The form of a character in this drawing differs from that of IPM.

<table>
<thead>
<tr>
<th>No.</th>
<th>Part Name</th>
<th>Material</th>
<th>Treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Case</td>
<td>Epoxy</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>Substrate</td>
<td>IMST substrate</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>Lead Frame</td>
<td>Cu</td>
<td>Sn</td>
</tr>
</tbody>
</table>

*Figure 25. Package Outline*
### 6.2. Pin Out Description

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PFC</td>
<td>Rectified AC Voltage Input</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>4</td>
<td>VB3</td>
<td>High Side Floating Supply Voltage 3</td>
</tr>
<tr>
<td>5</td>
<td>W,VS3</td>
<td>Output 3 - High Side Floating Supply Offset Voltage</td>
</tr>
<tr>
<td>6</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>7</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>8</td>
<td>VB2</td>
<td>High Side Floating Supply Voltage 2</td>
</tr>
<tr>
<td>9</td>
<td>V,VS2</td>
<td>Output 2 - High Side Floating Supply Offset Voltage</td>
</tr>
<tr>
<td>10</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>11</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>12</td>
<td>VB1</td>
<td>High Side Floating Supply Voltage 1</td>
</tr>
<tr>
<td>13</td>
<td>U,VS1</td>
<td>Output 1 - High Side Floating Supply Offset Voltage</td>
</tr>
<tr>
<td>14</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>15</td>
<td>-</td>
<td>none</td>
</tr>
<tr>
<td>16</td>
<td>VCC</td>
<td>Positive PFC Output Voltage / Positive Bus Input Voltage</td>
</tr>
<tr>
<td>17</td>
<td>-</td>
<td>None</td>
</tr>
<tr>
<td>18</td>
<td>-</td>
<td>None</td>
</tr>
<tr>
<td>19</td>
<td>-VCC</td>
<td>Negative PFC Output Voltage</td>
</tr>
<tr>
<td>20</td>
<td>WN</td>
<td>Low Side Emitter Connection - Phase W</td>
</tr>
<tr>
<td>21</td>
<td>VN</td>
<td>Low Side Emitter Connection - Phase V</td>
</tr>
<tr>
<td>22</td>
<td>UN</td>
<td>Low Side Emitter Connection - Phase U</td>
</tr>
<tr>
<td>23</td>
<td>HIN1</td>
<td>Logic Input High Side Gate Driver - Phase U</td>
</tr>
<tr>
<td>24</td>
<td>HIN2</td>
<td>Logic Input High Side Gate Driver - Phase V</td>
</tr>
<tr>
<td>25</td>
<td>HIN3</td>
<td>Logic Input High Side Gate Driver - Phase W</td>
</tr>
<tr>
<td>26</td>
<td>LIN1</td>
<td>Logic Input Low Side Gate Driver - Phase U</td>
</tr>
<tr>
<td>27</td>
<td>LIN2</td>
<td>Logic Input Low Side Gate Driver - Phase V</td>
</tr>
<tr>
<td>28</td>
<td>LIN3</td>
<td>Logic Input Low Side Gate Driver - Phase W</td>
</tr>
<tr>
<td>29</td>
<td>PFCIN</td>
<td>Logic Input PFC Gate Driver</td>
</tr>
<tr>
<td>30</td>
<td>FLTEN</td>
<td>Enable input / Fault output</td>
</tr>
<tr>
<td>31</td>
<td>PFCTRIP</td>
<td>Current protection pin for PFC</td>
</tr>
<tr>
<td>32</td>
<td>ITRIP</td>
<td>Current protection pin for inverter</td>
</tr>
<tr>
<td>33</td>
<td>TH</td>
<td>Thermistor output</td>
</tr>
<tr>
<td>34</td>
<td>VDD</td>
<td>+15V Main Power Supply</td>
</tr>
<tr>
<td>35</td>
<td>VSS</td>
<td>Negative Main Power Supply</td>
</tr>
</tbody>
</table>
7. Demo Board

The demo board consists of the minimum required components such as snubber capacitor and bootstrap circuit elements of STK57FU394A-E.

Figure 26. Evaluation board schematic

Top view

Bottom view

Figure 27. Appearance photo

Length : 121mm
Side : 200mm
Thickness : 1.6mm

Rigid double-sided substrate
Material : FR-4
Copper foil thickness : 70μm
Both sides resist coating
**Figure 28. PCB layout (Top view)**

* IC1, DB1, R11-24, C14-20 are arranged on backside.

**Figure 29. Transparent view from top side**

- **U, V, W**: 3 phase inverter output
- **VDD**: Control power supply (DC15V)
- **VSS**: Signal GND
- **PFC**: Rectified AC Voltage input
- **HIX, LINx, PFCIN**: Control signal input
- **ITRIP**: Over current protection for Inverter
- **PFCTRIP**: Over current protection for PFC
- **VEXT**: FLTEN, TH pull-up
  - Impress DC5V
- **FLTEN**: Enable input and Fault output
- **TH**: Internal termistor
- **ACIN1, ACIN2**: Bridge diode AC voltage input
  - +, -: Bridge diode output
- **R1-6**: Shunt resistor, 3 parallel connection
- **R8 (, C12)**: RC filter for ITRIP
- **R7 (, C13)**: RC filter for PFCTRIP
- **R9**: Pull-up to VEXT (TH)
- **R10**: Pull-up to VEXT (FLTEN)
- **R11-17, C14-20**: Low pass filter for signal input
  - Prevention malfunction by noise
- **C4-6**: Boot strap capacitor
- **R18-24**: Pull-down to VSS for signal input
  - Prevention malfunction by external wiring
- **IC1**: IPM
- **DB1**: Bridge diode
Figure 30. Connection Example

Operation procedure

**Step1:** Please connect IPM, each power supply, logic parts, inductor and the motor to the evaluation board, and confirm that each power supply is OFF at this time.

**Step2:** Please impress DC15V to VDD and DC5V to VEXT.

**Step3:** Please perform a voltage setup according to specifications, and impress AC power supply between ACIN1 and ACIN2.

**Step4:** By inputting signal to the logic part, IPM control is started.

(Therefore, please set electric charge to the boot-strap capacitor of high side to turn on low side IGBT before running.)

Note: When turning off the power supply part and the logic part, please carry out in the reverse order to above steps.