# AND9289/D

# KNX Family: Guidelines for Porting NCN5120 to NCN5110/21/30 Transceivers ICs

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APPLICATION NOTE

### Introduction

NCN5120 and NCN5110/5121/5130 are receivers−transmitters ICs suitable for use in KNX twisted pair networks (KNX TP1−256). They support the connection of actuators, sensors, microcontrollers, switches or other applications in a building network.

NCN51xx ICs handle the transmission and reception of data on the bus. They generate their own power supplies, as well as power for external devices, from the unregulated bus voltage.

The goal of this Application Note is to present the main differences between the KNX family members and how to shift a design between the different ICs depending on design's needs and usages.

The first part of this application note will highlight the differences between all those ICs. Then the 2nd part of the application note will help a designer to identify the schematics/BoM change required to move from one part to another.

### NCN51xx Family ICs Features

Latest platform new IC family is composed of 3 products: NCN5110, NCN5121 and NCN5130.

NCN5110 is an analog only IC, in charge of the physical transmission over the KNX twisted pair network. It acts as a bit transceiver. The MAC layer being pushed to the micro−controller connected to the NCN5110.

NCN5121 is a pin−to−pin part replacement of NCN5120 with the same set of improved features.

NCN5130 is a full feature device for new design.

For more information please refer to the datasheets of the components available on ON Semiconductor website.

| | NCN5120 | NCN5121 | NCN5110 | NCN5130 |
|---|---|---|---|---|
| **Efficiency Increase** | | ✓ | ✓ | ✓ |
| **10/20 mA Bus Current Consumption** | ✓ | ✓ | | |
| **5 to 40 mA Bus Current Consumption** | | | ✓ | ✓ |
| **KNX Bus Current Limit** | | ✓ | ✓ | ✓ |
| **PHY + MAC Layer (TPUART function)** | ✓ | ✓ | | ✓ |
| **PHY Layer (analog only)** | | | ✓ | |
| **3.3 V Fixed DC/DC** | ✓ | ✓ | ✓ | ✓ |
| **Variable DC/DC** | ✓ | ✓ | ✓ | ✓ |
| **20 V LDO** | ✓ | ✓ | ✓ | ✓ |
| **Analog Monitor Output** | | ✓ | | ✓ |
| **Extended Temperature Range** | | ✓ | ✓ | ✓ |

## BLOCK DIAGRAM COMPARISON

Main changes between NCN5120 & NCN5110/21/30 are:

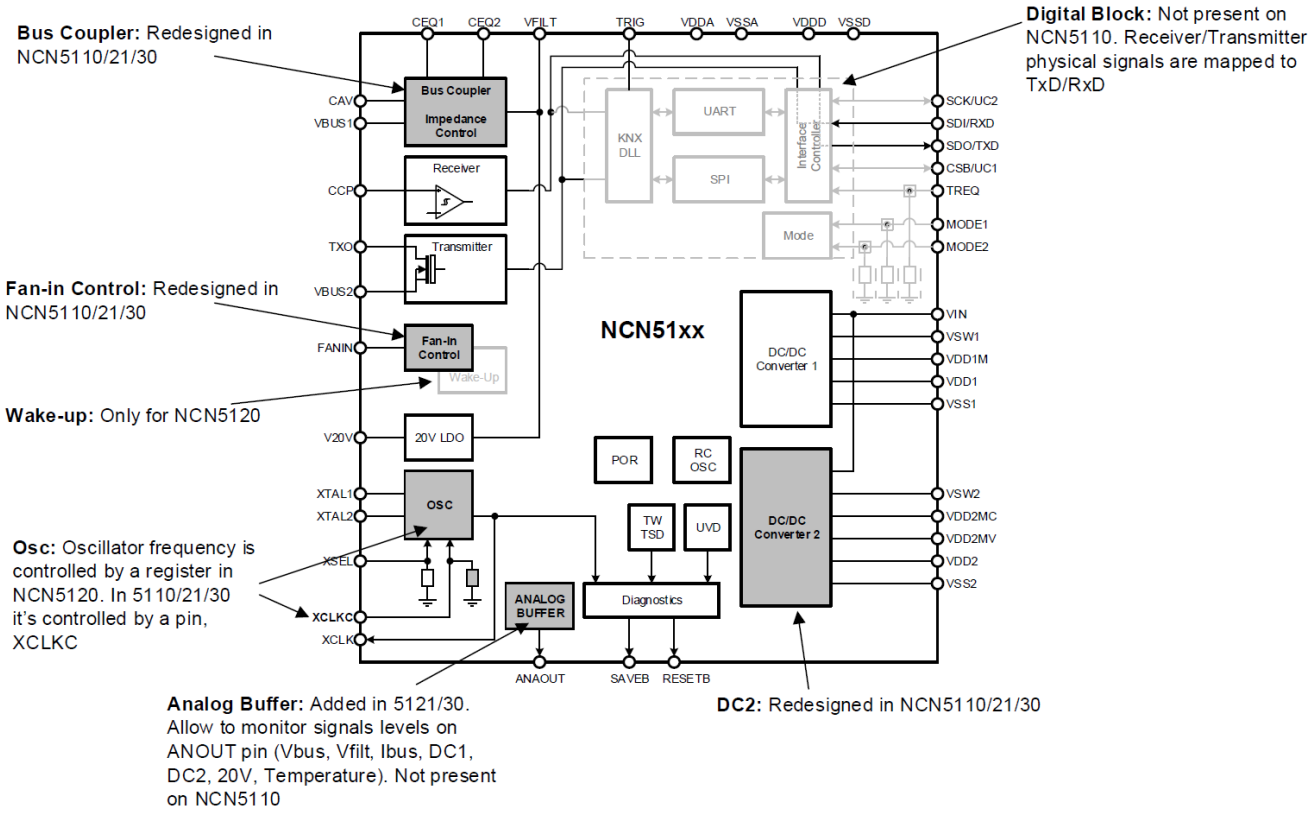


**Figure 1. NCN 51xx Block Diagram**

### Oscillator

Oscillator block has been modified. Oscillator frequency (8/16 MHz) was previously controlled by a register for NCN5120. Now on NCN5110/21/30 it is controlled by a pin, XCLKC (pin 21), that was not connected in NCN5120. If XCLKC is connected to ground (or not connected) then an 8 MHz clock signal is present on XCLK. If XCLKC is connected to Vdd then a 16 MHz clock signal is present on XCLK.

### Configuration

NCN5120/21/30 can be configured by registers that can be accessed through UART or SPI interface.

Registers allow to:

- Enable/disable DC2, 20 V LDO, Clock output
- Set the signal to be monitored on ANAOUT pin
- Configure/Set watchdog
- ...

On NCN5110:

- Enable/Disable of DC2 is driven by pin 29 (nDC2EN−pin)
- Enable/Disable of 20 V LDO is driven by pin 26 (nV20Ven)

**Table 1. MAIN FEATURES LIST COMPARISON**

| | NCN5120 | NCN5121 | NCN5110 | NCN5130 |
|---|---|---|---|---|
| **Main Application** | | Part replacement for NCN5120 (recommended for new design) | Analog only mode (Bit Transceiver) | Full feature |
| **Bus Coupler Current Consumption** | 2 discrete models: 10 or 20 mA | 2 discrete models: 10 or 20 mA | − 2 discrete models: 10 or 20 mA<br>− Analog model from 5 to 40 mA (additional resistor) | − 2 discrete models: 10 or 20 mA<br>− Analog model from 5 to 40 mA (additional resistor) |
| **Bus Coupler Current limitation** | No current limitation | Current limitation (based on bus coupler current consumption model) | Current limitation (based on bus coupler current consumption model) | Current limitation (based on bus coupler current consumption model) |
| **Bus Coupler Voltage Drop**<br>**(Bus current consumption)** | 3.5 V Typ. (at 12 mA)<br>8 V Max. (at 24 mA) | 1.75 V Typ. (at 10 mA)<br>2.8 V Max. (at 20 mA) | 1.75 V Typ. (at 10 mA)<br>4.05 V Max.(at 40 mA) | 1.75 V Typ. (at 10 mA)<br>4.05 V Max.(at 40 mA) |
| **Bus Current Consumption (50% comm. on the bus)** | 5 mA typ. | 2.7 mA typ. | 2.5 mA typ. | 2.7 mA typ. |
| **Bus Current Consumption (No comm. on the bus)** | 3.6 mA typ. | 2.5 mA typ. | 2.3 mA typ. | 2.5 mA typ. |
| **DC/DC1**<br>**DC/DC2** | 3.3 V Fixed<br>3.3−21 V Selectable | 3.3 V Fixed<br>1.2−21 V Selectable | 3.3 V Fixed<br>1.2−21 V Selectable | 3.3 V Fixed<br>1.2−21 V Selectable |
| **20V LDO output current** | 4 mA typical<br>~11 mA max | ~24 mA max<br>Current limitation configurable per register | ~37 mA max | ~48mA max<br>Current limitation configurable per register |
| **DC2/20V Enable/Disable** | Configured by register | Configured by register | Configured by signals | Configured by register |
| **Temperature range** | −25°C to +85°C | −40°C to +105°C | −40°C to +105°C | −40°C to +105°C |

## TYPICAL BOM

The table below presents the difference in the bill of material between the different parts

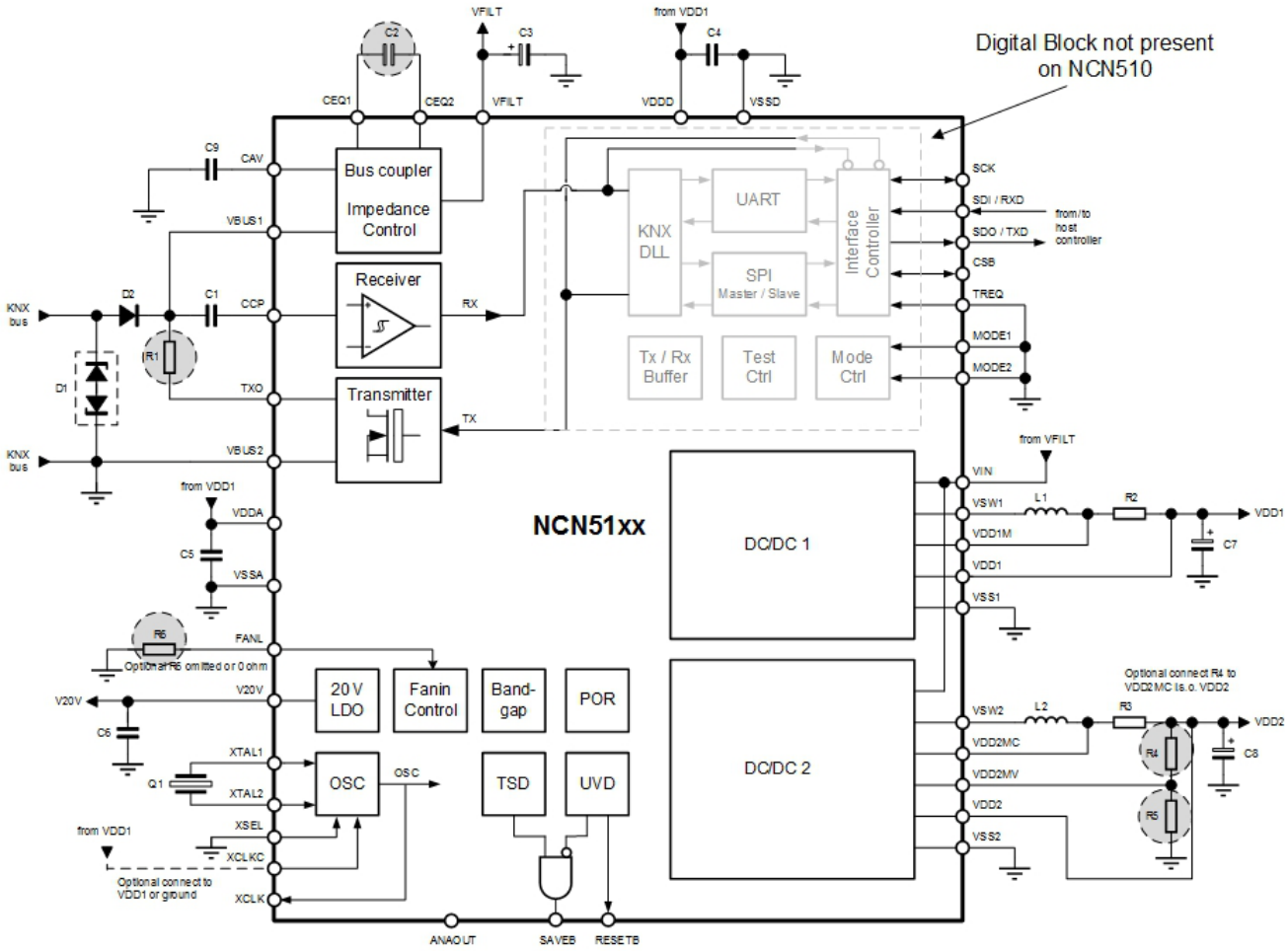


**Figure 2. NCN51xx Typical BoM**

**Table 2. TYPICAL BOM**

| | Function | NCN5120 | NCN5121 | NCN5110 | NCN5130 | Tol. | Units |
|---|---|---|---|---|---|---|---|
| C1 | AC coupling capacitor | 47 | | | | ±20% | nF |
| C2 | Energy conservation capacitor | 4.7 (±10%) | 220 (±20%) | | | | nF |
| C3 | Storage and Filter capacitor | 100 | | | | ±20% | uF |
| C4 | HF rejection capacitor at VDDD | 100 | | | | ±20% | nF |
| C5 | HF rejection capacitor at VDDA | 100 | | | | ±20% | nF |
| C6 | Load capacitor V20V | 1 | | | | ±10% | μF |
| C7 | Load capacitor VDD1 | 10 | | | | ±20 | μF |
| C8 | Load capacitor VDD2 | 10 | | | | ±20 | μF |
| C9 | Bus current slope capacitor | 100 | | | | ±20% | nF |
| R1 | Shunt resistor for transmitting | 22 | 27 | | | ±10% | Ω |
| R2 | DC1 sensing resistor | 1 | | | | ±5% | Ω |
| R3 | DC2 sensing resistor | 1 | | | | ±5% | Ω |
| R4/R5 | DC2 voltage divider | Calculation (Note 2) | | | | | |
| R6 | Fan−in resistor | N/A (Note 3) | | 10 – 93.1 (Note 3) | | ±1% | KΩ |
| L1/L2 | DC1/DC2 Coil | 220 | | | | ±20% | μH |
| D1 | Voltage suppressor | 1SAM40CA | | | | | |
| D2 | Reverse polarity protection diode | SS16 | | | | | |
| Q1 | Crystal oscillator | 16 | | Omitted (optional) (Note 1) | 16 | 50 | ppm |

1. Optional. Can be mounted if NCN5110 is used as to output a clock signal.
2. One formula for NCN5120. Formula is the same for NCN5110/NCN5121/NCN5130.
3. Only discrete mode for 5120/21 (connected to ground or not connected). Discrete or analog mode for 5110/30. Refer to Figures 3 and 4.

## Bus Current Consumption & Limitation

At startup the bus current consumption profile, Ibus, is as follow:

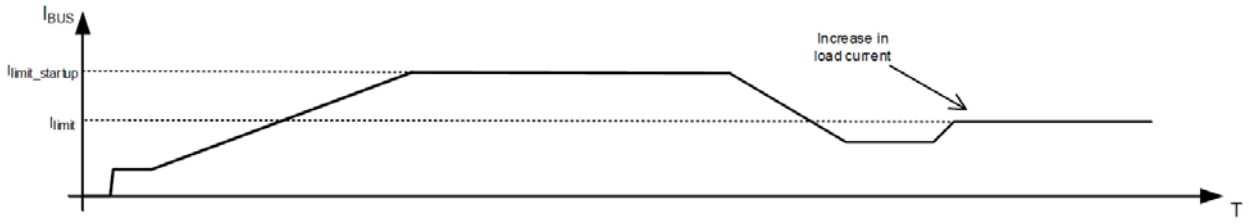


**Figure 3. Ibus Profile**

With $I_{limit}$ and $I_{limit\_startup}$ defined as:

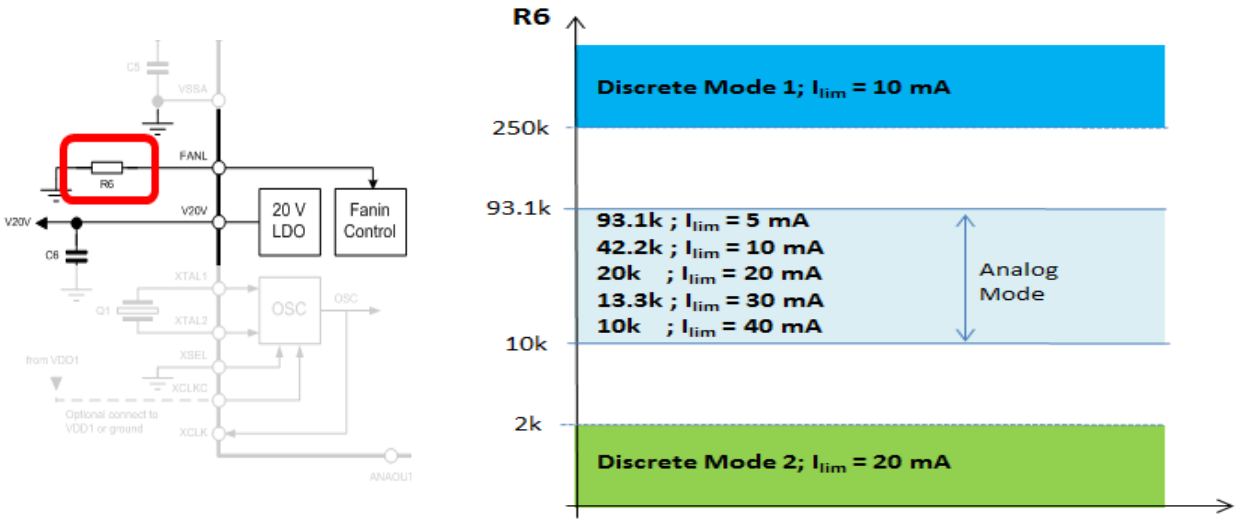


**Figure 4. $I_{lim}$ Value**

With $I_{limit\_startup}$ being approximately 2 times $I_{limit}$:
Ilimit_startup = 2 x Ilimit
In discrete mode mode the FANL pin should either be strapped to ground or kept floating.

## MOVING FROM NCN5120 TO NCN5110/21/30

### From NCN5120 to NCN5121

NCN5121 can then be used as a part replacement for NCN5120. While strictly the same PCB layout can be used when migrating from NCN5120 to NCN5121, few minor modifications (mainly components value) are needed to migrate and benefit all new NCN5121 features.

Designer needs to pay attention to the BOM change as per Table 2:

- Wake−up functionality is no longer supported. So if used then layout has to be updated to remove it.
- Clock signal output on XCLK−pin is now controlled by XCLKC−pin. If XCLK−pin was used to feed a clock signal to host controller then attention needs to be paid on XCLKC−pin for frequency.
- The shunt resistor for transmitting (R1) is 27 Ohm.
- The energy conservation capacitor (C2) value has been changed from 4.7 nF to 220 nF/50 V
- If DC2 is used, then attention needs to be paid to the voltage divider (R4/R5). Resistors must be changed compared to NCN5120 to maintain the same divider value.

### From NCN5120 to NCN5110

When NCN5120 is used in analog mode only (bit transceiver), NCN5110 can be used as a part replacement. While strictly the same PCB layout can be used when migrating from NCN5120 to NCN5110, few minor modifications (mainly components value) are needed to migrate and benefit all new NCN5110 features.

Designer needs to pay attention to the BOM change as per Table 2:

- Wake−up functionality is no longer supported. So if used then layout has to be updated to remove it.
- If crystal is not used to feed clock to another component (e.g. μC), through XCLK−pin, then crystal can be omitted (Not populated).
- Clock signal output on XCLK−pin is now controlled by XCLKC−pin. If XCLK−pin was used to feed a clock signal to host controller then attention needs to be paid on XCLKC−pin for frequency.
- If DC2 is used, then attention needs to be paid to the voltage divider (R4/R5). Resistors must be changed to maintain the same divider value.
- The shunt resistor for transmitting (R1) is 27 Ohm.
- The bus current consumption limitation can be set in discrete mode, as for NCN5120 if strapped to GND or floating, but also in analog mode if R6 is used.
- The energy conservation capacitor (C2) value has been changed from 4.7 nF to 220 nF/50 V
- If DC2 and/or 20VLDO are not used, pins 26 & 29 are used to disable those blocks.

### From NCN5120 to NCN5130

On new design NCN5130 can be used as a part replacement for NCN5120 to benefit the extra features brought by NCN5130 (see Table 1). The same PCB layout can be used while minor modifications on the BOM will benefit the improvements of NCN5130.

Designer needs to pay attention to the BOM change as per Table 2:

- Wake−up functionality is no longer supported. So if used then layout has to be updated to remove it.
- Clock signal output on XCLK−pin is now controlled by XCLKC−pin. If XCLK−pin was used to feed a clock signal to host controller then attention needs to be paid on XCLKC−pin for frequency.
- If DC2 is used, then attention needs to be paid to the voltage divider (R4/R5). To obtain the same divider value of resistors must be changed.
- The bus current consumption limitation can be set in discrete mode, as for NCN5120 if strapped to GND or floating, but also in analog mode if R6 is used.
- The shunt resistor for transmitting (R1) is 27 Ohm.
- The energy conservation capacitor (C2) value is 220 nF.

### New design in analog mode (bit transceiver)

When starting a new design in analog mode NCN5110 is the preferred IC. Since the design is not digital and will not decode the symbol, there is no need for an external clock source. The crystal oscillator can then be omitted.

### New design in full feature mode

If starting a new design in full feature mode, then, in order to benefit all the improvements of the new platform the layout and BOM should be modified according to Table 2.

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