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AND9217/D

Designing a NCL30086-Controlled LED Driver

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APPLICATION NOTE

Description

This paper proposes the key steps to rapidly design a NCL30086-driven flyback converter to power an LED string. The process is illustrated by a practical 10-W, universal mains application:

- Maximum Output Power: 10 W
- Input Voltage Range: 90 to 265 V rms
- Output Voltage Range: 12 to 20 V dc
- Output Current: 500 mA

Introduction

The NCL30086 is a power factor corrected flyback controller targeting isolated and non-isolated "Smart-dimmable" constant current LED drivers. An internal proprietary circuitry controls the input current in such a way that a power factor as high as 0.99 and an output current deviation below ±2% are typically obtained without the need for a secondary-side feedback. The current-mode, quasi-resonant architecture optimizes the efficiency by turning on the MOSFET when the drain-source voltage is minimal (valley). At high line, the circuit delays the MOSFET turn on until the second valley is detected to reduce the switching losses (see Figure 1). The device is specifically intended for very compact space efficient designs and supports analog and PWM dimming with a dedicated dimming input intended to control the average LED current. Valley lockout and frequency fold-back capabilities maintain high-efficiency performance in dimmed conditions. In addition, the circuit contains a suite of powerful protections to ensure a robust LED driver design without the need for extra components or overdesign. Among them, one can list:

- *Over Temperature Thermal Fold-Back:* connecting a NTC to the SD pin allows for gradual reduction of the LED current down to 50% of its nominal value when the temperature is excessive. If the current reduction does not prevent the temperature from reaching a second level, the controller stops operating (SD pin OTP).
- *Over Voltage Protection:* A Zener diode can further be used on the SD pin to provide an adjustable OVP protection (SD pin OVP).
- *Cycle-by-Cycle Peak Current Limit:* when the current sense voltage exceeds the internal threshold (V_{ILIM}), the MOSFET immediately turns off (cycle-by-cycle current limitation).
- *Winding and Output Diode Short-Circuit Protection (WOD_SCP):* an additional comparator stops the controller if the CS pin voltage exceeds (150% · V_{ILIM}) for 4 consecutive cycles. This feature can protect the converter if a winding or the output diode is shorted or simply if the transformer saturates.
- *Output Short-Circuit Protection (AUX_SCP):* If the ZCD pin voltage remains low for a 90-ms time interval, the controller stops pulsating until 4 seconds have elapsed.
- *Open LED Protection:* if the V_{CC} pin voltage exceeds the OVP threshold, the controller shuts down and waits 4 seconds before restarting switching operation.
- *Floating/Short Pin Detection:* the circuit can detect most of these situations which helps pass safety tests [1].

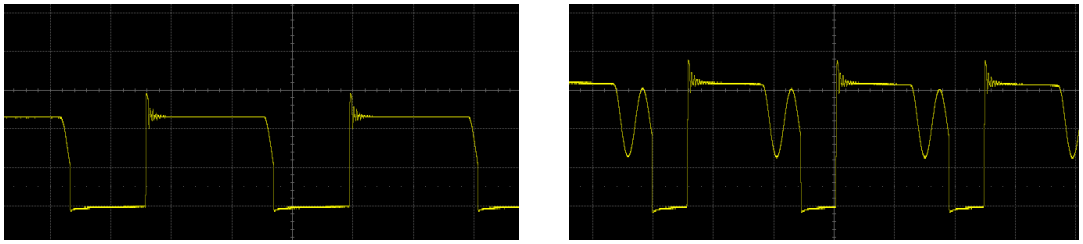

Figure 1. Quasi-Resonant Mode in Low Line (Left), Turn On at Valley 2 when in High Line (Right)

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SELECTING THE RIGHT NCL30086 VERSION

There exist four NCL30086 versions. They differ in:

- Their respective protection mode. The AUX_SCP, WOD_SCP and SD pin over-temperature (SD_OTP) and over-voltage (SD_OVP) protections are latching-off with the A and C versions and auto-recovery (the circuit resumes operation after a 4-second delay) with the B and D versions.
- The internal duty-ratio limitation. NCL30086A/B duty-ratio is internally limited to 50% at the top of the lowest line sinusoid. They are recommended if the lowest line peak voltage exceeds the inductor demagnetization voltage, i.e.,:

♦ If $\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} \geq V_{out} + V_f\right)$ with non-isolated converters,

♦ If $\left(\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} \geq \frac{n_p}{n_s}\left(V_{out} + V_f\right)\right)$ in flyback applications,

where $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (85 or 90 V rms in general) and (V_f) is the output diode forward voltage. The C and D versions that allow the duty-ratio to reach 60% at the top of the lowest line sinusoid, must be preferred otherwise.

Table 1 summarizes the differences between the four versions.

Table 1. SELECTING THE RIGHT NCL30086 VERSION

	AUX_SCP, WOD_SCP, SD_OTP, SD_OVP Protection Mode	**Output Voltage Range for Non-Isolated Converters** (Note 1)	**Output Voltage Range for Flyback Converters** (Note 1)
NCL30086A (Note 2)	Latching Off	$V_{out} + V_f \leq \sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$	$V_{out} + V_f \leq \frac{n_s}{n_p}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$
NCL30086B	Auto-Recovery	$V_{out} + V_f \leq \sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$	$V_{out} + V_f \leq \frac{n_s}{n_p}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$
NCL30086C (Note 2)	Latching Off	$V_{out} + V_f \leq \frac{3}{2}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$	$V_{out} + V_f \leq \frac{n_s}{n_p}\cdot\frac{3}{2}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$
NCL30086D	Auto-Recovery	$V_{out} + V_f \leq \frac{3}{2}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$	$V_{out} + V_f \leq \frac{n_s}{n_p}\cdot\frac{3}{2}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL}$

1. $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (e.g., 85 V rms), (V_f), the output diode forward voltage.
2. Please contact local sales representative for availability.

As an example, let's assume that we must design a 90 to 265 V rms, non-isolated buck-boost converter whose output can be as high as 150 V. Let's see if the NCL30086A or the NCL30086B can be used.

$$\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} = \sqrt{2}\cdot 90 \cong 127\ V \leq \leq V_{out} + V_f \cong 150\ V \quad \text{(eq. 1)}$$

Equation 1 indicates that Table 1 conditions of using the A and B versions are not met for non-isolated converters applications. Hence, the A/B version is not recommended while the C or D version is ok since:

$$\frac{3}{2}\cdot\sqrt{2}\cdot\left(V_{in,rms}\right)_{LL} = \frac{3}{2}\cdot\sqrt{2}\cdot 90 \cong 191\ V \geq \geq V_{out} + V_f \cong 150\ V \quad \text{(eq. 2)}$$

Generally speaking, whenever conditions of using the A and B versions are fulfilled, prefer these versions to optimally tailor the LED driver power capability to the application of interest. From this perspective, the NCL30086A and NCL30086B are typically preferred for most flyback converters* and for narrow-mains, non-isolated LED drivers. C and D versions are generally to be selected for wide-mains, non-isolated converters.

If the duty-ratio limitation is exceeded in your application, the LED current will be below its nominal value at the lowest line voltage but will meet the target when the input voltage level is sufficient. Thus, you can start with the NCL30086A or the NCL30086B and consider the NCL30086C or NCL30086D if the LED current is too low at the lowest line levels. By the way, a symptom of the duty-ratio limitation effect can be observed as shown by Figure 2 where the input current is clamped by the over-current protection during normal load conditions.

*The turns ratio of isolated flyback converters, gives some flexibility (see Table 1 conditions).

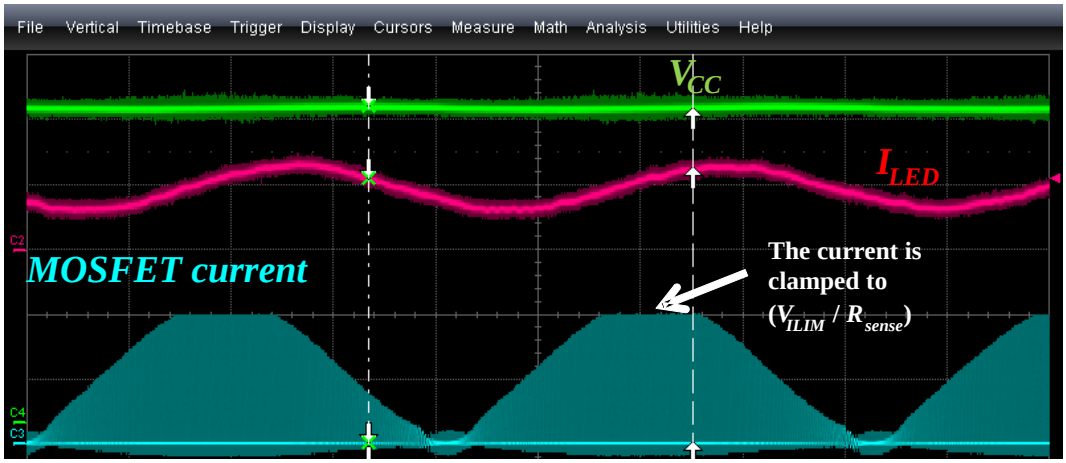


Figure 2. Current Over-Current Limitation (V_{ILIM} is the Over-Current Threshold, R_{SENSE} the Current Sense Resistor)

Our application of interest is a flyback converter. In this case, the turns ratio must be considered when selecting the appropriate version. We can see that in this specific case, the NCL30086B is the appropriate option.

LED DRIVER DIMENSIONING

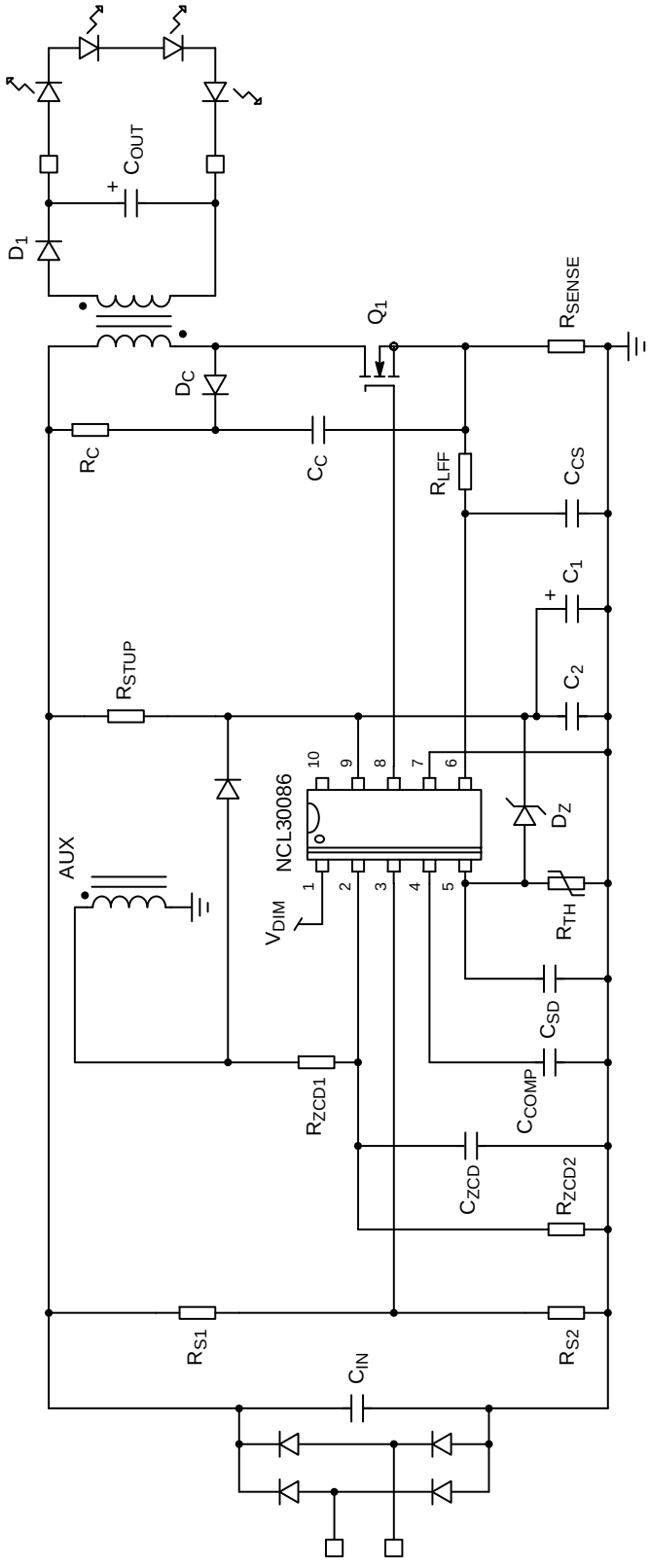


Figure 3. Basic Schematic

LED DRIVER DESIGN STEPS

AND9200 [3] details the design procedure of a LED driver controlled by the NCL30088. The same process is valid for the NCL30086 apart from a few specificities.

This application note will not re-discuss the AND9200 procedure but only provide below summary of the key design steps. Note that an online EXCEL®-based design tool is available to automate discussed computations [2]. Keep in mind however that if provided equations must help provide a good starting point, bench validation remains necessary!

SUMMARY OF KEY DESIGN STEPS

Table 2. DESIGN STEPS TABLE

Step	Components	Formula	Comments
Step 1: Power Components Selection	Transformer: Auxiliary Winding Number of Turns	$n_{AUX} \le n_s \cdot \frac{\left(V_{CC(OVP)}\right)_{min} + V_f}{V_{out(OVP)} + V_f}$	If a Zener diode is connected between the V_{CC} rail and the SD pin protection for OVP protection, $V_{CC(OVP)}$ is to be replaced by the (V_Z + 2.5). $V_{out(OVP)}$ is the output voltage when the V_{CC} or SD pin OVP trips ($V_{out(OVP)}$ can be viewed as the possible maximum value of the output voltage)
	MOSFET Turn Off Overshoot	$V_{Q-ov} = k_c \cdot \frac{n_p}{n_s} \cdot \left(V_{out} + V_f\right)$	The MOSFET turn-off overshoot due to the leakage inductor reset is expressed as a function of the reflected voltage (see Figure 4)
	MOSFET Turn Off Overshoot Coefficient	$0.5 \le k_c \le 1.0$	A low k_c reduces the MOSFET voltage stress but requires more losses to be dissipated in the clamping network. As a rule of thumb, take k_c between 0.5 and 1.0.
	Transformer: Secondary Winding Number of Turns	$\frac{n_p}{n_s} < \frac{\alpha V_{DSS} - \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}}{(1 + k_c) \cdot \left(V_{out(OVP)} + V_f\right)}$	V_{DSS} is the MOSFET breakdown voltage, α designates the derating factor (85% typically)
	Transformer: Primary Inductance	$L_p \ge \frac{\left(V_{in,rms}\right)^2}{2 f_{sw,T} P_{in,avg}} \cdot \left(\frac{\frac{n_p}{n_s}\left(V_{out} + V_f\right)}{\beta \cdot V_{in,pk} + \frac{n_p}{n_s}\left(V_{out} + V_f\right)} \right)^2$	If the primary inductor is selected equal to the proposed expression, the switching frequency will be below $f_{sw,T}$ when the line instantaneous voltage is between ($\beta \cdot V_{in,pk}$) and $V_{in,pk}$ where ($\beta \le 1$). For instance, one can force the full-load frequency range at the 115-V rms nominal voltage to be around 65 kHz for instance, by practically opting for (β = 50%) and ($f_{sw,T}$ = 65 kHz)
	Clamping Network Resistor Value	$R_c \le \frac{2 \cdot k_c}{N_{PS}} \cdot \left(V_{out(OVP)} + V_f\right) \cdot \frac{\frac{1+k_c}{N_{PS}} \cdot \left(V_{out(OVP)} + V_f\right) + \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}}{L_{leak} \cdot \left(\frac{V_{ILIM}}{R_{sense}}\right)^2 \cdot f_{SW,HL}}$	V_{ILIM} is the NCL30086 internal threshold for over-current limitation (1 V typically). $(V_{in,rms})_{HL}$ and $f_{sw,HL}$ are the rms input voltage and the switching frequency at the line highest level.

Table 2. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
	Clamping Network Resistor Losses	$P_{R_c} \le \frac{\left(\frac{n_p}{n_s} \cdot (1 + k_c) \cdot \left(V_{out(OVP)} + V_f\right)\right)^2}{R_C}$	$V_{out(OVP)}$ is the output voltage when the V_{CC} or SD pin OVP trips ($V_{out(OVP)}$ can be viewed as the possible maximum value of the output voltage)
	Clamping Network Capacitor	$C_C \cong \frac{1\ ms}{R_C}$	
	Maximum Primary Inductor Peak Current	$\left(I_{L,pk}\right)_{max} = 2\sqrt{2} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \left(1 + \frac{n_s \cdot \sqrt{2}\left(V_{in,rms}\right)_{LL}}{n_p \cdot \left(V_{out} + V_f\right)}\right)$	
	Maximum Primary Inductor rms Current	$\left(I_{L,rms}\right)_{max} = \frac{2 \cdot \left(P_{in,avg}\right)_{max}}{\sqrt{3} \cdot \left(V_{in,rms}\right)_{LL}} \cdot \sqrt{1 + \frac{16 \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{3\pi \cdot \frac{V_{out}+V_f}{N_{PS}}} + \frac{6\pi \cdot \left(V_{in,rms}\right)_{LL}^2}{4 \cdot \left(\frac{V_{out}+V_f}{N_{PS}}\right)^2}}$	N_{PS} is the turns ratio $N_{PS} = n_s / n_p$
	MOSFET rms Current	$\left(I_{Q,rms}\right)_{max} = \frac{2}{\sqrt{3}} \cdot \frac{\left(P_{in,avg}\right)_{max}}{\left(V_{in,rms}\right)_{LL}} \cdot \sqrt{1 + \frac{8\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{3\pi \cdot \frac{V_{out}+V_f}{N_{PS}}}}$	
	Maximum MOSFET Drain-Source Voltage	$V_{ds,max} = \sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} + \frac{(1 + k_c) \cdot \left(V_{out(OVP)} + V_f\right)}{\frac{n_s}{n_p}}$	
	Maximum Output Diode Voltage	$V_{diode,max} = \left(\frac{n_s}{n_p} \cdot \sqrt{2} \cdot \left(V_{in,rms}\right)_{max}\right) + V_{out} + V_f + V_{D-ov}$	V_{D-ov} is the output diode overshoot that occurs when the MOSFET turns on.
	Output Diode Average Current	$I_{diode,avg} = I_{out}$	
	Output Diode Rms Current	$\left(I_{D,rms}\right)_{max} = \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{n_p}{n_s}\right)^2 \cdot \frac{\left(P_{in,avg}\right)_{max}^2}{V_{in,rms} \cdot \frac{V_{out}+V_f}{N_{PS}}} \cdot \left[1 + \frac{9\pi^2}{16\sqrt{2}} \cdot \frac{V_{in,rms}}{\frac{V_{out}+V_f}{N_{PS}}}\right]}$	
	Minimum Output Capacitor Value	$C_{out,min} = \frac{\sqrt{\left[\frac{2}{\frac{\left(\Delta I_{out}\right)_{pk-pk}}{I_{out,nom}}}\right]^2 - 1}}{4\pi \cdot f_{line,min} \cdot R_{LED,min}}$	$I_{out,nom}$ is the nominal output current, $R_{LED,min}$, the minimum LED series resistor, and $(\Delta I_{out})_{pk-pk}$, the output current targeted peak-to-peak ripple.
	Output Capacitor Rms Current	$\left(I_{C,rms}\right)_{max} = \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{n_p}{n_s}\right)^2 \cdot \frac{\left(P_{in,avg}\right)_{max}^2}{V_{in,rms} \cdot \frac{V_{out}+V_f}{N_{PS}}} \cdot \left[1 + \frac{9\pi^2}{16\sqrt{2}} \cdot \frac{V_{in,rms}}{\frac{V_{out}+V_f}{N_{PS}}}\right] - I_{out,nom}^2}$	

Table 2. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
Step 2: Output Current Setting	Current Sense Resistor	$R_{sense} = \frac{n_p}{n_s} \cdot \frac{V_{REF}}{2 \cdot I_{out,nom}}$	V_{REF} is the internal reference. (V_{REF} is 250 mV with the NCL30086A and NCL30086B versions, 200 mV with the NCL30086C and NCL30086D versions)
	COMP Capacitor	1 μF or More	
	V_{SENSE} Resistors	$R_{S1} = R_{S2} \cdot \left(\frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{BOH}}{V_{BO(on)}} - 1 \right)$	$(V_{in,rms})_{BOH}$ is the minimum line rms voltage for entering operation. $V_{BO(on)}$ is the upper threshold of the internal Brown-Out comparator (1 V typically).
	Feedforward Resistor	$R_{LFF} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \cdot \frac{t_{prop} \cdot R_{sense}}{L_p \cdot K_{LFF}}$	T_{prop} is the total propagation delay between the instant when the MOSFET current reaches the setpoint and the effective MOSFET turn off. You can take 250 ns or 300 ns as a starting value. K_{FLL} is an internal ratio (20 μS typically)
	Current Sense Capacitor	Few pF	No capacitor is normally necessary. 10 to 22 pF can be placed in case of noisy signals. Please note that too large a filtering capacitor can alter the WOD_SCP triggering (the WOD_SCP protection is to face core saturation events and/or output diode or winding short circuit situations) if the CS pin signal is too softened.
Step 3: SD Pin Management	SD Pin OVP Threshold	$\left(V_{CC}\right)_{SD,OVP} = V_Z + V_{OVP}$	V_{OVP} is the SD pin OVP internal threshold (2.5 V typically)
	SD Pin Capacitor	< 4.7 nF	A filtering capacitor can be placed across the pin and ground. This capacitor must be less than 4.7 nF. If not, a false OTP detection may occur (see data sheet).
	SD Pin NTC		See Figure 5
Step 4: Auxiliary Winding and V_{CC}	V_{CC} Capacitor Minimum Value	$\left(C_{Vcc}\right)_{min} \cong \frac{n_s \cdot C_{out}}{n_{aux}} \cdot \frac{\left(I_{CC2} + Q_g \cdot f_{sw}\right)}{I_{out}} \cdot \frac{\left(V_{CC(off)}\right)_{max}}{\left(V_{CC(HYS)}\right)_{min}}$ or $\left(C_{Vcc}\right)_{min} \cong 1.175 \cdot \frac{n_s \cdot C_{out}}{n_{aux}} \cdot \frac{\left(I_{CC2} + Q_g \cdot f_{sw}\right)}{I_{out}}$	$(I_{CC2} + Q_g \cdot f_{sw})$ is an estimation of the circuit consumption (I_{CC2} is 4 mA max, Q_g is the MOSFET gate charge and f_{sw} is the switching frequency). $(((V_{CC(off)})_{max} / (V_{CC(HYS)})_{min}) = 1.175)$ is the ratio of the maximum value of the V_{CC} voltage necessary to maintain operation (9.4 V) over the minimum UVLO hysteresis (8 V).

Table 2. DESIGN STEPS TABLE (continued)

Step	Components	Formula	Comments
	Required Start-up Current	$I_{startup} = \frac{\left(V_{CC(on)}\right)_{max} \cdot C_{Vcc}}{t_{startup}} + \left(I_{CC(start)}\right)_{max}$ $I_{startup} = \frac{20 \cdot C_{Vcc}}{t_{startup}} + 30\ \mu A$	$(V_{CC(on)})_{max}$ is the maximum value of the VCC voltage necessary to enter operation (20 V), $(I_{CC(start)})_{max}$ is the maximum circuit consumption before entering operation (30 μA), $t_{startup}$ is the targeted start-up time.
	Start-up Resistor Value	Half-Wave Connection: $R_{startup1/2} = \frac{\frac{\left(V_{in,rms}\right)_{LL} \cdot \sqrt{2}}{\pi}}{I_{startup}}$ Bulk Connection: $R_{startup} = \frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{LL}}{I_{startup}}$	See Figure 6
	Start-up Resistor Losses	Half-Wave Connection: $P_{startup1/2} = \frac{\left(\frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}}{\pi} - V_{CC}\right)^2}{R_{startup1/2}} \leq \frac{2}{\pi^2} \cdot \frac{\left(V_{in,rms}\right)^2_{HL}}{R_{startup1/2}}$ Bulk Connection: $P_{startup1/2} = \frac{\left(\sqrt{2} \cdot \left(V_{in,rms}\right)_{HL} - V_{CC}\right)^2}{R_{startup}} \leq \frac{2 \cdot \left(V_{in,rms}\right)^2_{HL}}{R_{startup}}$	
	Upper ZCD Resistor	$R_{ZCD1} \geq \frac{V_{CC(OVP)_{max}} + V_f}{I_{ZCD,dmg}}$ And: $R_{ZCD1} \geq \frac{n_{aux}}{n_p} \cdot \frac{\sqrt{2} \cdot \left(V_{in,rms}\right)_{HL}}{I_{ZCD,on}}$	$I_{ZCD,dmg}$ is the maximum current that can be injected in the ZCD pin (5 mA), $I_{ZCD,on}$ is the maximum current which can be extracted from the ZCD pin (2 mA).
	Bottom ZCD Resistor	$R_{ZCD2} \leq \frac{5\ V}{V_{CC(OVP)} + V_f - 5\ V} \cdot R_{ZCD1}$	R_{ZCD2} serves to maintain the ZCD pin voltage below 5 V for optimal operation.
	ZCD Pin Capacitor	Few Tens of pF	Add the capacitor necessary for MOSFET turn on at the very valley. *Such a capacitor can further help if spikes of the ZCD signal which may lead to an improper ZCD detection occur after the ZCD blanking time. However, in this case, it is recommended to check that the MOSFET clamping network is properly damped (having for instance a resistor like R_{14} of Figure 7)*

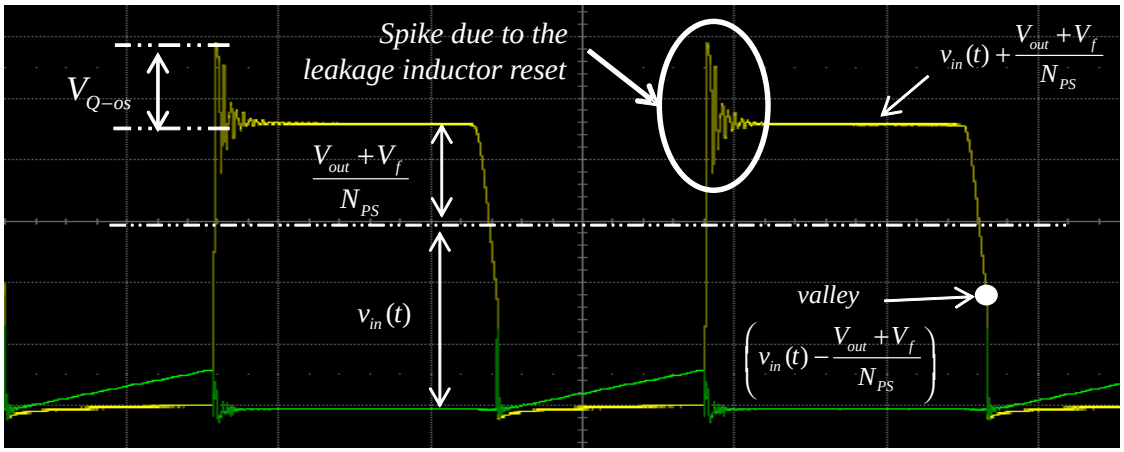


Figure 4. MOSFET Drain-Source Voltage (Yellow Trace) and Current (Green)

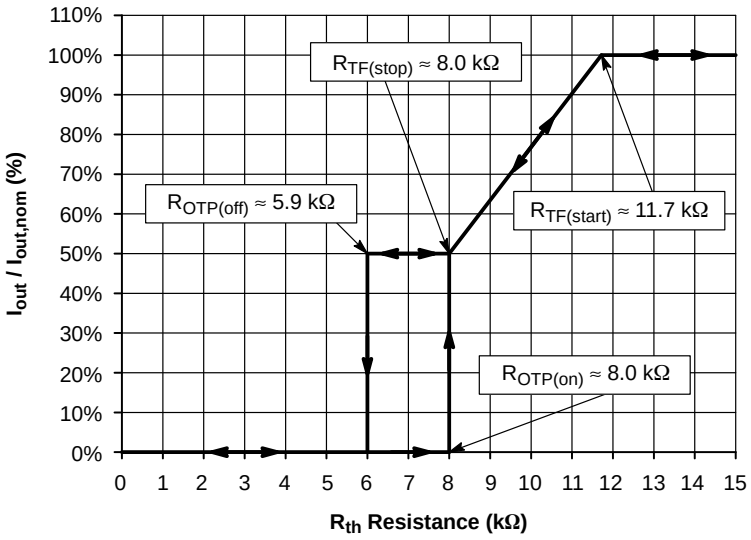


Figure 5. Thermal Foldback Characteristics and Over-Temperature Protection

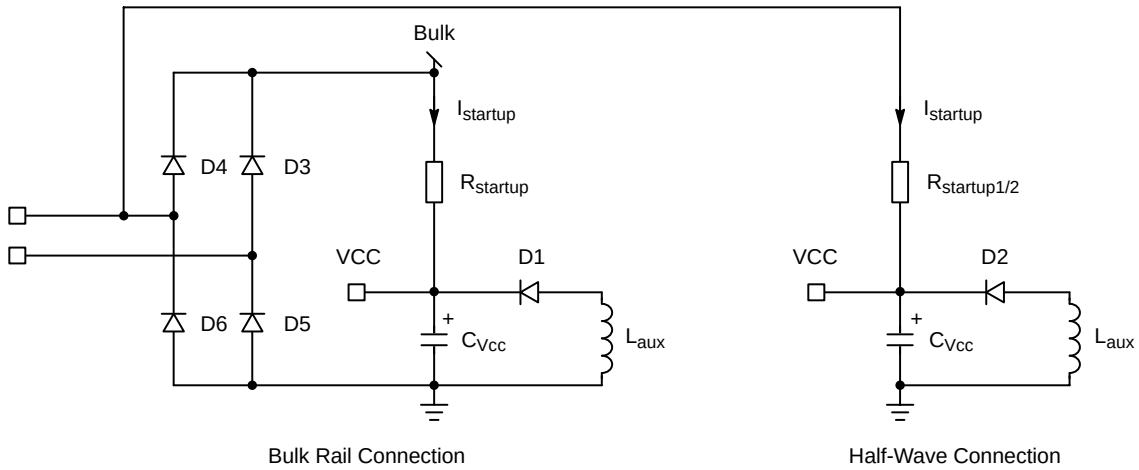


Figure 6. The Start-Up Resistor can be Connected to the Bulk Rail or to the Half-Wave

EXPERIMENTAL DATA

Application Schematic

The application of Figure 7 has been used to obtain below experimental data.

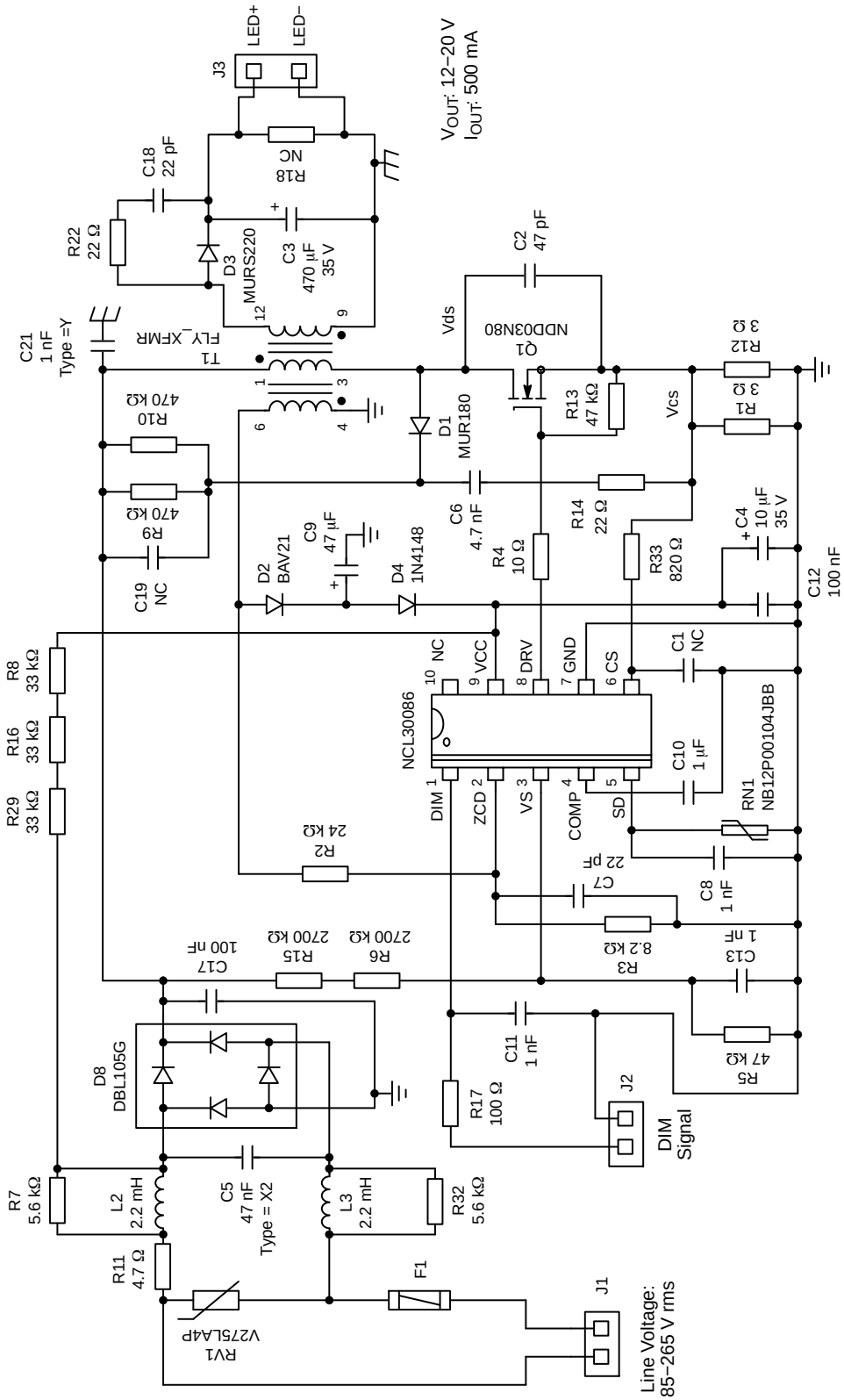


Figure 7. Application Schematic

General Operation

Figure 8 shows the output current as a percentage of its nominal value. We can see that its characteristic is very flat with respect to the temperature.

Thermal Foldback starts at about 80°C. As a result, the output current linearly decays to reach 50% of its nominal value at nearly 92°C. The circuit stops operating (SD pin Over Temperature Protection) at approximately 105°C and resumes operation when the temperature drops down to about 90°C. These temperature thresholds depend on the thermistor connected to the SD pin. Below characteristics were obtained with a NB12P00104JBB thermistor manufactured by AVX.

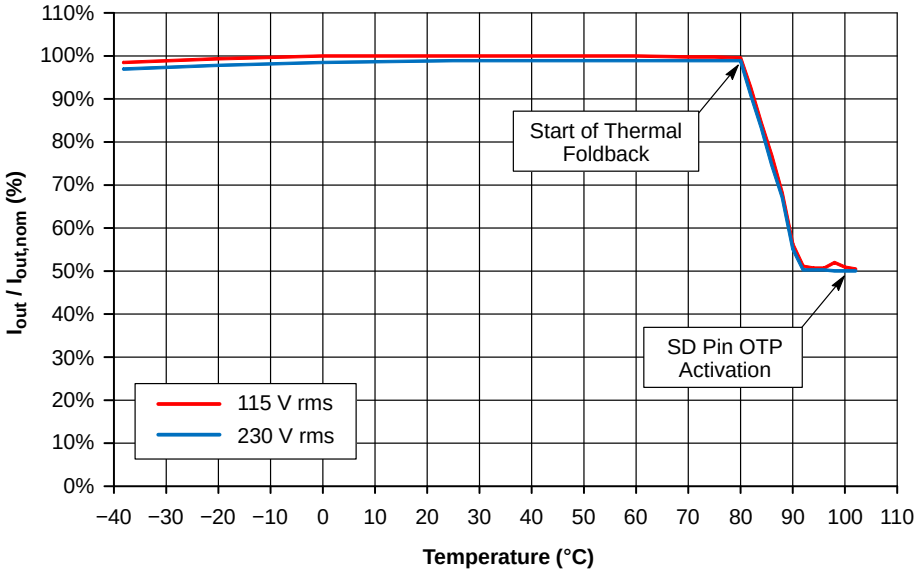


Figure 8. LED Current Characteristics over the Temperature Range without a Dimming Signal

Figure 9 shows the power factor measured at two different line magnitudes (115 V rms and 230 V rms). The power factor is extremely stable over the considered temperature range from −40°C to 80°C. Above 80°C, the performance is affected by the thermal foldback which reduces the output current.

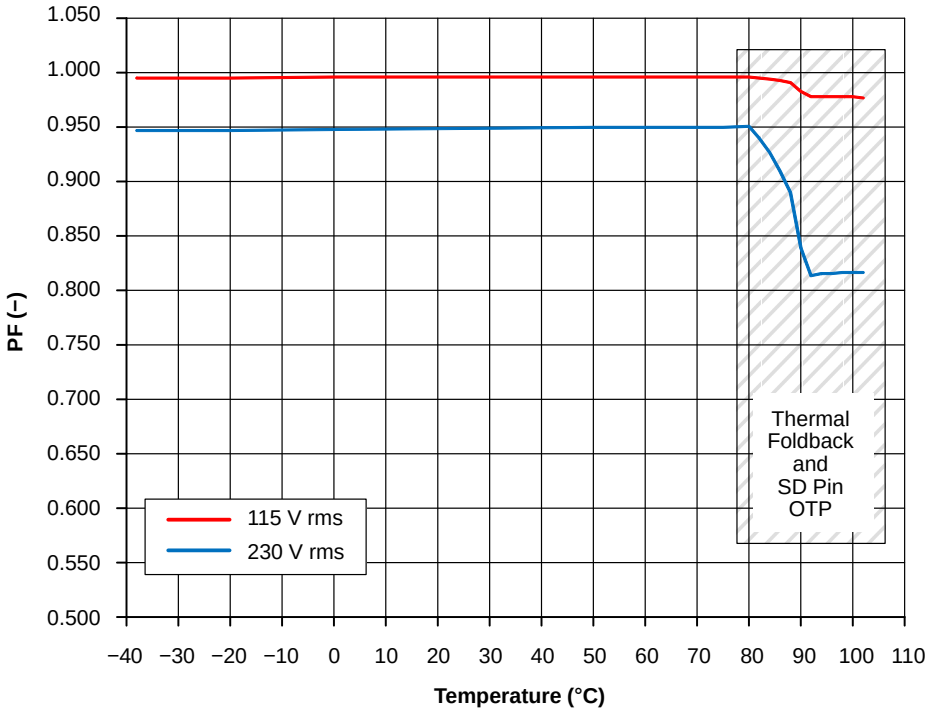
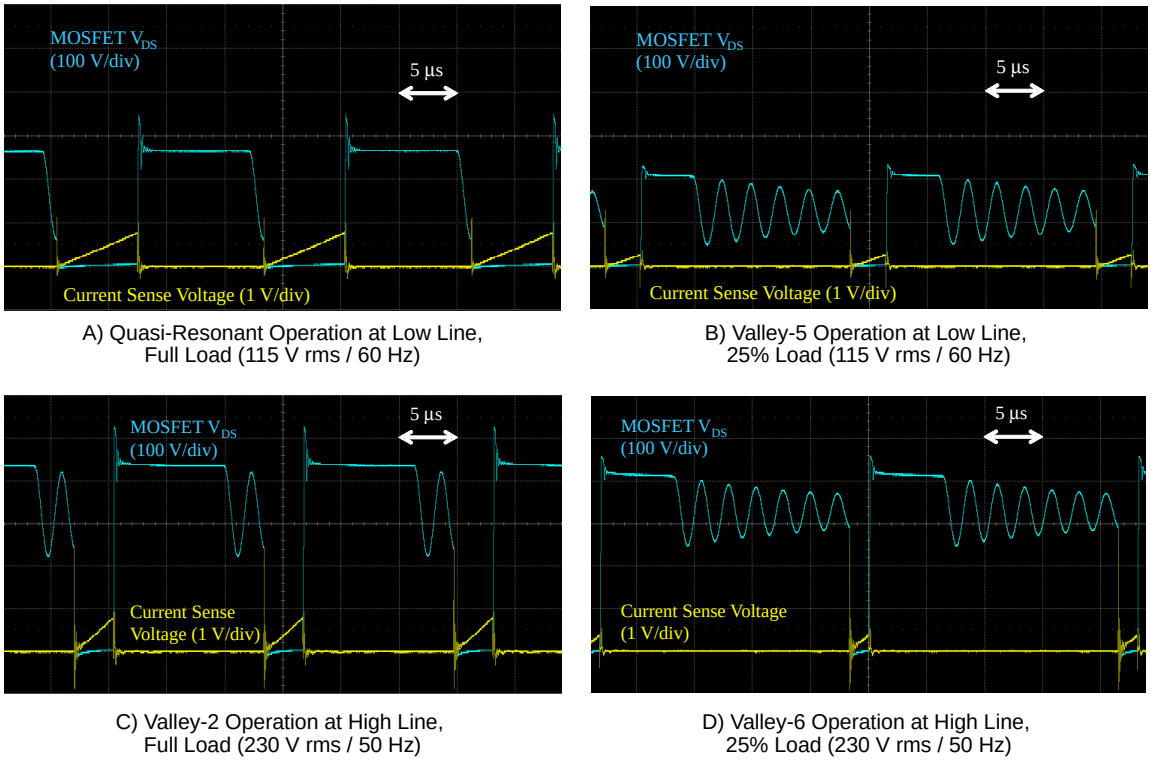


Figure 9. Power Factor Performance over the Temperature Range (No Dimming)

Valley Lockout and Frequency Foldback

The NCL30086 implements a current-mode, quasi-resonant architecture which optimizes the efficiency over a wide load range, by turning on the MOSFET when its drain-source voltage is minimal (valley). When the light is dimmed, not the first detected valley but a following one is used to initiate a new switching cycle to reduce the switching losses (see Figure 10). For stable operation, the valley at which the MOSFET closes remains locked until the light demand is changed (Valley Lockout). Practically, the NCL30086 transitions from quasi-resonant to valley-2 operation at low line and from valley-2 to valley-3 operation at high line when the LED driver load goes below 80% of its nominal value. At 25% of the nominal LED current, the circuit operates at the 5th valley (6th valley) in low-line (high-line) conditions. If the light is further dimmed, the switching frequency is further decreased by having the 5th valley (low line) or the 6th valley (high line) followed by an additional dead-time. This extra dead-time gradually increases as the line demand drops. It typically reaches 40 μs at 5% of the nominal load.



A) Quasi-Resonant Operation at Low Line, Full Load (115 V rms / 60 Hz)

B) Valley-5 Operation at Low Line, 25% Load (115 V rms / 60 Hz)

C) Valley-2 Operation at High Line, Full Load (230 V rms / 50 Hz)

D) Valley-6 Operation at High Line, 25% Load (230 V rms / 50 Hz)

Figure 10. NCL30086 Valley Lockout

It is worth noting that high-frequency operation would lead to small current levels in light-load conditions. Hence, valley lockout and frequency foldback not only optimize efficiency and reduce the power supply pollution (valley turn-on reduces noise and low-frequency operation helps pass EMI standard) but also contribute in maintaining a relatively high MOSFET peak current even at the lowest loads. This ensures a robust and accurate output current control over the dimming range.

The NCL30086 detects high-line conditions when the V_S pin voltage exceeds 2.4 V typically and remains in this state until the V_S pin voltage happens to remain below 2.3 V for 25 ms (typical values). In high-line conditions, switching losses generally are particularly critical. It is thus efficient to skip an additional valley to lower the switching frequency. At full load for instance, the NCL30086 turns on the MOSFET at the first valley in low-line conditions and at the second valley in high-line ones as shown by Figure 1. This helps operate with a strong current sense signal for a robust and accurate control even in the light load cases.

Dimming

The NCL30086 forces full LED current when the DIM pin voltage exceeds V_{DIM100} (2.5 V, typically) and interrupts the power delivery when V_{DIM} drops below V_{DIM0} (0.7 V, typically). When the DIM pin voltage is between these two levels, the output current set-point is an affine function of V_{DIM}. Finally, the output current can then be controlled by the DIM pin as follows:

$$I_{out} = 0 \quad \text{if } V_{DIM} \le V_{DIM0}$$

$$I_{out} = I_{out,nom} \quad \text{if } V_{DIM} \ge V_{DIM100} \qquad \text{(eq. 3)}$$

$$I_{out} = \frac{V_{DIM} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} \cdot I_{out,nom} \quad \text{otherwise}$$

Where $I_{out,nom}$ is the nominal output current (full-load current).

PWM Dimming

As shown by Figure 11, PWM dimming consists of applying a signal abruptly varying between an upper level higher than V_{DIM100} and a floor value below V_{DIM0} so that the output current will be:

$$I_{out} \cong I_{out,nom} \cdot d_{DIM} \qquad \text{(eq. 4)}$$

Where d_{DIM} is the duty ratio of the DIM pin signal.

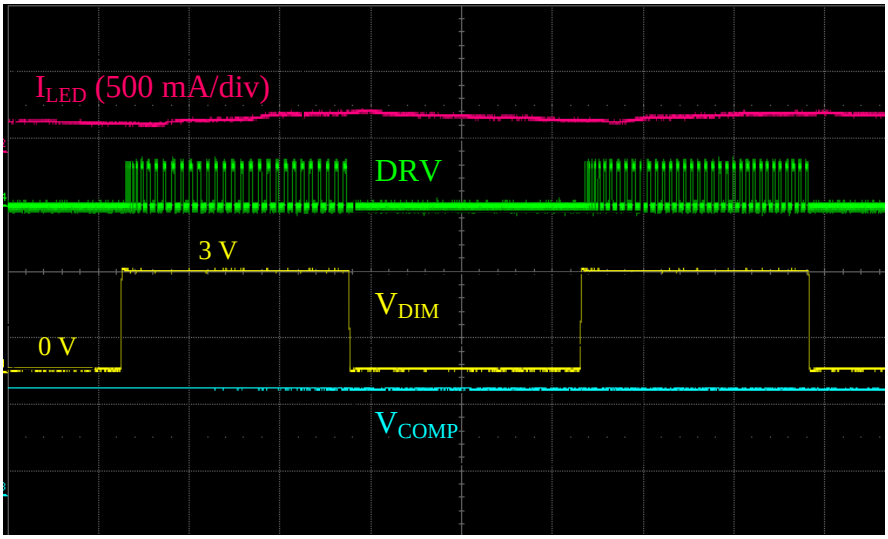


Figure 11. Pin DIM Chronograms

The NCL30086 is optimized for PWM dimming operation. In particular, the COMP pin discharge is very limited when $V_{DIM} < 0.7$ V and delays are minimized. However, there are sources of deviations which lead the output current to be a bit lower than the value suggested by Equation 4. First, if the DIM pin voltage edges are not steep enough, the output current setpoint will gradually change during the transitions instead of abruptly changing from maximum to zero and vice versa. Second, when the V_{DIM} goes above V_{DIM100}, the output current does not immediately take its nominal value:

- The NCL30086 needs some time to provide the full current. As shown by Figure 12, the first drive pulse occurs about 10 μs after the DIM pin rising edge. In addition, a short soft-start takes place. All this leads to an approximate 30-μs total delay for full power operation.
- As illustrated by Figure 13, it takes about 2.5-μs time to have the drive output disabling when the DIM pin transitions to low state. The practical effect of this delay depends on when the last drive pulse occurs compared to the DIM signal falling edge but in general, it cannot compensate for above one.

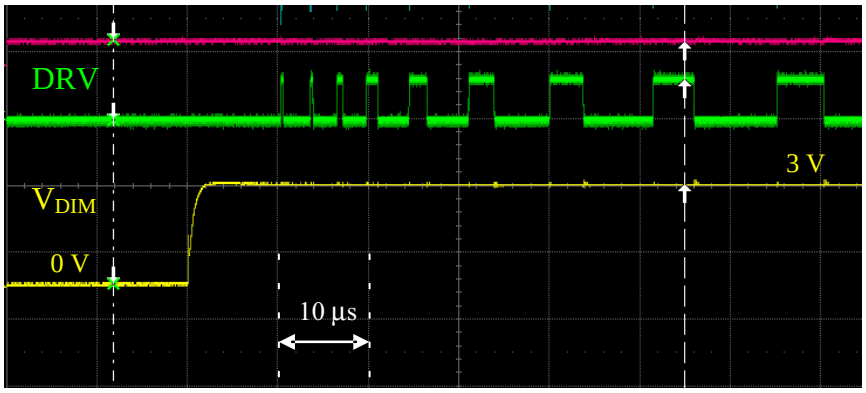


Figure 12. PWM Dimming − DIM Pin Rising Edge

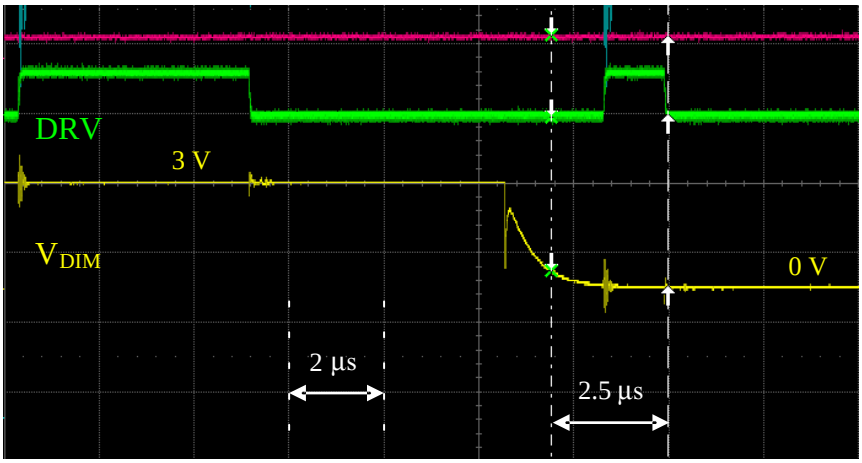


Figure 13. PWM Dimming − DIM Pin Falling Edge

The influence of these delays is particularly significant when the time for which $V_{DIM} > 2.5$ V is short, that is, when the dimming signal frequency is high and the duty ratio is small. Hence, from that perspective, the DIM signal frequency should not be selected too high particularly if operation at low duty-ratios is targeted.

Also, the chopped nature of the power transfer may affect the output current accuracy, particularly at light load, where for instance, the MOSFET clamping network capacitor (C_C of Figure 3) may have time to discharge during the off-period of time. A high frequency dimming operation may be preferred on that point of view.

Generally, since like for any power factor corrected single stage architecture there will be a component of line ripple (100/120 Hz) on the output. If PWM dimming is used, it is recommended to have the dimming frequency selected sufficiently high not to generating beat frequencies that could create optical artifacts.

>> ***As a rule of thumb, the PWM frequency should be selected between 5 and 20 times the line frequency.***

Figure 14 shows the output current as function of the PWM dimming signal duty-ratio. Tests were made at 115 V rms, 60 Hz. The dimming signal was a 1-kHz, variable duty-ratio square-wave signal varying between 0 and 3 V (yellow signal of Figure 12 and Figure 13).

The output current is displayed as a percentage of its nominal value at four different ambient temperatures. We can observe that the output current is nicely controlled by the dim pin even if as expected, the measured current is slightly below the theoretical value ($I_{out} / I_{out,nom} = d_{DIM}$) suggested by the red dotted lines of Figure 14. The relative deviation is worse at low duty ratio and reduces as the light demand increases.

As aforementioned, the thermistor applied to the SD pin (NB12P00104JBB from AVX), leads the output current to reduce when the temperature exceeds 80°C and makes it gradually decay to 50% at 95°C**. Because of this thermal foldback characteristic, the non-dimmed output current is only 60% of its nominal value at 90°C. That is why as shown by Figure 14 D), the output current varies from 0 to 60% of its nominal value at this temperature level.

** The Over Temperature Protection trips if the temperature further increases up to 105°C. In this case, the circuit stops operating until the temperature drops down to 85°C.

This illustrates that as explained in the data sheet, thermal foldback and dimming current reductions are cumulative. For instance, if the DIM pin voltage and the thermal foldback respectively, reduces the output current set-point by 50% and 20% respectively, the output current will be 50% · 80% that is 40% of its nominal level.

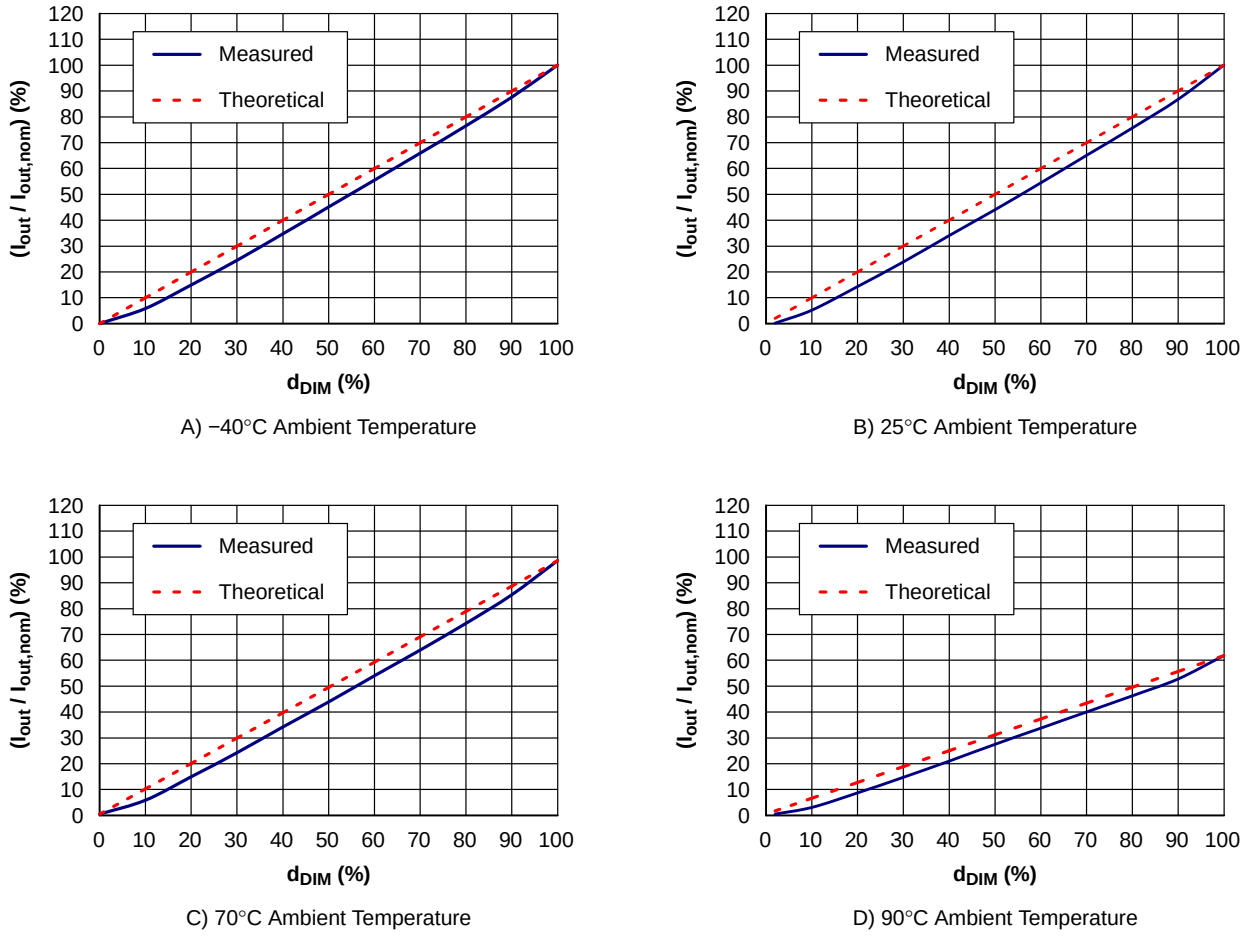


Figure 14. ($(I_{out} / I_{out,nom})$ (%)) vs. Dimming Duty-Ratio

Analogue Dimming

Figure 15 shows the output current as function of the voltage applied to the DIM pin. Tests were made at 115 V rms, 60 Hz. The output current is displayed as a percentage of its nominal value at four different ambient temperatures.

The measured characteristic (in blue) is compared to the theoretical one (red dotted curve) drawn by assuming that:

$$I_{out} = 0 \quad \text{if } V_{DIM} \le V_{DIM0}$$

$$I_{out} = I_{out,nom} \quad \text{if } V_{DIM} \ge V_{DIM100} \qquad \text{(eq. 5)}$$

$$I_{out} = \frac{V_{DIM} - V_{DIM0}}{V_{DIM100} - V_{DIM0}} \cdot I_{out,nom} \quad \text{otherwise}$$

We can observe that the output current characteristic perfectly matches the expected one: at a null when the DIM pin voltage is below 0.7 V and maximum when V_{DIM} exceeds 2.5 V, the output current is the expected nice affine function of the DIM pin voltage between these two levels.

Again, as already detailed in the PWM dimming section, a thermistor NB12P00104JBB being applied to the SD pin, the output current cannot exceed 63% at 90°C (thermal foldback protection). That is why as shown by Figure 15 D), the output current varies from 0 to 63% of its nominal value at this temperature level. The observed deviation at intermediate V_{DIM} values, is assumed to be due to a 1 or 2-degree temperature variation in the oven that may have affected the thermal foldback output current reduction during the measure.

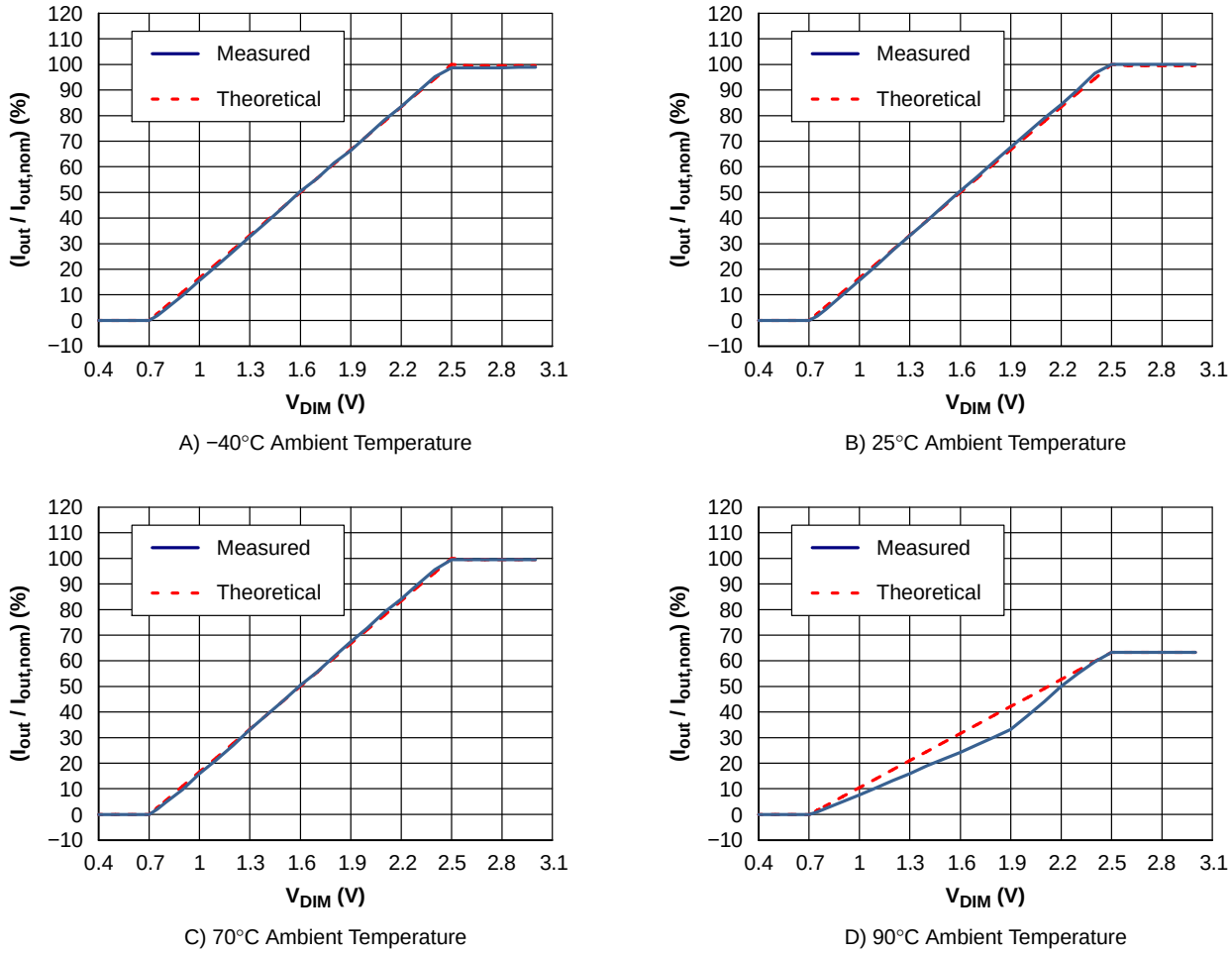


Figure 15. ($(I_{out} / I_{out,nom})$ (%)) vs. The DIM Pin Voltage

Safety Performance

The NCL30086 incorporates the same large suite of protections as the NCL30088 and in particular, the capability to face shorted/open situations of the LED string or an output diode failure. Some experimental data on the circuit under such faults can be found in [3]. In addition, [1] provides a detailed analysis of the circuit behavior under traditional safety tests (short between adjacent pins, open/grounded pin situations…). This application note demonstrates the capability of built-in safety features to dramatically help pass these tests.

REFERENCES

[1] Joel TURCHI, “NCL30088 and NCL30085 Safety Tests Consideration”, Application Note AND9204/D.
[2] Frazier PRUETT, NCL30085−6−8 Design & Development Tool, http://m.onsemi.com/support/documents?type=tools&rpn=NCL30086
[3] Joel TURCHI, “4 Key Steps to Design a NCL30088-Controlled LED Driver”, Application Note AND9200/D.

An 8-W high-PF SEPIC LED driver with a 3.3-V “always on” auxiliary voltage rail to power a MCU/wireless transceiver plus other accessories and a simple dimming and ON/OFF control that demonstrates dimming control of the NCL30086 as well as dim to off operation, is detailed in following evaluation board manual:

[4] Frazier PRUETT, “NCL30086SMRTGEVB 8-W Smart LED Driver Evaluation Board User’s Manual”, http://www.onsemi.com/pub_link/Collateral/EVBUM2293−D.PDF

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