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4 Key Steps to Design a NCL30088-Controlled LED Driver

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APPLICATION NOTE

Description

This paper proposes the key steps to rapidly design a NCL30088-driven flyback converter to power an LED string. The process is illustrated by a practical 10 W, universal mains application:

- Maximum Output Power: 10 W
- Input Voltage Range: 90 to 265 V rms
- Output Voltage Range: 12 to 20 V dc
- Output Current: 500 mA

Introduction

The NCL30088 is a driver for power-factor corrected flyback, non-isolated buck-boost and SEPIC converters. The current-mode, quasi-resonant architecture optimizes the efficiency by turning on the MOSFET when the drain-source voltage is minimal (valley). At high line, the circuit delays the MOSFET turn on until the second valley is detected to reduce the switching losses. An internal proprietary circuitry controls the input current in such a way that a power factor as high as 0.99 and an output current deviation below ±2% are typically obtained without the need for a secondary-side feedback. The circuit further contains a suite of powerful protections to ensure a robust LED driver design without the need for extra components or overdesign. Among them, one can list:

- *Over Temperature Thermal Fold-back*: connecting a NTC to the SD pin allows for gradual reduction of the LED current down to 50% of its nominal value when the temperature is excessive. If the current reduction does not prevent the temperature from reaching a second level, the controller stops operating (SD_OTP).
- *Over Voltage Protection (SD_OVP)*: A Zener diode can further be used on the SD pin to provide an adjustable OVP protection (SD OVP).
- *Cycle-by-cycle Peak Current Limit*: when the current sense voltage exceeds the internal threshold (V_{ILIM}), the MOSFET immediately turns off (cycle-by-cycle current limitation).
- *Winding and Output Diode Short-circuit Protection (WODSCP)*: an additional comparator stops the controller if the CS pin voltage exceeds ($150\% \cdot V_{ILIM}$) for 4 consecutive cycles. This feature can protect the converter if a winding or the output diode is shorted or simply if the transformer saturates.
- *Output Short-circuit Protection (AUXSCP)*: If the ZCD pin voltage remains low for a 90-ms time interval, the controller stops pulsating until 4 seconds has elapsed.
- *Open LED Protection*: if the V_{CC} pin voltage exceeds the OVP threshold, the controller shuts down and waits 4 seconds before restarting switching operation.
- *Floating/Short Pin Detection*: the circuit can detect most of these situations which helps pass safety tests.

Selecting the Right NCL30088 Version

There exist four NCL30088 versions. They differ in:

- Their respective protection mode. The WODSCP, AUXSCP and the SD over-temperature (OTP) and over-voltage (OVP) protections are latching-off (A and C versions) or auto-recovery (the circuit resumes operation after a 4-second delay – B and D versions).
- The internal duty-ratio limitation. NCL30088A/B duty-ratio is internally limited to 50% at the top of the lowest line sinusoid. They are recommended if the lowest line peak voltage is higher than the inductor demagnetization voltage, i.e.,:
  - If $\left(\sqrt{2} \cdot (V_{in,rms})_{LL} \geq V_{out} + V_f\right)$ with non-isolated converters,
  - If $\left(\sqrt{2} \cdot (V_{in,rms})_{LL} \geq \frac{n_p}{n_s}(V_{out} + V_f)\right)$ in flyback applications

  where $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (85 or 90 V rms in general) and (V_f) is the output diode forward voltage. The C and D versions that allow the duty-ratio to reach 60% at the top of the lowest line sinusoid, must be preferred otherwise. See Table 1.

Table 1. SELECTING THE RIGHT NCL30088 VERSION

	WODSCP, AUXSCP, SD_OTP and SD_OVP Protection Mode	**Output Voltage Range for Non-isolated Converters** (Note1)	**Output Voltage Range for Flyback Converters** (Note 2)
NCL30088A (Note 3)	Latching Off	$V_{out} + V_f \le \sqrt{2}(V_{in,rms})_{LL}$	$V_{out} + V_f \le \frac{n_s}{n_p}\sqrt{2}(V_{in,rms})_{LL}$
NCL30088B	Auto-recovery	$V_{out} + V_f \le \sqrt{2}(V_{in,rms})_{LL}$	$V_{out} + V_f \le \frac{n_s}{n_p}\sqrt{2}(V_{in,rms})_{LL}$
NCL30088C (Note 3)	Latching Off	$V_{out} + V_f \le \frac{3}{2}\cdot\sqrt{2}(V_{in,rms})_{LL}$	$V_{out} + V_f \le \frac{n_s}{n_p}\cdot\frac{3}{2}\cdot\sqrt{2}(V_{in,rms})_{LL}$
NCL30088D	Auto-recovery	$V_{out} + V_f \le \frac{3}{2}\cdot\sqrt{2}(V_{in,rms})_{LL}$	$V_{out} + V_f \le \frac{n_s}{n_p}\cdot\frac{3}{2}\cdot\sqrt{2}(V_{in,rms})_{LL}$

1. $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (e.g., 85 V rms), (V_f), the output diode forward voltage.
2. $(V_{in,rms})_{LL}$ is the lowest-line rms voltage (e.g., 85 V rms), (V_f), the output diode forward voltage.
3. Please contact local sales representative for availability.

As an example, let's assume that we must design a 90 to 265 V rms, non-isolated buck-boost converter whose output can be as high as 150 V. Let's see if A/B version can be used.

$$\sqrt{2}(V_{in,rms})_{LL} = \sqrt{2}\cdot 90 \cong 127V \le V_{out} + V_f \cong 150V \quad \text{(eq. 1)}$$

Eq. 1 indicates that the Table 1 condition of using the A and B versions in non-isolated converters applications is not met. Hence, the A/B version is not recommended while the C or D version is ok since:

$$\frac{3}{2}\cdot\sqrt{2}(V_{in,rms})_{LL} = \frac{3}{2}\cdot\sqrt{2}\cdot 90 \cong 191V \ge V_{out} + V_f \cong 150V \quad \text{(eq. 2)}$$

Generally speaking, the A and B versions are typically preferred in narrow-mains non-isolated converters or flyback LED drivers [the turns ratio of isolated flyback converters, gives some flexibility − see Table 1 conditions]. C and D versions are generally to be selected for wide-mains, non-isolated converters.

If the duty-ratio limitation is exceeded by your application, the LED current will be below its nominal value at the lowest line voltage but will meet the target when the input voltage level is sufficient. Thus, you can start with the NCL30088A or the NCL30088B and consider the NCL30088C or NCL30088D if the LED current is too low at the lowest line levels. By the way, a symptom of the duty-ratio limitation effect can be observed as shown by Figure 1 where the input current is clamped by the over-current protection during normal load conditions.

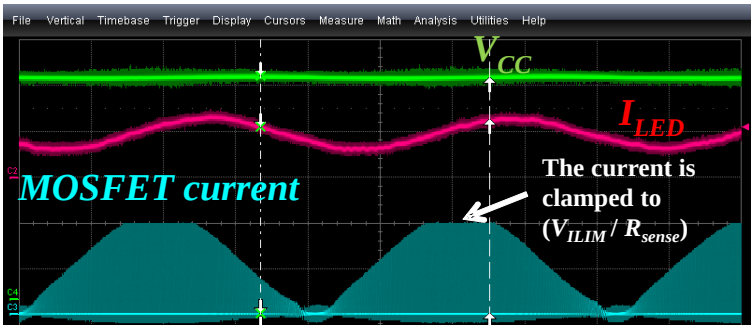

Figure 1. Current Over-current Limitation
(V_{ILIM} is the Over-current Threshold, R_{sense} the Current Sense Resistor)

Our application of interest is a flyback converter. In this case, the turns ratio must be considered when selecting the appropriate version. We will see that in this specific case, the NCL30088B is the appropriate option.

LED Driver Dimensioning

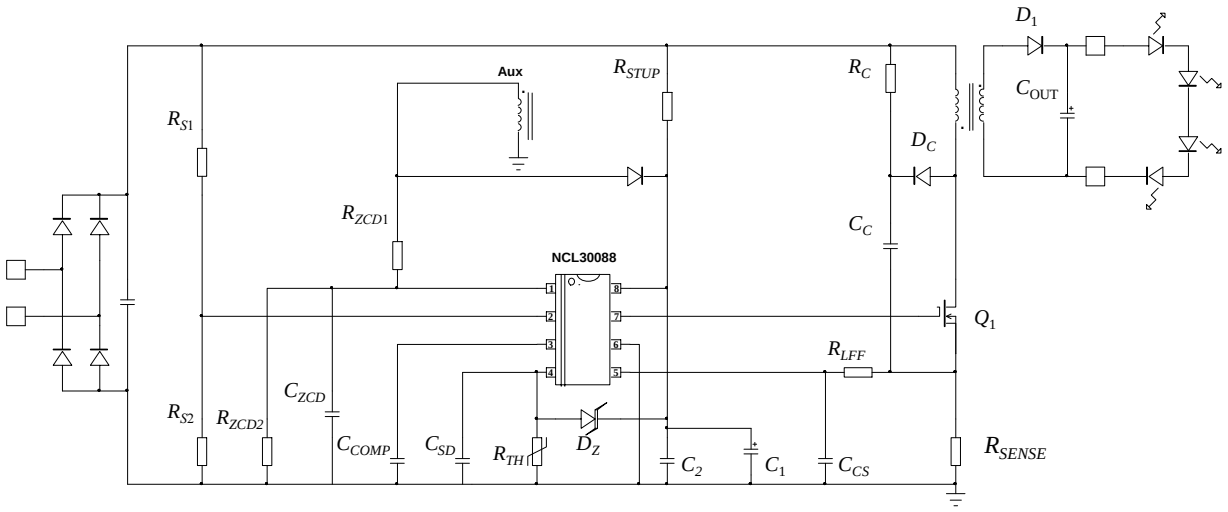

Figure 2. Basic Schematic

STEP 1: POWER COMPONENTS SELECTION

Basically, the transformer, the output capacitor and the power silicon devices are dimensioned “as usual”, that is, as done with any other PF corrected, quasi-resonant flyback converter. This chapter does not detail this process, but highlights the major points.

Transformer Selection

Selecting the Auxiliary Winding Number of Turns

An auxiliary winding is necessary for zero current detection and to provide the V_{CC} voltage. The output voltage of a LED driver generally exhibits a large range. The V_{CC} voltage provided by the auxiliary winding will vary in a similar manner. The NCL30088 features a large V_{CC} range to address these variations. Practically, after start-up, the operating range is 9.4 V up to 25.5 V.

NOTE: $(V_{CC(OVP)})_{min}$ = 25.5 V is the threshold minimum value of the V_{CC} over-voltage protection. This safety feature protects the circuit if the LED string happens to be disconnected.

The auxiliary winding number of turns can be selected so that the auxiliary voltage is slightly below $(V_{CC(OVP)})_{min}$ when the output voltage is at a maximum factoring in impact of the 100/120-Hz ripple. Practically, this criterion turns into:

$$\frac{n_{AUX}}{n_S}(V_{out,max} + V_f) \le (V_{CC(OVP)})_{min} + V_f \quad \text{(eq. 3)}$$

Hence:

$$n_{AUX} \le n_S \cdot \frac{(V_{CC(OVP)})_{min} + V_f}{V_{out,max} + V_f} \quad \text{(eq. 4)}$$

This leads in our case to:

$$n_{AUX} \le n_S \cdot \frac{25.5}{20 + 1} \cong 1.3 \cdot n_S \quad \text{(eq. 5)}$$

Practically, we will select ($n_{AUX} = n_S$).

In this case, V_{CC} will be in the range of V_{out} , with some deviations due to the imperfect coupling.

Selecting the Secondary Winding Number of Turns

In general, N_{PS}, the secondary to primary transformer turns ratio ($N_{PS} = n_S / n_P$) [n_P designates the primary number of turns, n_S , the secondary number of turns] is selected as low as possible so that the input current stress is reduced. N_{PS} cannot be too small however. N_{PS} sets the amount of voltage reflected during the off-time (see Figure 3) and hence, must be high enough to limit the voltage stress across the primary-side MOSFET. Indeed, the voltage to be sustained by the primary-side MOSFET and the output diode are:

$$V_{DS,max} = \sqrt{2}(V_{in,rms})_{max} + \frac{V_{out} + V_f}{N_{PS}} + V_{Q-ov} \quad \text{(eq. 6)}$$

$$V_{diode,max} = N_{PS}\sqrt{2}(V_{in,rms})_{max} + V_{out} + V_f + V_{D-ov}$$

Where:

- N_{PS} is the secondary to primary transformer turns ratio $N_{PS} = n_S / n_P$
- V_{Q-ov} is the MOSFET overvoltage shown in Figure 3. This overshoot is due to the leakage inductor reset. It is limited by the clamping network consisting of D_C, C_C and R_C of Figure 2.
- V_{D-ov} is a similar overshoot that occurs across the output diode when the MOSFET turns on.

The clamping network is often designed so that V_{Q-ov} is between 50% and 100% of the reflected voltage:

$$V_{Q-ov} = k_C \cdot \frac{v_{out} + V_f}{N_{PS}} \quad \text{with} \quad 0.5 \le k_c \le 1.0 \qquad \text{(eq. 7)}$$

We can estimate the maximum voltage reached on the drain node, considering $V_{out(OVP)}$ level as the maximum output voltage:

$$V_{ds,max} = \sqrt{2} \cdot (V_{in,rms})_{HL} + \frac{(1 + k_c)(V_{out(OVP)} + V_f)}{N_{PS}} \qquad \text{(eq. 8)}$$

Some derating is generally requested. The typically-applied 15% safety factor implies that the MOSFET voltage does not exceed 85% of its breakdown voltage. Hence:

$$V_{ds,max} = \sqrt{2} \cdot (V_{in,rms})_{HL} + \frac{(1 + k_c)(V_{out(OVP)} + V_f)}{N_{PS}} \le 85\%V_{DSS} \qquad \text{(eq. 9)}$$

Where V_{DSS} is the MOSFET breakdown voltage.

Finally:

$$\frac{n_P}{n_S} \le \frac{85\%V_{DSS} - \sqrt{2} \cdot (V_{in,rms})_{HL}}{(1 + k_c)(V_{out(OVP)} + V_f)} \qquad \text{(eq. 10)}$$

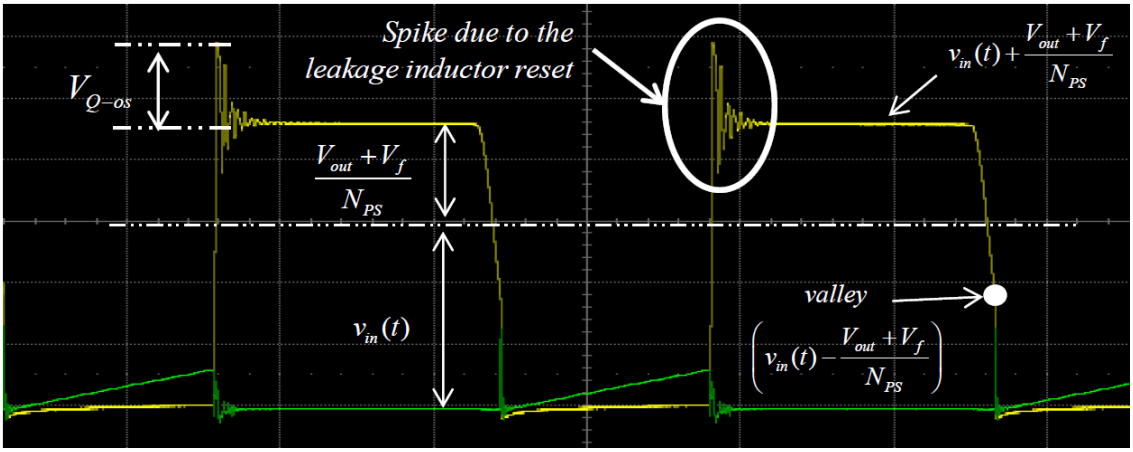

Figure 3. MOSFET Drain-source Voltage (Yellow Trace) and Current (Blue)

In our application, $(V_{in,rms})_{HL}$ is 265 V rms and $(V_{out(OVP)} + V_f)$ is about 28 V.

With a 600 V MOSFET,

$$\frac{n_P}{n_S}(1 + k_c) \le \frac{85\% \cdot 600 - \sqrt{2} \cdot 265}{28} \cong 4.8 \qquad \text{(eq. 11)}$$

With a 800 V MOSFET,

$$\frac{n_P}{n_S}(1 + k_c) \le \frac{85\% \cdot 800 - \sqrt{2} \cdot 265}{28} \cong 10.9 \qquad \text{(eq. 12)}$$

We select the second option (800 V MOSFET) with $\left(\frac{n_P}{n_S} = 6\right)$ and (k_C = 80%), which meets Eq. 12 requirements since $\left(\frac{n_P}{n_S}(1 + k_c) = 6 \cdot 180\% = 10.8 \le 10.9\right)$.

It can be easily checked that the Table 1 condition of using the A or B version is met. The NCL30088B will be used for this application.

Selecting the Primary Inductance

Assuming a quasi-resonant operation and neglecting the small delay necessary for detecting the MOSFET drain-source valley, the primary inductance dictates the switching frequency as follows:

$$f_{sw} = \frac{(V_{in,rms})^2}{2L_P P_{in,avg}} \cdot \left(\frac{V_{out} + V_f}{N_{PS}\, v_{in}(t) + V_{out} + V_f}\right)^2 \qquad \text{(eq. 13)}$$

The switching frequency is a rising function of the rms line voltage. At a given line magnitude, the switching frequency is yet higher near the line zero crossing and decays as the line voltage rises due to the ($v_{in}(t)$) term.

Note that when high-line conditions are detected (see NOTE), the NCL30088 does not operate in quasi-resonant mode but delays the MOSFET turn on until the 2nd valley is detected (see Figure 4). This reduces the switching frequency upper range and optimizes the high-line efficiency.

NOTE: The input voltage is sensed by the V_S pin for brown-out protection, feedforward and line range detection. High-line conditions are detected when the V_S pin voltage exceeds 2.4 V typically. See data sheet for more details.

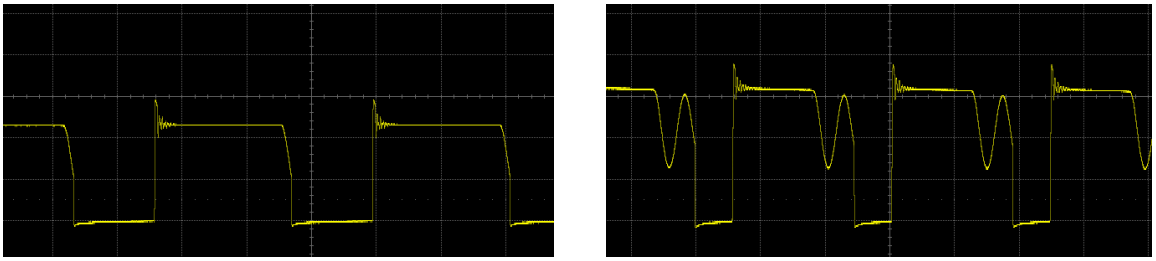

Figure 4. Quasi-Resonant Mode in Low Line (Left), Turn On at Valley 2 when in High Line (Right)

The primary inductor will be selected with respect to the targeted switching frequency range, keeping in mind that:

- High switching frequency levels reduce the size of the storage elements
- Conversely, increasing the switching frequency leads to more switching noise and losses. Also, EMI filtering may be tougher because of the EMI generated at the switching frequency and close harmonic levels. Most power supplies have to meet standards which apply to frequencies above 150 kHz. That is why SMPS designers often select F_{SW} = 130 kHz to keep the fundamental component below 150 kHz and then out of the regulation scope. Often, 65 kHz is also chosen to not to have to damp harmonic 2 too.

As the rule of thumb, let us select L_P as follows:

- In wide mains application: choose L_P so that the switching frequency is below 65 kHz at the low-line range nominal voltage (typically 115 V rms) over a large part of the sinusoid. Practically, we can select that the frequency target will have to meet starting from $(V_{in,pk}/2)$ that is $\left(\sqrt{2}\cdot 115/2\right)$. This arbitrary choice relies on the idea that for below this line voltage level the input current is relatively small and easy to filter. Check that at the high-line nominal voltage (230 V rms typically), the switching frequency stays below 65 kHz thanks to the valley-2 operation.
- Similarly, in a narrow mains operation case, select L_P so that the switching frequency is below 65 kHz at the nominal line voltage when $\left(\nu_{in}(t) = V_{in,pk}/2\right)$

Our application is a wide-range one.

Let us compute L_P so that at 115 V rms, the switching frequency is below $f_{sw,T}$ = 65 kHz:

$$L_P \geq \frac{(V_{in,rms})^2}{2 f_{sw,T} P_{in,avg}} \cdot \left(\frac{V_{out} + V_f}{N_{PS}\frac{\sqrt{2}\cdot V_{in,rms}}{2} + V_{out} + V_f} \right)^2 \quad \text{(eq. 14)}$$

Which leads to:

$$L_P \geq \frac{115^2}{2 \cdot 65 \cdot 10^3 \cdot 12} \cdot \left(\frac{12+1}{\frac{\sqrt{2}\cdot 115}{6\cdot 2} + 12 + 1} \right)^2 \cong 2\ \text{mH} \quad \text{(eq. 15)}$$

Finally we have to consider the primary current magnitude constraints:

$$(I_{L,pk})_{max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cdot \left(1 + \frac{N_{PS}(V_{in,rms})_{LL}}{V_{out} + V_f}\right) \quad \text{(eq. 16)}$$

$$(I_{L,pk})_{max} = \frac{2}{\sqrt{3}} \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \sqrt{1 + \frac{16\sqrt{2}\cdot (V_{in,rms})_{LL}}{3\pi \cdot \frac{V_{out}+V_f}{N_{PS}}} + \frac{6\pi \cdot (V_{in,rms})_{LL}^2}{4 \cdot \left(\frac{V_{out}+V_f}{N_{PS}}\right)^2}} \quad \text{(eq. 17)}$$

In our application, assuming an efficiency of 84% ($(P_{in,avg})_{max}$ = 12 W), Eq. 16 and Eq. 17 lead to:

$$(I_{L,pk})_{max} = 2\sqrt{2} \cdot \frac{12}{90} \cdot \left(1 + \frac{\frac{90}{6}}{20+1}\right) \cong 0.65\ \text{A} \quad \text{(eq. 18)}$$

$$(I_{L,rms})_{max} = \frac{2}{\sqrt{3}} \cdot \frac{12}{90} \cdot \sqrt{1 + \frac{16\sqrt{2}\cdot 90}{3\pi \cdot 6 \cdot 21} + \frac{6\pi \cdot 90^2}{4 \cdot (6\cdot 21)^2}} \cong 350\ \text{mA} \quad \text{(eq. 19)}$$

We selected transformer 750871144 from Wurth Elektronik with the following characteristics: L_P = 1.9 mH, $n_P / n_{AUX} = n_P / n_S = 6$.

Power Switches

MOSFET

The voltage constraints on the MOSFET have been discussed in the transformer section. Conduction losses depend on the MOSFET rms current which can be computed with the following equation:

$$(I_{Q,rms})_{max} = \frac{2}{\sqrt{3}} \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \sqrt{1 + \frac{8\sqrt{2} \cdot (V_{in,rms})_{LL}}{3\pi \cdot \frac{V_{out}+V_f}{N_{PS}}}} \quad \text{(eq. 20)}$$

A NDD03N80 MOSFET is selected (DPAK, 800 V, 4.5 Ω).

Output Diode

Similarly, the voltage constraints have been discussed in the previous section.

Losses are mainly produced by the average current flowing through the diode. This average is simply the LED current (0.5 A in our case).

A 200-V, 2-A SMB diode is selected (MURS220).

Snubber and Clamping Network

A snubber capacitor can be placed across the MOSFET to reduce the dV/dt and lower the switching noise. A 47-pF, 1,000-V capacitor is placed in our application (C_2 of Figure 9). Note that for optimal operation, it is recommended to connect the snubber capacitor between the MOSFET drain and source terminals rather than between drain and ground.

When the MOSFET turns off, the magnetizing inductor energy is conveyed to the secondary side and charges the output. The leakage inductor current cannot be used by the output. It must be diverted from the MOSFET. If not, the MOSFET drain-source voltage would rise to destructive levels. A clamping network is hence necessary. Such a circuit requires a diode, a resistor and a capacitor (D_C, R_C and C_C of Figure 2):

- The capacitor C_C absorbs the leakage inductor energy when the MOSFET turns off. The voltage rating of this capacitor must be equal to the MOSFET breakdown voltage or higher. Note that similarly to the snubber capacitor, the C_C negative terminal should preferably be connected to the MOSFET source rather than to ground.
- The resistor R_C loads C_C to ensure that the C_C voltage does not drift up but stabilize at a level which ensures a proper MOSFET protection (the MOSFET voltage is clamped to the C_C voltage by means of D_C).
- The diode D_C prevents C_C from discharging when the MOSFET turns on. This diode is generally a fast-recovery diode. A low-value resistor (R_{14} of Figure 9) is inserted to limit the current spike which otherwise occurs when the MOSFET turning off, C_C abruptly charges. Do not oversize this series resistor. The leakage current flowing through it creates a voltage drop. The MOSFET voltage is clamped to the C_C voltage ***PLUS*** the series resistor voltage. In our case, the maximum leakage current is (V_{ILIM}/R_{sense}) that is $(1\,V\,/\,1.5\,\Omega \cong 667\,mA)$. In our design, a 22 Ω resistor is implemented that results in an overshoot less than $(22\,\Omega \cdot 0.667 \cong 17\,V)$.

Eq. 8 gives the maximum voltage

$$\left(\sqrt{2} \cdot (V_{in,rms})_{HL} + \frac{(1 + k_c)(V_{out(OVP)} + V_f)}{N_{PS}}\right)$$

the MOSFET must sustain. This voltage is the C_C maximum voltage. Hence, the energy that R_C can consume and re-inject to the input over a switching cycle is given by:

$$E_{R_C} = \frac{\frac{(1+k_c)\cdot(V_{out(OVP)}+V_f)}{N_{PS}} \cdot \left(\frac{(1+k_c)\cdot(V_{out(OVP)}+V_f)}{N_{PS}} + \sqrt{2} \cdot (V_{in,rms})_{HL}\right) \cdot T_{SW}}{R_C} \quad \text{(eq. 21)}$$

The energy due to the leakage inductor must be handled. It is maximal when the primary current exceeds its $\left(\frac{V_{ILIM}}{R_{sense}}\right)$ limit where V_{ILIM} is the over-current protection threshold and R_{sense}, the current sense resistor:

$$E_{L_{leak}} = \frac{1}{2} L_{leak} \left(\frac{V_{ILIM}}{R_{sense}}\right)^2 \cdot \frac{\frac{(1+k_c)\cdot(V_{out(OVP)}+V_f)}{N_{PS}}}{\frac{(1+k_c)\cdot(V_{out(OVP)}+V_f)}{N_{PS}} - \frac{(V_{out(OVP)}+V_f)}{N_{PS}}} = \frac{1 + k_C}{2 \cdot k_C} L_{leak} \left(\frac{V_{ILIM}}{R_{sense}}\right)^2 \quad \text{(eq. 22)}$$

This energy of Eq. 21 must be equal or higher than the leakage inductor energy defined in Eq. 22. From this, we can deduce the following minimum R_C value:

$$R_C \le \frac{\frac{(V_{out(OVP)}+V_f)}{N_{PS}} \cdot \left(\frac{(1+k_c)\cdot(V_{out(OVP)}+V_f)}{N_{PS}} + \sqrt{2} \cdot (V_{in,rms})_{HL}\right)}{\frac{1}{2 \cdot k_C} L_{leak} \left(\frac{V_{ILIM}}{R_{sense}}\right)^2 \cdot f_{SW}} \quad \text{(eq. 23)}$$

Select the C_C capacitor so that the time constant ($R_C \cdot C_C$) is large compared to a switching period, practically, in the range of 1 ms.

Since in our application, we have selected (k_C = 80%), it comes:

$$R_C \le \frac{28 \cdot 6\left((180\% \cdot 28 \cdot 6) + \sqrt{2} \cdot 265\right)}{\frac{1}{2 \cdot 80\%}\, 20\mu \left(\frac{1}{1.5}\right)^2 \cdot 65k} \cong 315\ k\Omega \quad \text{(eq. 24)}$$

This resistor will dissipate $\frac{(180\% \cdot 28 \cdot 6)^2}{315k} \cong 290\ mW$

Two 470 kΩ, 1/2 W resistors are placed in parallel for the following effective resistance: (470 k || 470 k = 235 kΩ).

A 4.7 nF/100 V capacitor is implemented for C_C that with R_C forms a 1.1 ms time constant.

Output Capacitor

The power delivered by PFC converters exhibits a large ac component at twice the line frequency. To some extend, the output capacitor compensates for it but yet, the output current exhibits some ripple inversely proportional to the capacitor value (C_{out}).

Below equation expresses the current ripple:

$$\frac{(\Delta I_{out})_{pk-pk}}{I_{out,nom}} = \frac{2}{\sqrt{1 + (4\pi \cdot f_{line} \cdot R_{LED} \cdot C_{out})^2}} \quad \text{(eq. 25)}$$

From Eq. 25, the following minimum value for C_{out} can be deduced (Eq. 26):

$$C_{out,min} = \frac{\sqrt{\left[\frac{2}{\frac{(\Delta I_{out})_{pk-pk}}{I_{out,nom}}}\right]^2 - 1}}{4\pi \cdot f_{line,min} \cdot R_{LED,min}} \quad \text{(eq. 26)}$$

C_{out} must then be large enough to avoid an excessive current ripple which could reduce the LED reliability. The flicker index is commonly specified below 0.15. This requirement corresponds to a 100% peak-to-peak ripple in a PF-corrected LED driver with a sinusoidal output current shape

This criterion (100% peak to peak ripple), leads to:

$$\frac{(\Delta I_{out})_{pk-pk}}{I_{out,nom}} = 1 \quad \text{(eq. 27)}$$

In our application the minimum LED dynamic resistance is estimated to be 6 Ω and the minimum line frequency is 50 Hz. In this case, the minimum output capacitor value is:

$$C_{out,min} = \frac{\sqrt{\left(\frac{2}{1}\right)^2 - 1}}{2 \cdot 100\pi \cdot 6} \cong 460\ \mu F \quad \text{(eq. 28)}$$

A 470 F/35 V is implemented.

Bulk Capacitor Heating:

It must also be checked that the ESR is low enough to prevent the rms current that flows through it, from overheating the bulk capacitor. This capacitor rms current can be estimated using the following expression.

$$(I_{C,rms})_{max} = \sqrt{\left[\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{n_P}{n_S}\right)^2 \cdot \frac{(P_{in,avg})_{max}^2}{V_{in,rms} \cdot \frac{V_{out}+V_f}{N_{PS}}}\left[1 + \frac{9\pi^2}{16\sqrt{2}} \cdot \frac{V_{in,rms}}{\frac{V_{out}+V_f}{N_{PS}}}\right]\right] - I_{out,nom}^2} \quad \text{(eq. 29)}$$

It remains wise to check the output capacitor heating in the lab.

STEP 2: OUTPUT CURRENT SETTING

As explained in the data sheet, the output current is regulated to equal the following $I_{out,nom}$ nominal output current:

$$I_{out,nom} = \frac{V_{REF}}{2N_{PS}R_{sense}} \quad \text{(eq. 30)}$$

Where:

- N_{PS} is the secondary to primary transformer turns ratio $N_{PS} = n_S / n_P$
- R_{sense} is the current sense resistor (see Figure 2)
- V_{REF} is the output current internal reference.

Hence once the transformer is designed, N_{PS} is known and the only current sense resistor dictates the output current level.

$$R_{sense} = \frac{V_{REF}}{2N_{PS}I_{out,nom}} \quad \text{(eq. 31)}$$

The power dissipated by R_{sense} can be computed by the following equation:

$$P_{R_{sense}} = \frac{4}{3}R_{sense}\left(\frac{P_{in,avg}}{V_{in,rms}}\right)^2\left[1 + \frac{8\sqrt{2} \cdot V_{in,rms}}{3\pi \cdot \frac{V_{out}}{N_{PS}}}\right] \quad \text{(eq. 32)}$$

In our application:

- N_{PS} = 1/6
- $I_{out,nom}$ = 500 mA
- $(P_{in,avg})_{max}$ = 12 W
- $(V_{in,rms})_{LL}$ = 90 V
- $V_{out,min}$ = 10 V

Hence:

$$R_{sense} = \frac{250 \cdot 10^{-3}}{2 \cdot \frac{1}{6} \cdot 500 \cdot 10^{-3}} = 1.5\ \Omega \qquad \text{(eq. 33)}$$

And:

$$P_{R_{sense}} = \frac{4}{3} 1.5 \left(\frac{12}{90}\right)^2 \left(1 + \frac{8\sqrt{2} \cdot 90}{3\pi \cdot \frac{10}{1/6}}\right) \cong 100\ mW \qquad \text{(eq. 34)}$$

Two 3 Ω resistors are placed in parallel.

Input Voltage Sensing and Feedforward:

A portion of the input voltage must be applied to the V_S pin to provide the circuit with the sinusoidal reference necessary for shaping the input current (PFC). The obtained current reference is further modulated so that when averaged over a half-line period, it is equal to the output current reference (V_{REF}). This averaging process is made by an internal Operational Trans-conductance Amplifier (OTA) and the capacitor connected between the COMP pin (pin3) and ground. The recommended minimum COMP capacitance is 1 μF.

COMP Pin Capacitor

A 1 μF capacitor is to be placed between COMP pin and ground.

Input Voltage Sensing

A resistors divider (R_{S1} and R_{S2} of Figure 2) provides pin 2 with the V_S signal. The scale-down factor is computed in accordance with the brown-out protection. If $(V_{in,rms})_{BOH}$ is the targeted minimum line rms voltage necessary for entering operation, R_{S1} and R_{S2} must comply with:

$$\frac{R_{S2}}{R_{S1} + R_{S2}} \cdot \sqrt{2} (V_{in,rms})_{BOH} = V_{BO(on)} \qquad \text{(eq. 35)}$$

Where $V_{BO(on)}$ is the internal threshold (1 V typically) the V_S pin voltage must exceed to allow circuit operation.

In other words,

$$R_{S1} = R_{S2} \left(\frac{\sqrt{2} \cdot (V_{in,rms})_{BOH}}{V_{BO(on)}} - 1\right) \qquad \text{(eq. 36)}$$

R_{S2} values in the range of 50 kΩ generally provide a good tradeoff between losses and noise immunity. In our application, we select 47 kΩ. Our system being supposed to enter operation when the line voltage exceeds 81 V rms:

$$R_{S1} = 47 \cdot 10^3 \cdot \left(\frac{\sqrt{2} \cdot 81}{1} - 1\right) \approx 5.4\ M\Omega \qquad \text{(eq. 37)}$$

It is generally recommended not to have a single resistor placed between a high-voltage rail and a low potential node. Instead, two or more resistors are to be placed in series. In our case, we use two 2,700 kΩ resistors for R_{S1}.

Feedforward

The NCL30088 computes the current setpoint ($V_{control}$) for power factor correction and proper regulation of the LED current. Now, the MOSFET cannot turn off at the very moment when the current-sense voltage exceeds $V_{control}$. There actually exists a propagation delay t_{prop} (Figure 5) for which the primary current keeps rising. As a result, the primary current does not exactly peak to the expected ($V_{control}$ / R_{sense}) value but to a higher level. The output current is hence also affected. Optimal regulation performance requires the peak current increase caused by t_{prop} to be compensated.

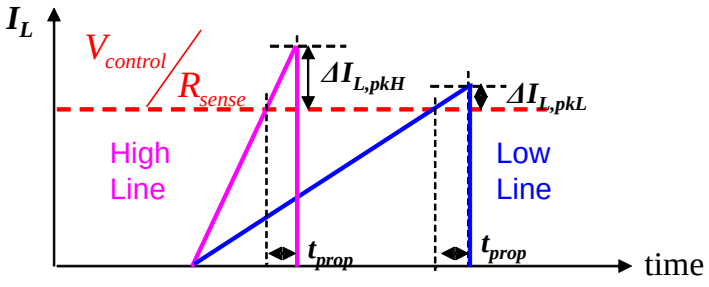

Figure 5. Propagation Delay Effect on Peak Current

The NCL30088 compensates for the propagation delay by sourcing a current proportional to the V_S pin voltage out of the CS pin during the on-time. Placing a resistor R_{LFF} between the CS pin and the sense resistor, the following offset is hence obtained:

$$V_{CS(offset)} = K_{LFF}\, \nu_S\,(t) R_{LFF} \qquad \text{(eq. 38)}$$

Where the V_S pin voltage $v_S(t)$ equates:

$$\nu_S(t) = \frac{R_{S2}}{R_{S1} + R_{S2}}\, \nu_{in}(t) \qquad \text{(eq. 39)}$$

Since the CS pin offset must compensate for $\left(R_{sense} \cdot \Delta I_{L,pk} = \frac{R_{sense} \cdot \nu_{in}(t) \cdot t_{prop}}{L_P}\right)$, the offset resistor value can be computed as follows:

$$R_{LFF} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \frac{t_{prop} R_{Sense}}{L_P K_{LFF}} \qquad \text{(eq. 40)}$$

Where:

- K_{LFF} is the V_S pin voltage to CS pin current conversion ratio. Its typical value is 20 μS.
- R_{S1} and R_{S2} are the input voltage sensing resistors (see Figure 2).

Parameter t_{prop} includes the controller internal delay of the controller (about 50 ns) and the MOSFET turning off time. Thus, it varies with respect to the chosen MOSFET and the way it is driven (value of the gate resistors for instance). As a consequence, it is difficult to predict its exact value prior to evaluating the LED driver design.

However, for a first approximation, we can calculate R_{LFF}, using t_{prop} = 200 ns.

Then, the offset resistor value can be fine-tuned on the bench so that the output current characteristic is nearly flat over the line voltage range.

Using Eq. 40, we can calculate the first value of R_{LFF} for our design:

$$R_{LFF} = \left(1 + \frac{R_{S1}}{R_{S2}}\right) \frac{t_{prop} R_{Sense}}{L_P K_{LFF}} = \qquad \text{(eq. 41)}$$

$$= \left(1 + \frac{5400}{47}\right) \frac{200n \times 1.5}{1900\mu \times 20\mu} \cong 915\Omega$$

After experiments in the lab, R_{LFF} value was decreased to 820 Ω.

Important Note: As indicated in the NCL30088 data sheet, R_{LFF} must be selected higher than 250 Ω. If not, the circuit may improperly detect that the CS pin is grounded.

Selecting the CS Pin Capacitor

The shape of the current-sense voltage influences the output current regulation. If the CS pin filter (R_{LFF}, C_{CS}) is too big, the output current setpoint will vary (I_{out} higher than expected value). Thus, once R_{LFF} has been chosen, it is important to keep the value of C_{CS} as small as possible to have an optimal output current regulation. C_{CS} should be in the range of 10–100 pF.

Finally: (see Table 2)

Table 2.

R_{S1}	R_{S2}	C_{COMP}	R_{SENSE}	R_{LFF}	C_{CS}
5400 kΩ (two 2.7 MΩ placed in series)	47 kΩ	1 μF	1.5 Ω (two 3 Ω resistors in parallel)	820 Ω	–

NCL30088 proprietary regulation technique ensures a very precise LED current control.

Please note that sources of deviation are however to be considered. They are detailed in [3]. Let's recall the main points:

- The NCL30088 regulates the total current provided by the converter, that are, the LED current plus the V_{CC} current. Hence, the actual output current is:

$$I_{out,nom} = \frac{N_P \cdot V_{REF}}{2 \cdot N_S \cdot R_{sense}} - \frac{N_{Aux}}{N_S}\, I_{CC} \qquad \text{(eq. 42)}$$

In general, the $\left(\frac{N_{Aux}}{N_S}\, I_{CC}\right)$ term is small compared to the target LED current and can be ignored. If not, R_{sense} should be reduced to compensate for the circuit consumption.

- The output current value depends on the sense resistor (R_{sense}). Select a precise resistor and avoid long tracks that lead to an additional series resistance. If R_{sense} is 1 Ω and that the circuit additionally senses the voltage across a 20 mΩ track, the total sensing resistor will be 1.02 Ω instead of 1 Ω. Ultimately, the output current will 2% below target.
- Avoid inductive sense resistor. If not, the output current will be less than the target because of the offset the series inductor causes on the CS pin voltage: $\left(\frac{l_{R_{sense}}}{L_P} \cdot \nu_{in}(t)\right)$ where $l_{R_{sense}}$ is the R_{sense} parasitic inductance.

STEP 3: SD PIN MANAGEMENT

The Thermal Foldback and Shutdown block of the NCL30088 is inherited from the NCL30082 and its functioning and design is detailed in application note AND9131/D ([2]). Only key points will be highlighted here.

Selecting the SD Over-voltage Zener Diode

A Zener diode can be placed between the V_{CC} and the SD pins. The circuit detects an OVP fault if the SD pin voltage exceeds 2.5 V. Note that the NCL30088 ensures that a 700 μA minimum current flows through the Zener diode in this case (see [1]) so that it can be operated far from its knee region. The SD OVP threshold on V_{CC} is:

$$(V_{CC})_{SD,OVP} = V_Z + V_{OVP} \qquad \text{(eq. 43)}$$

Where V_{OVP} is the 2.5-V SD OVP threshold.

An SD OVP fault is detected if V_{CC} exceeds $(V_{CC})_{SD,OVP}$. For instance, if you applied a Zener diode exhibiting an 18-V Zener breakdown voltage (when biased by a 700 μA current), the SD_OVP protection will trip when V_{CC} exceeds (18.0 + 2.5) volts, that is, 20.5 V. In this case, the NCL30088B/D stops operating for the auto-recovery 4 s delay. At the end of this time, the circuit attempts to resume operation. If the fault is still present, the circuit again detects an SD OVP fault and stops for 4 s. Finally, the NCL30088B or NCL30088D enters a safe, very low duty-ratio burst mode. An SD OVP fault leads the NCL30088A and NCL30088C to latch off until the LED driver is unplugged and V_{CC} drops below $V_{CC(reset)}$. At that moment, the fault is cleared and the circuit can resume operation.

Such a programmable protection feature is useful if the fixed V_{CC} OVP protection which trips when V_{CC} exceeds $V_{CC(OVP)}$ (26.8 V typically) does not clamp the output voltage at a low enough level. This is not the case in our application. No Zener diode is hence implemented.

Selecting the Thermistor

The resistance of a Negative Coefficient Temperature thermistor (NTC) reduces when its temperature rises. An NTC is to be placed between the SD pin and ground to detect an over-temperature condition. In response to a high temperature, the circuit gradually reduces the LED current down 50% of its nominal value. If despite the current reduction, the temperature still increases, the circuit will eventually stop operation. In general a 50% reduction in current is more than a 50% drop dissipated power as the LED forward voltage will decrease as the current is folded back.

More specifically, as shown by Figure 6, R_{th} designating the NTC resistance:

- The circuit starts to gradually reduce the output current when R_{th} drops below $R_{TF(start)}$ and continues diminishing it until R_{th} goes below $R_{TF(stop)}$.
- At that moment, it maintains the output current at 50% of its nominal level as long as R_{th} is between $R_{TF(stop)}$ and $R_{OTP(off)}$. If on the contrary, a temperature decay leads R_{th} to rise above $R_{TF(stop)}$, the current increases according the precedent characteristics. If R_{th} exceeds $R_{TF(start)}$, full current capability is recovered.
- The LED driver totally stops operating if R_{th} drops below $R_{OTP(off)}$ and stays off until the temperature having reduced, R_{th} exceeds $R_{OTP(on)}$. At that moment, the circuit resumes (NCL30088B and NCL30088D only – A and C versions latch off) and delivers 50% of the nominal current.
- If R_{th} further rises, the current regulation grows as well until R_{th} reaches $R_{TF(start)}$. At that moment, the LED driver provides the full current.

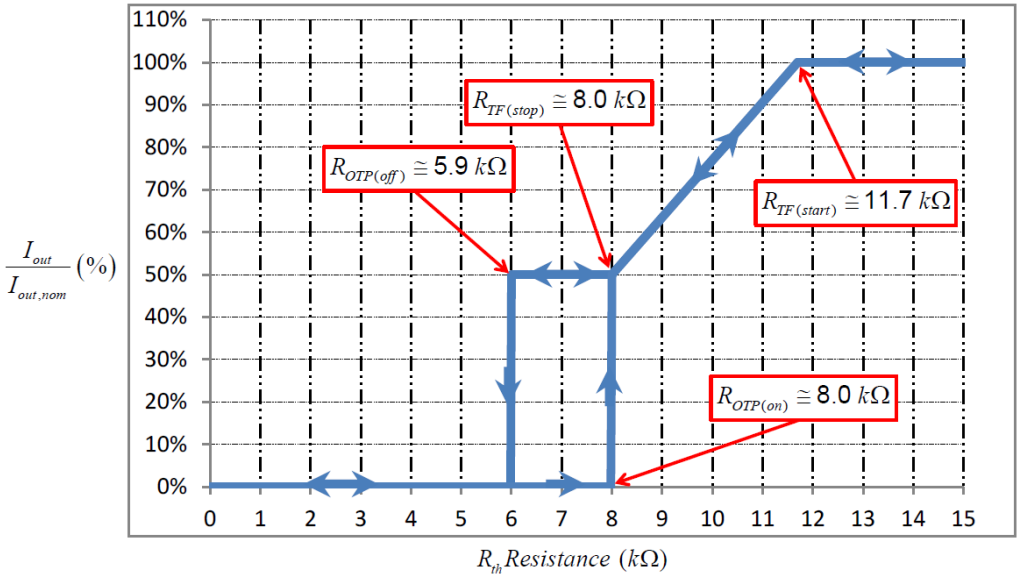

Figure 6. Thermal Foldback Characteristics and Over-temperature Protection

As an example, if thermistor NB12P00104JBB from AVX is implemented:

- The circuit starts to reduce the output current at about 82°C ambient temperature.
- The circuit stops operation at about 104°C ambient temperature.
- The circuit recovers operating at about 90°C ambient temperature.

Selecting the SD Pin Capacitor

A small capacitor can be placed between the SD pin and ground to prevent the pin from picking up possible surrounding noise. Please note that the value of this capacitor must not exceed **4.7 nF** so that it can charge to its nominal level before the OTP blanking time has elapsed.

NOTE: At start-up, the controller blanks the SD function until a delay of 250 μs minimum (OTP blanking time), has elapsed, to provide C_{SD} with enough time to properly charge above the 0.5 V over-temperature threshold. If not, the low SD pin voltage will be considered as caused by the low-resistance of an NTC in excessive temperature conditions.

Finally: (see Table 3)

Table 3.

D_Z	R_{th}	C_{SD}
N/A	NB12P00104JBB (AVX)	1 nF

STEP 4: AUXILIARY WINDING AND V_{CC} MANAGEMENT

V_{CC} Capacitor Refueling

In nominal operation, the auxiliary winding provides the V_{CC} voltage as shown by Figure 2. The auxiliary winding number of turns (n_{aux}) is computed in the transformer section of the “Step 1” paragraph. Note that during the on-time, diode D_{AUX} of Figure 2 rectifies the auxiliary voltage to provide V_{CC}. Hence, neglecting the turn on spike, D_{AUX} must be able to sustain:

$$V_{D_{AUX}} = V_{CC} + \left(\frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot (V_{in,rms})_{HL}\right) \quad \text{(eq. 44)}$$

The V_{CC} highest value is the maximum voltage the $V_{CC(OVP)}$ threshold can take (28.5 V). Therefore:

$$V_{D_{AUX}} = (V_{CC(OVP)})_{max} + \left(\frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot (V_{in,rms})_{HL}\right) \quad \text{(eq. 45)}$$

In our case:

$$V_{D_{AUX}} = (V_{CC(OVP)})_{max} + \left(\frac{n_{AUX}}{n_P} \cdot \sqrt{2} \cdot (V_{in,rms})_{HL}\right) \cong \cong 28.5 + \left(\frac{1}{6} \cdot \sqrt{2} \cdot 265\right) \cong 91\ V \quad \text{(eq. 46)}$$

Due to the turn on spike, some significant headroom is necessary. Selecting a diode exhibiting at least twice the computed V_{RRM} value seems a good practice.

A 250 V/0.2 A BAV21 diode is implemented in our application.

V_{CC} Capacitor Value and Startup Circuitry

When off (that is until V_{CC} has reached the 18-V start-up level), the NCL30088 consumes a very low current (13 μA typically, 30 μA maximum). Thus, high-impedance, low dissipation, resistors can be used to charge the V_{CC} capacitor at start-up.

Note however, that faults like a V_{CC} over-voltage condition lead the LED driver to stop operation and refrain from attempting to recover until a 4 s delay is elapsed. A low duty-ratio burst mode of operation is hence obtained as long as the fault is present. V_{CC} cycles up and down in such a case. For this time, the (off-mode) consumption is slightly higher (75 μA max.). It is hence recommended to have the startup current ($I_{startup}$ in Figure 7) above 75 μA. If not, V_{CC} may collapse and the circuit reset before the 4 s delay has elapsed.

As detailed in application note AND9131/D [2], the startup resistor $R_{startup}$ can either be connected to the bulk rail or to half-wave (Figure 7). Connecting the startup resistor to the half-wave allows decreasing the power dissipated in the startup resistor.

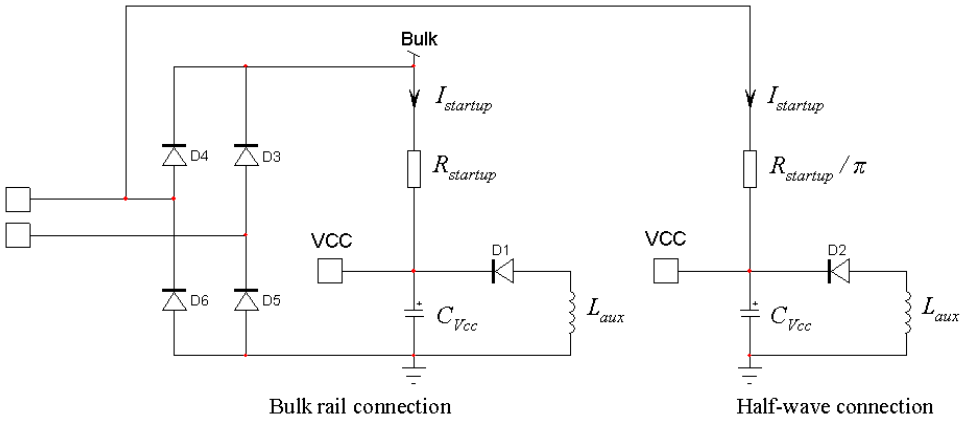

Figure 7. The Startup Resistor can be Connected to the Bulk Rail or to the Half Wave

Calculating the V_{CC} Capacitor

The V_{CC} capacitor value (C_{Vcc}) must be large enough to feed the controller until the auxiliary winding voltage V_{aux} is sufficiently large to supply the controller. The time duration where the controller is supplied by the only C_{Vcc} capacitor is noted t_{reg} (Figure 8).

The circuit enters operation when the V_{CC} capacitor is charged to the $V_{CC(on)}$ startup level. For the t_{reg} duration, the V_{CC} capacitor must be able to maintain the V_{CC} voltage above the UVLO level ($V_{CC(off)}$) while providing the current consumed by the circuit (I_{CC2} specified in the data sheet) and the current necessary to drive the MOSFET.

We can estimate t_{reg} by considering that for this period of time, all the LED driver output current is absorbed by the output capacitor (no current flows through the LED string). t_{reg} lasts until the output voltage reaches the level at which V_{CC} starts to be charged. In general, we try to minimize the C_{Vcc} capacitor by allowing a nearly maximal V_{CC} capacitor discharge, that is, down to a value close to the UVLO level. At that moment, the output voltage will nearly be $\left(V_{out} = (V_{CC(off)})_{max}\frac{n_s}{n_{aux}}\right)$ and t_{reg} can then computed as follows:

$$t_{reg} \cong \frac{C_{out}}{I_{out}}\left((V_{CC(off)})_{max}\frac{n_s}{n_{aux}}\right) \qquad \text{(eq. 47)}$$

Now, using the minimum value of the UVLO hysteresis (minimum value of $V_{CC(on)} - V_{CC(off)}$), the minimum V_{CC} capacitor value comes:

$$C_{Vcc} \geq \frac{(I_{CC2} + Q_g f_{sw})t_{reg}}{(V_{CC(HYS)})_{min}} \cong \frac{n_s \cdot C_{out}}{n_{aux}} \cdot \frac{(I_{CC2} + Q_q f_{sw})}{I_{out}} \cdot \frac{(V_{CC(off)})_{max}}{(V_{CC(HYS)})_{min}} \qquad \text{(eq. 48)}$$

Where:

- I_{CC2} is the NCL30088 consumption at 65 kHz when the DRV pin is unloaded (4 mA max)
- Q_g is the MOSFET total gate charge
- $(V_{CC(HYS)})_{min}$ is the UVLO hysteresis minimum value (8 V)

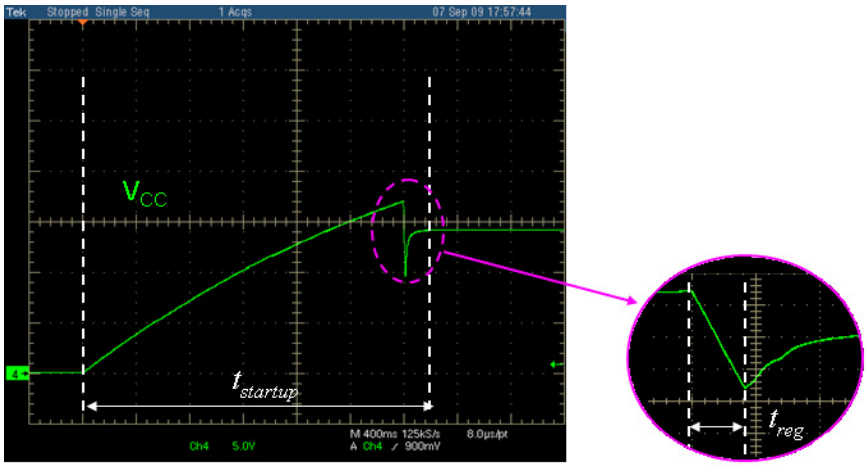

Figure 8. V_{CC} Waveform during Startup

Once the V_{CC} capacitor value is known, the start-up current needed to charge C_{Vcc} can be computed as a function of the maximum acceptable start-up time if specified. Recall anyway that this startup current should not be less than

75 μA so that as explained at the beginning of this section, the circuit does not reset in fault mode. Hence:

$$I_{startup} = \frac{(V_{CC(on)})_{max}\, C_{Vcc}}{t_{startup}} + (I_{CC(start)})_{max} \text{ if } \frac{(V_{CC(on)})_{max}\, C_{Vcc}}{t_{startup}} + (I_{CC(start)})_{max} \geq 75\ \mu A$$

$$I_{startup} = 75\ \mu A \text{ otherwise} \quad \text{(eq. 49)}$$

Where:

- $(V_{CC(on)})_{max}$ is the V_{CC} startup threshold maximum value
- $(I_{CC(start)})_{max}$ is the maximum value of the NCL30088 startup consumption (30 μA)
- $t_{startup}$ is the targeted startup time

In our case, assuming a 19-nC gate charge MOSFET, a 65-kHz operation and a 0.5-s target for the startup time, it comes: (Eq. 50 and Eq. 51)

$$t_{reg} \cong \frac{C_{out}}{I_{out}}\left((V_{CC(off)})_{max}\frac{n_s}{n_{aux}}\right) = \frac{470\ \mu F}{500\ mA}(9.4 \cdot 1) \cong 9\ ms \quad \text{(eq. 50)}$$

$$C_{Vcc} \geq \frac{(I_{CC2} + Q_g f_{sw})t_{reg}}{(V_{CC(HYS)})_{min}} \cong \frac{(4m + 19n\ 65k)9m}{8} \cong 6\ \mu F \quad \text{(eq. 51)}$$

We will select a 10 μF/35 V capacitor. Hence:

$$I_{startup} = \frac{(V_{CC(on)})_{max}\, C_{Vcc}}{t_{startup}} + (I_{CC(start)})_{max} \cong \frac{20 \cdot 10\mu}{0.5} + 30\mu = 430\ \mu A \geq 75\ \mu A \quad \text{(eq. 52)}$$

Startup Resistor Calculation

Bulk Connection

For start-up time, the bulk rail sees the line peak voltage (the input voltage becomes a rectified sinusoid when the LED driver starts to operate), the following formula gives the $R_{startup}$ value:

$$R_{startup} = \frac{\sqrt{2} \cdot (V_{in,rms})_{LL}}{I_{startup}} \quad \text{(eq. 53)}$$

Where:

- $I_{startup}$ is the startup current
- $(V_{in,rms})_{LL}$ is the lowest line rms voltage

The maximum power dissipated by the startup resistor connected to the bulk rail is:

$$P_{startup} = \frac{\left(\sqrt{2} \cdot (V_{in,rms})_{HL} - V_{CC}\right)^2}{R_{startup}} \leq \frac{2 \cdot (V_{in,rms})_{HL}^{\ 2}}{R_{startup}} \quad \text{(eq. 54)}$$

Where $(V_{in,rms})_{HL}$ is the highest line rms voltage.

Half-wave Connection

If the resistor is connected to the half-wave:

$$R_{startup1/2} = \frac{\frac{\sqrt{2} \cdot (V_{in,rms})_{LL}}{\pi}}{I_{Cvcc} + I_{CC(start)}} = \frac{R_{startup}}{\pi} \quad \text{(eq. 55)}$$

The maximum power dissipated by the startup resistor connected to the half-wave is thus:

$$P_{startup1/2} = \frac{\left(\frac{\sqrt{2} \cdot (V_{in,rms})_{HL}}{\pi} - V_{CC}\right)^2}{R_{startup1/2}} \leq \frac{2}{\pi^2}\frac{(V_{in,rms})_{HL}^{\ 2}}{\frac{R_{startup}}{\pi}} = \frac{2}{\pi}\frac{(V_{in,rms})_{HL}^{\ 2}}{R_{startup}} \quad \text{(eq. 56)}$$

In Our Application:

We selected the half-wave configuration. Since we have computed that the startup current had to be 430 μA or more, we can deduce:

$$R_{startup1/2} = \frac{\frac{(V_{in,rms})_{LL}\sqrt{2}}{\pi}}{I_{startup}} = \frac{\frac{90\sqrt{2}}{\pi}}{430\mu} \cong 94\ k\Omega \quad \text{(eq. 57)}$$

The power dissipated for the startup resistor at maximum input voltage is:

$$P_{startup1/2} \leq \frac{\left(\frac{(V_{in,rms})_{HL}\sqrt{2}}{\pi}\right)^2}{R_{startup1/2}} = \frac{\left(\frac{265\sqrt{2}}{\pi}\right)^2}{94}k \cong 151\ mW \quad \text{(eq. 58)}$$

Three 33-kΩ, 1/4 W resistors are placed in series.

ZCD Network

R_{ZCD1} of Figure 2 limits:

- The current injected into the ZCD pin during the demagnetization time. As indicated in the data sheet, this current must remain below 5 mA.
- The current extracted from the ZCD pin during the on-time. This current must not exceed 2 mA.

During the on-time, the ZCD pin current is maximal at the highest line voltage:

$$I_{ZCD,on} = \frac{n_{aux}}{n_P} \frac{\sqrt{2} \cdot (V_{in,rms})_{HL}}{R_{ZCD1}} \leq 2mA \quad \text{(eq. 59)}$$

During the demagnetization time, the auxiliary winding voltage is maximal when V_{CC} is at its maximum value, that is, the OVP level. Hence:

$$I_{ZCD,dmg} = \frac{V_{CC(OVP)max} + V_f}{R_{ZCD1}} \leq 5mA \quad \text{(eq. 60)}$$

Where $V_{CC(OVP)max}$ is the V_{CC} maximum value for V_{CC} OVP protection tripping (28.5 V).

For optimal output current regulation, it is recommended to keep the ZCD pin voltage below 5 V. This is the goal of R_{ZCD2} of Figure 2.

$$\frac{R_{ZCD2}\,(V_{CC,max} + V_f)}{R_{ZCD1} + R_{ZCD2}} \leq 5V \quad \text{(eq. 61)}$$

Where $V_{CC,max}$ is the maximal V_{CC} voltage in normal operation (20 V in our application).

Finally, this resistor together with the C_{ZCD} capacitor delays the zero-voltage crossing event and helps to tune the turn-on instant when the drain voltage is in the valley.

Finally: (see Table 4)

Table 4.

C_{VCC}	$R_{startup1/2}$	$R_{startup}$	D_{AUX}	R_{ZCD1} / R_{ZCD2}	C_{ZCD}
10 μF / 35 V	three 33 kΩ, 1/4 W resistors in series	N/A	BAV21	33 kΩ / 10 kΩ	22 pF

DETAILED SCHEMATIC FOR OUR 10 W, UNIVERSAL MAINS LED DRIVER

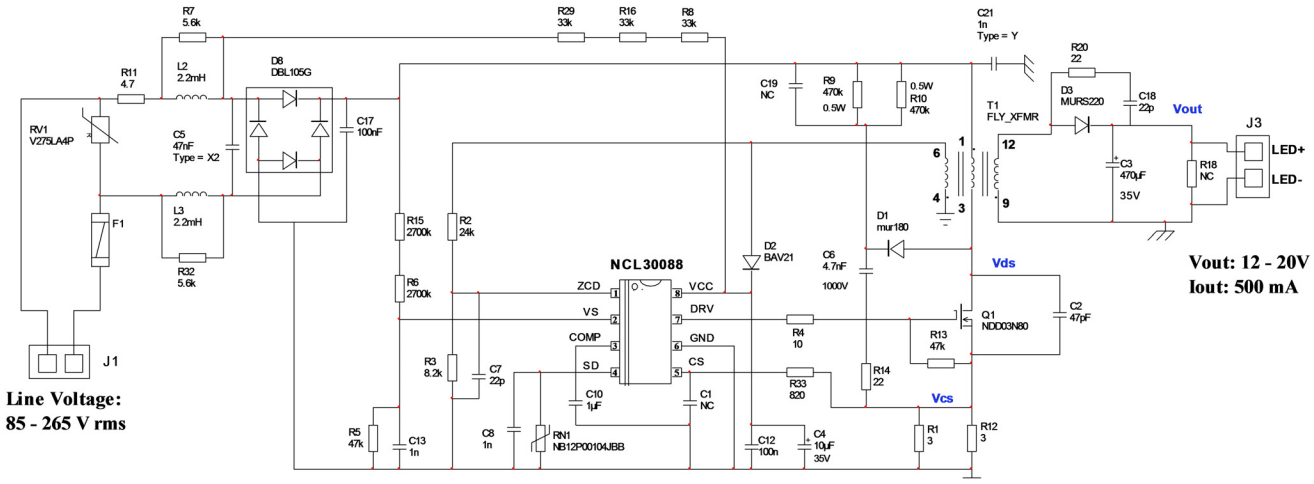

Figure 9. Application Schematic

EXPERIMENTAL DATA

Output Current Regulation

Figure 10 shows the output current as a percentage of its nominal value. We can see that its characteristic is very flat with respect to the temperature.

Thermal Foldback starts at about 80°C. As a result, the output current linearly decays to reach 50% of its nominal value at nearly 92°C. The circuit stops operating (SD pin Over Temperature Protection) at approximately 105°C and resumes operation when the temperature drops down to about 90°C. These temperature thresholds depend on the thermistor connected to the SD pin. Below characteristics were obtained with a NB12P00104JBB thermistor manufactured by AVX.

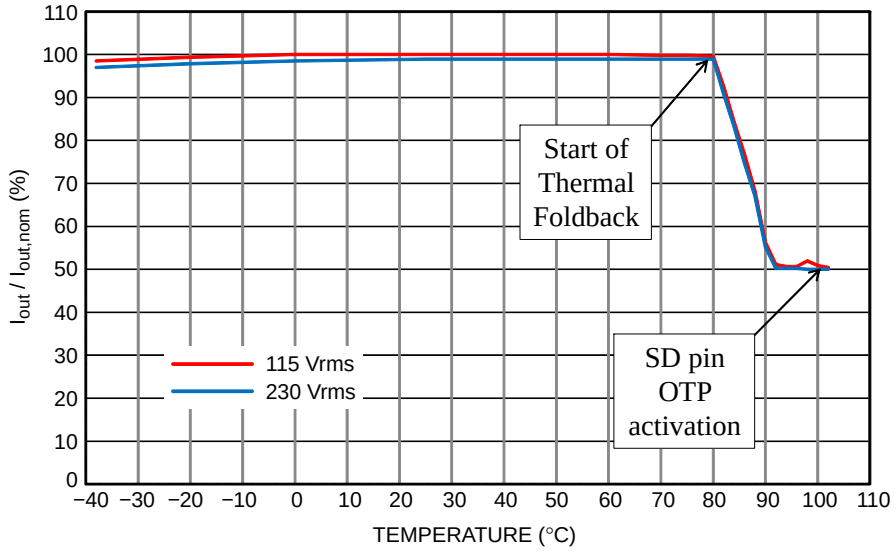

Figure 10. LED Current Characteristics over the Temperature Range

Power Factor

Figure 11 shows the power factor measured at two different line magnitudes (115 V rms and 230 V rms). The power factor is extremely stable over the considered temperature range from −40°C to 80°C. Above 80°C, the performance is affected by the thermal foldback which reduces the output current.

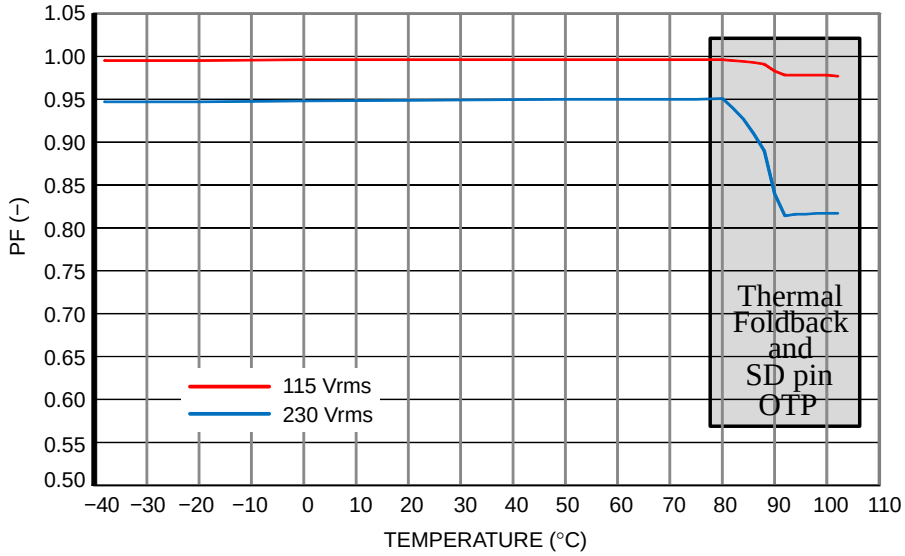

Figure 11. Power Factor Performance over the Temperature Range

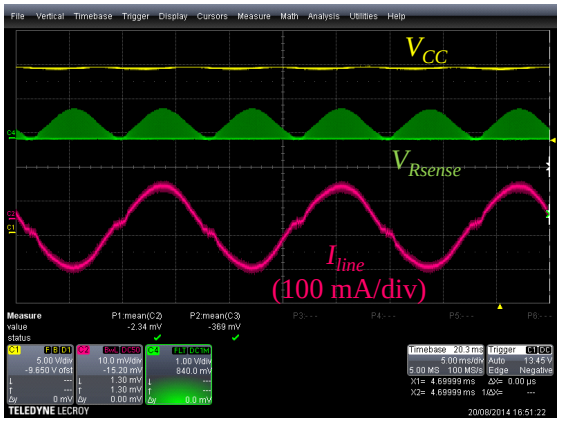

Figure 12. Current Waveform at 115 V rms

Fault Situations

The NCL30088 incorporates a large suite of protections. Next figures illustrate the circuit capability to address shorted/open situations of the LED string or an output diode failure. Tests have been made with the B version (NCL30088B). Application note AND9204/D discusses in details the NCL30088 behavior under safety tests [4].

Open LED String Situation

The LED string being disconnected, the V_{CC} voltage rises and the $V_{CC(OVP)}$ protection trips when V_{CC} exceeds 26.8 V (typically). At that moment, the circuit stops operating for the 4-s auto-recovery delay. The LED driver recovers normal operation when the LEDs are again connected.

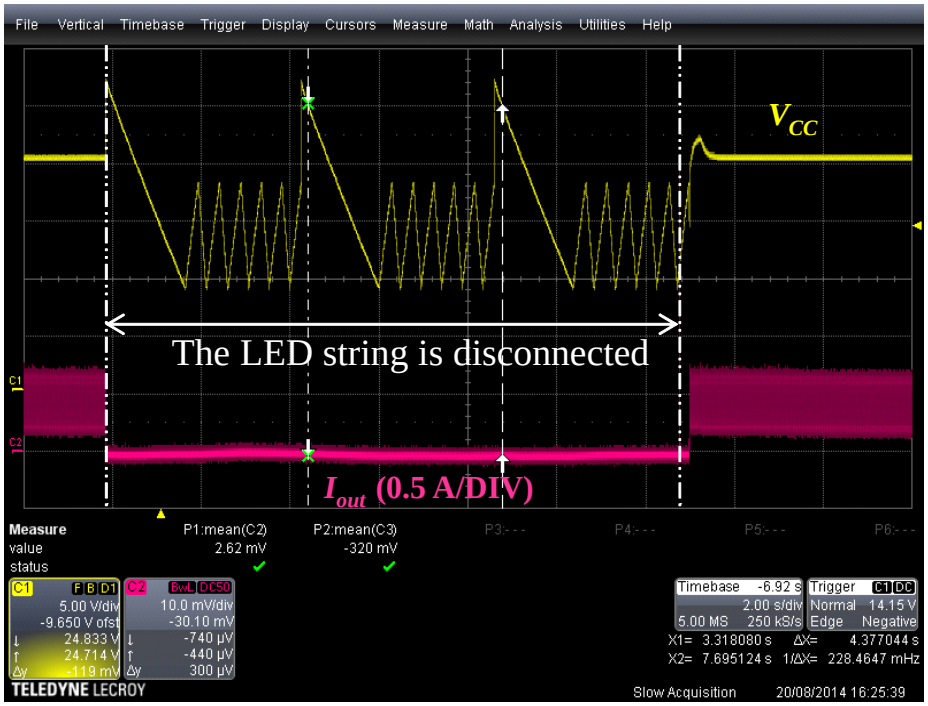

Figure 13. The System Enters a Safe Low Duty-ratio Burst Mode when the LED String is Disconnected (the LED Driver is Unloaded for about 15 s for this Test)

In the case of Figure 13, the only $V_{CC(OVP)}$ protection is in play. Note that a Zener diode could have been placed between the V_{CC} and SD pins to select a lower V_{CC} threshold for fault detection (see the SD pin OVP function in the NCL30088 data sheet). Further note that if the $V_{CC(OVP)}$ protection is auto-recovery in all NCL30088 versions, the SD pin OVP can be a latching-off (NCL30088A or NCL30088C) or an auto-recovery (NCL30088B or NCL30088D) protection.

LED String Short Situation

As illustrated by Figure 14, if the output is shorted, the AUX_SCP protection makes the LED driver enters a safe, low duty-ratio burst mode. Normal operation is recovered when the short is removed. The same behavior would be obtained with the D version. Note that the NCL30088A and NCL30088C latch off when an output short is detected. No recovery is hence possible with these versions until the LED driver is unplugged and V_{CC} drops below $V_{CC(reset)}$. At that moment, the fault is cleared and the circuit can resume operation.

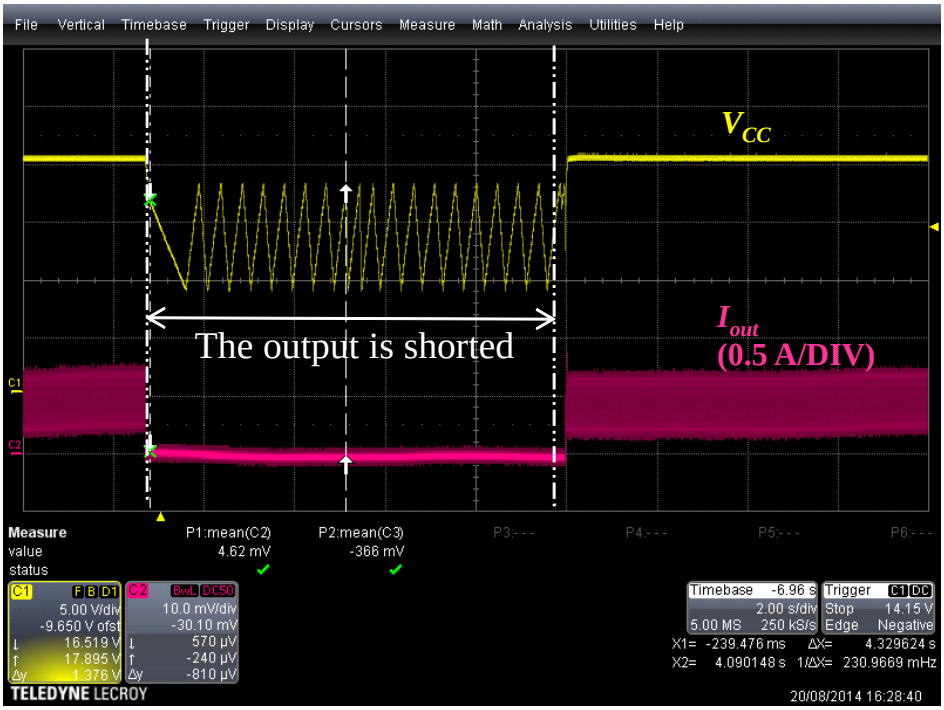

Figure 14. The System Enters a Safe Low Duty-ratio Burst Mode when the Output is Shorted (the LED Driver Output is Shorted for about 10 s for this Test)

Output Diode Short

The LED driver stops operation as soon as 4 faulty DRV pulses are detected (see Figure 16). In this situation, the NCL30088B and NCL30088D attempt to resume operation when the 4-s auto-recovery delay is elapsed. The NCL30088A and NCL30088C remain latched off until the system is reset.

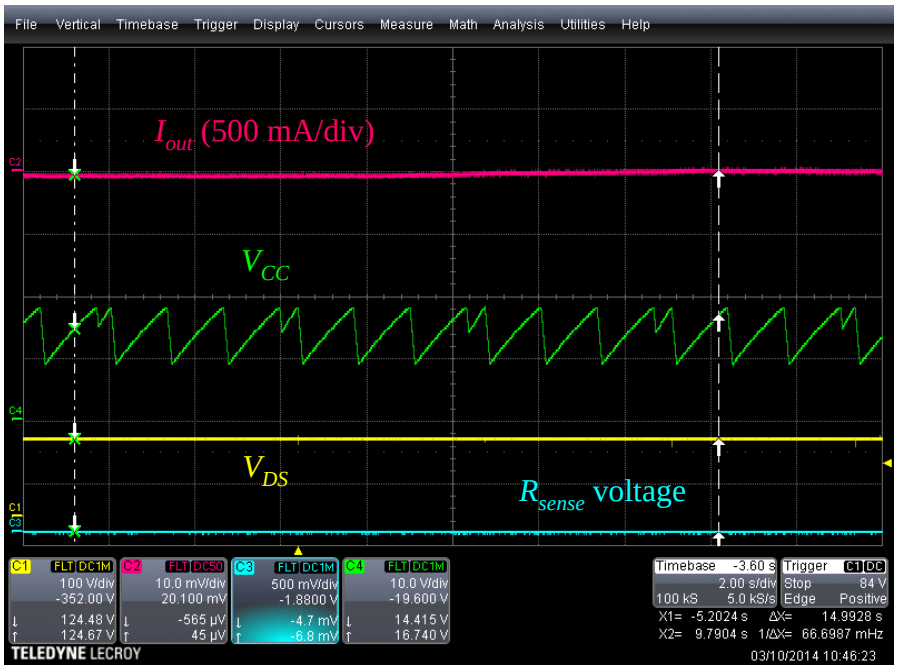

Figure 15. NCL30088B Operation when the Output Diode is Shorted

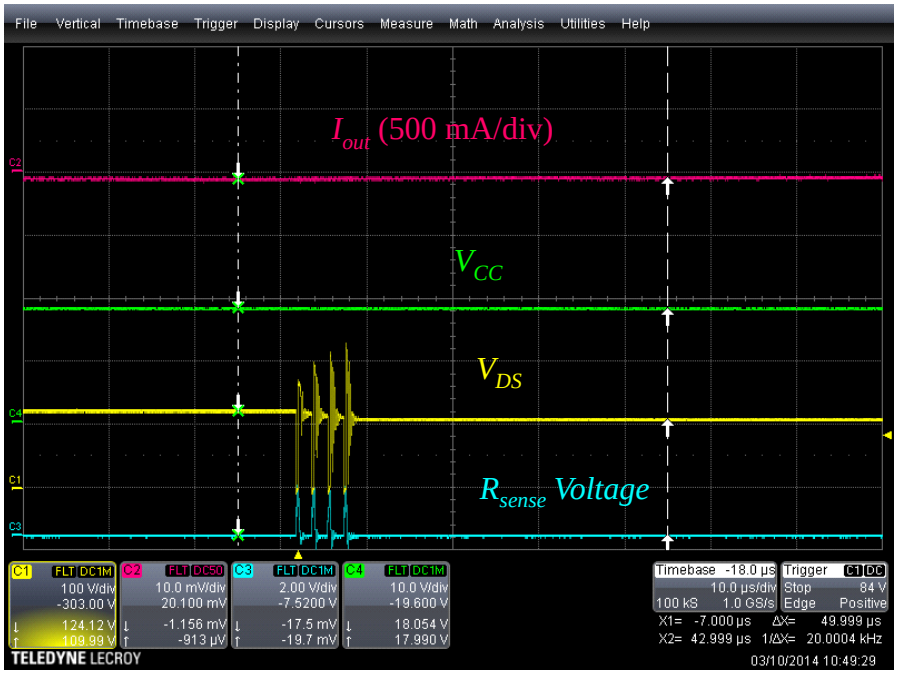

Figure 16. The Winding or Output Diode Short Circuit Protection (WODSCP) Trips as soon as 4 Consecutive Faulty DRV Pulses are Detected

REFERENCES

[1] NCL30088 Data Sheet, http://www.onsemi.com/pub_link/Collateral/NCL30088−D.PDF

[2] Stéphanie Cannenterre, Application Note AND9131/D, Designing a LED Driver with the NCL30080/81/82/83, http://www.onsemi.com/pub_link/Collateral/AND9131−D.PDF

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[4] Joel Turchi, “NCL30088 and NCL30085 Safety Tests Consideration”, Application Note http://www.onsemi.com/pub_link/Collateral/AND9204−D.PDF

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