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Phase Noise and Additive Phase Jitter Analysis Using the NB3V8312C

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APPLICATION NOTE

Creating and distributing clock signals are the heartbeat of digital systems.

Today's high−end systems demand extremely low noise clock signal integrity.

Jitter, and more recently, phase noise, are the most significant parameters when considering clock distribution timing budgets.

Jitter is a time domain parameter while phase noise is its frequency domain equivalent.

There are several technical jitter definitions and terms to introduce before we understand Additive Phase Jitter.

- Jitter − Jitter is the short−term frequency instability and is normally seen in the time domain on an oscilloscope.
- Phase Noise − Phase Noise is a ratio of signal power to noise power normalized to a 1 Hz bandwidth at a given offset from the carrier signal and is measured in the frequency domain on a phase noise analyzer. It is typically expressed as Single Side Band (SSB).
- Phase Jitter − Phase Jitter measures the amount of energy present in the specified frequency offsets from the carrier signal compared to the energy of the carrier signal by integrating the area under the phase noise plot.
- Noise Floor − Noise Floor is the noise level below which signals cannot be detected under the same measurement conditions. If an ideal clock is connected to the input of a buffer, the output phase noise of the buffer device is subtracted by the phase noise of the input clock signal. The generated phase noise of the buffer is also its noise floor.

  Noise floor is considered to be the lowest point of the plot.

  A buffer's Noise Floor can also be calculated from its phase noise measurement when a clean signal generator is the input source; see below.
- Additive Phase Jitter − Additive Phase Jitter is the amount of jitter caused by the device and is added to the input signal's phase jitter. In other words, it is the jitter contributed by the device. As will be demonstrated in this report, this value is highly dependent on the phase jitter of the input source. (Important Concept!)

To reiterate, Additive Phase Jitter of the device is an addition to the input signal noise, and is integrated under the Single Side Band (SSB). As an example, SONET uses a frequency offset of 12 kHz to 20 MHz from the carrier signal to integrate the area under the phase noise plot to measure phase jitter.

Introduction

The NB3V8312C is an ON Semiconductor high performance, low skew LVCMOS fanout buffer which can distribute 12 ultra−low jitter clocks from an LVCMOS/LVTTL input up to 250 MHz. (http://www.onsemi.com/pub/Collateral/NB3V8312C−D.PDF)

The core power supply (VDD) can be set to 3.3 V, 2.5 V or 1.8 V and the output power supply (VDDO) can be set to 3.3 V, 2.5 V, 1.8 V or 1.5 V; VDD ≥ VDDO.

The NB3V8312C will be characterized in this lab experiment to demonstrate how the equipment used to take the phase noise measurements can either expose or hide the actual additive phase jitter of the device, and to caution the knowledgeable system engineer when comparing datasheet specifications.

Lab Test Setup

A typical lab test setup for taking Phase Noise and Additive Phase Jitter measurements on an ON Semiconductor High−Performance Buffer product is illustrated in the block diagram in Figure 1.

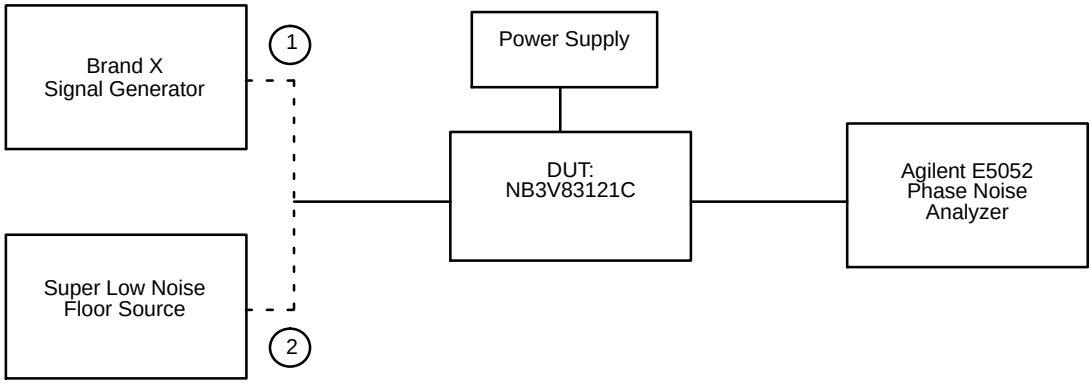

Figure 1. Basic Lab Setup for Phase Noise and Additive Phase Jitter

Additive Phase Jitter is examined using an input clock source with 50% duty cycle at a specified frequency and assumes that the noise processes are random and the input noise is not correlated to the output noise.

Two different input clock sources were used, one generic and one with very low noise.

The purpose of these sources is to contrast the:

1. types of additive phase jitter measurements one would obtain
2. degree of difference between additive phase jitter measurements

Enclosed are phase noise plots of the input / reference clock source and the device output along with a summary of the additive phase jitter and noise−floor measurements made.

These phase noise plots are superimposed so as to illustrate the noise floor of the source with respect to the noise floor of the device under test, DUT.

ADDITIVE PHASE JITTER LAB MEASUREMENT

In order to measure device performance it is important to select adequate equipment. Equipment selected needs to reflect requirements for edge dynamics and signal transition and not only output frequency.

Lab Equipment Used

Phase Noise Measurement − Agilent E5052A (offset up to 40 MHz)

DC Power Supply − Agilent 6624A

Matched high frequency cables − 26.5 GHz

How is **Additive Phase Jitter** measured?

Using the Agilent E5052A phase noise analyzer, phase noise is translated to the time domain by integrating the area under the curve using a filter. An example of an integration range for SONET is 12 kHz to 20 MHz.

Figures 2, 4 and 6 show phase−noise plots of the NB3V8312C superimposed with the generic 100 MHz Brand X input clock source.

Figures 3, 5 and 7 show the noise floor of the Brand X clock source, only.

Figures 8, 10 and 12 show phase−noise plots of the NB3V8312C superimposed with the super low noise input clock source.

Figures 9, 11 and 13 show the noise floor of the low noise source, only.

The stand alone phase noise plots of the clock sources captures the phase noise data of that source.

The DUT phase noise data is captured on the superimposed plots.

Input clock frequency is 100 MHz.

Power supply settings used in this experiment are:

1. $V_{DD} = V_{DDO} = 3.3$ V
2. $V_{DD} = V_{DDO} = 2.5$ V
3. $V_{DD} = V_{DDO} = 1.8$ V

PHASE NOISE AND INTEGRATED PHASE JITTER
$V_{DD} = V_{DDO} = 3.3$ V

NB3V8312C and Generator

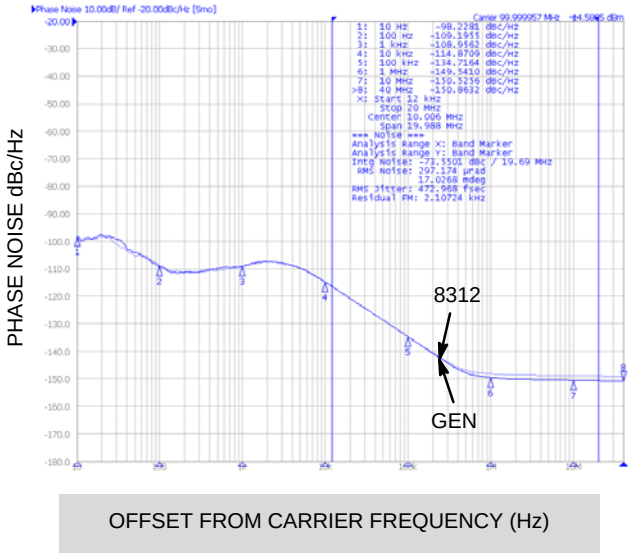

Figure 2.

Brand X Generator, Only

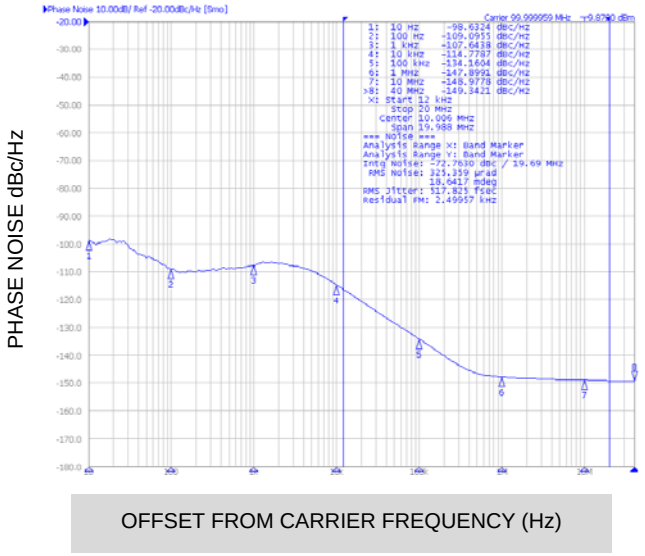

Figure 3.

For 100 MHz carrier, the NB3V8312C Additive Phase Noise (dBc/Hz) versus SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Lower Heavy Line) is 472.9 fs RMS. The Brand X Source Generator Additive Phase Noise (Upper Lighter Line) is 517.8 fs RMS.

PHASE NOISE AND INTEGRATED PHASE JITTER
$V_{DD} = V_{DDO} = 2.5$ V

NB3V8312C and Generator

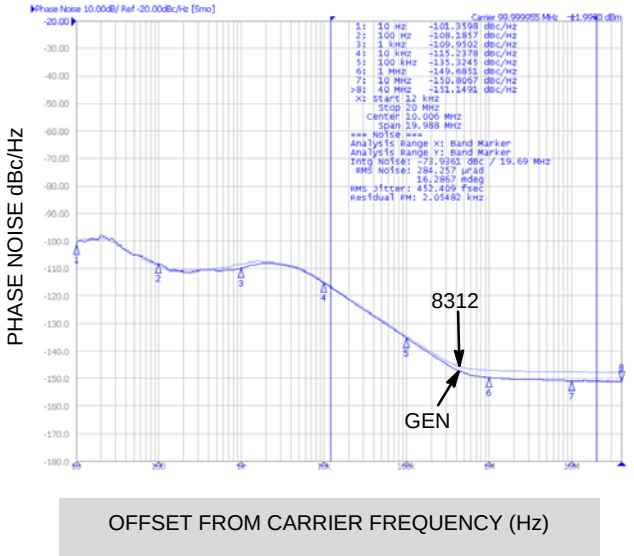

Figure 4.

Brand X Generator, Only

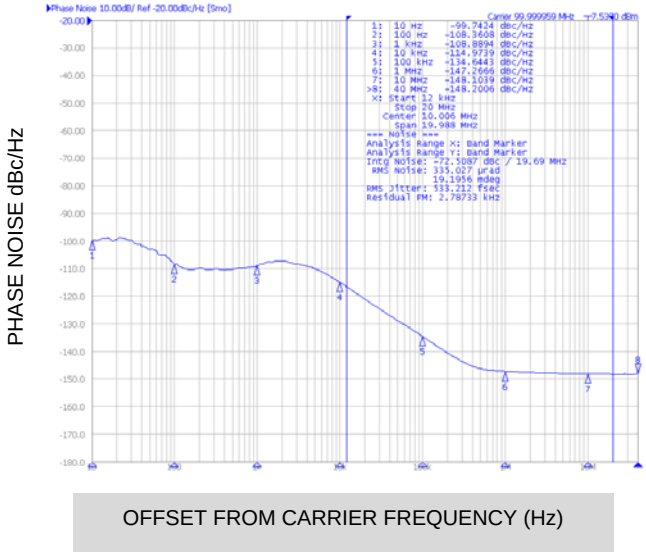

Figure 5.

For 100 MHz carrier, the NB3V8312C Additive Phase Noise (dBc/Hz) versus SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Lower Heavy Line) is 452.4 fs RMS. The Brand X Source Generator Additive Phase Noise (Upper Lighter Line) is 533.2 fs RMS.

PHASE NOISE AND INTEGRATED PHASE JITTER
$V_{DD} = V_{DDO} = 1.8$ V

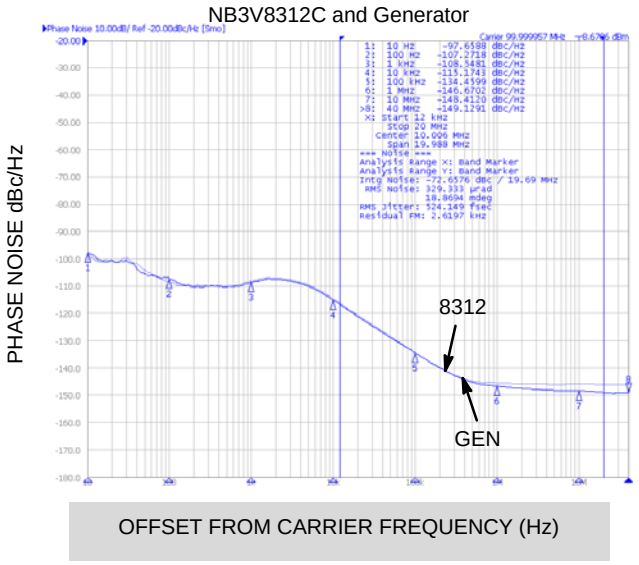

Figure 6.

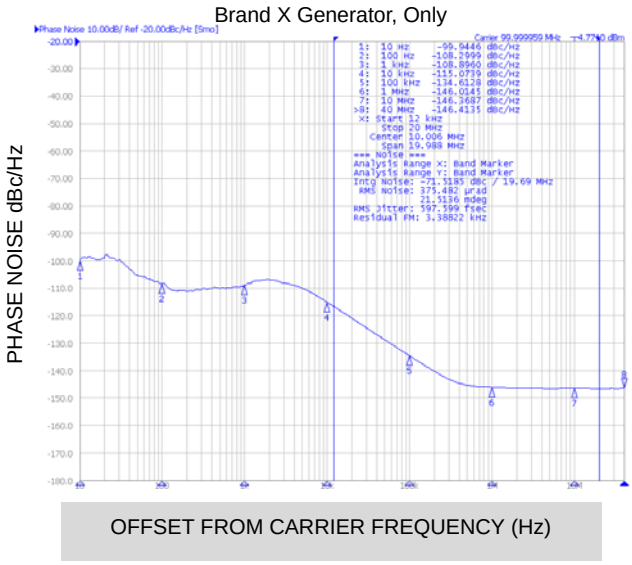

Figure 7.

For 100 MHz carrier, the NB3V8312C Additive Phase Noise (dBc/Hz) versus SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Lower Heavy Line) is 524.1 fs RMS. The Brand X Source Generator Additive Phase Noise (Upper Lighter Line) is 598.0 fs RMS.

Conclusion

Since the device output phase jitter is virtually the same as the input source phase jitter, and in this study exhibits slightly less than the input due to instrument measurement resolution, the additive phase jitter of the NB3V8312C is considered to be 0 fs. See Table 1.

PHASE NOISE AND INTEGRATED PHASE JITTER
$V_{DD} = V_{DDO} = 3.3$ V

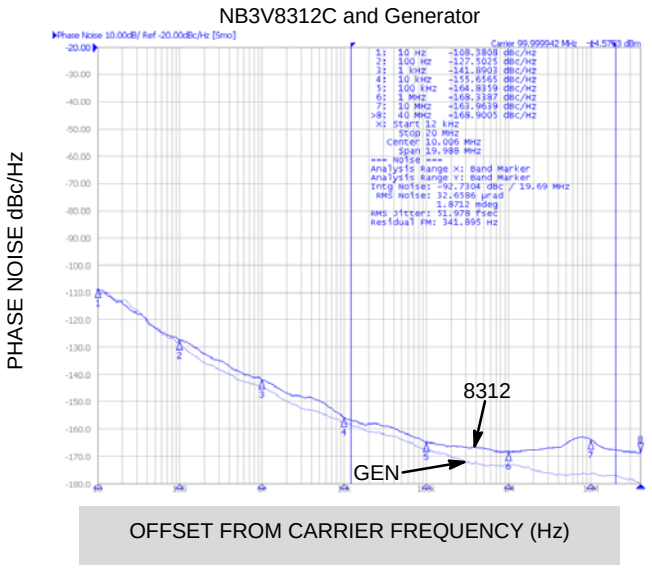

Figure 8.

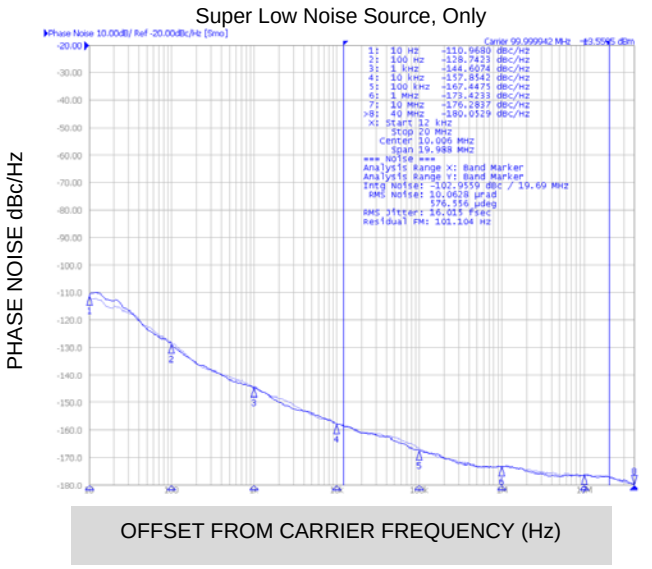

Figure 9.

For 100 MHz carrier, the NB3V8312C Additive Phase Noise (dBc/Hz) versus SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Upper Heavy Line) is 52.0 fs RMS. The Low Noise Source Generator Additive Phase Noise (Lower Lighter Line) is 16.0 fs RMS

PHASE NOISE AND INTEGRATED PHASE JITTER
$V_{DD} = V_{DDO} = 2.5$ V

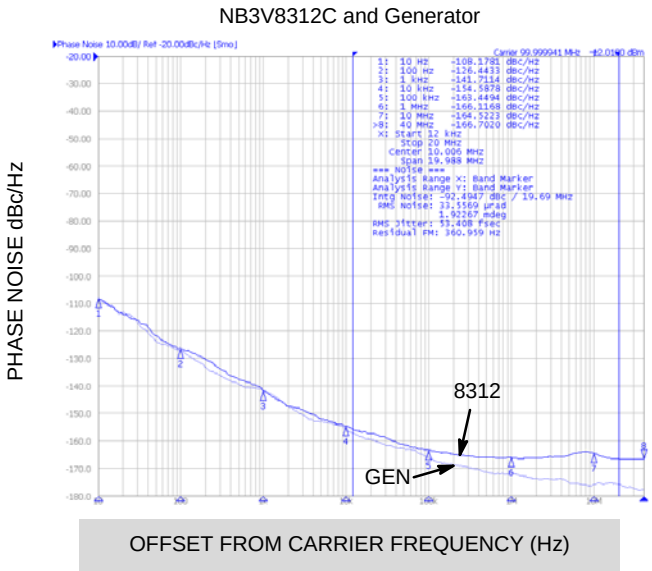

Figure 10.

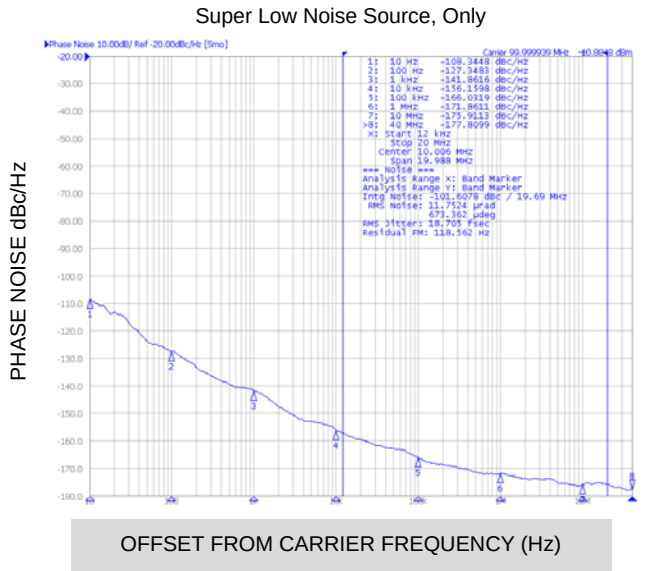

Figure 11.

For 100 MHz carrier, the NB3V8312C Additive Phase Noise (dBc/Hz) versus SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Upper Heavy Line) is 53.4 fs RMS. The Low Noise Source Generator Additive Phase Noise (Lower Lighter Line) is 18.7 fs RMS

PHASE NOISE AND INTEGRATED PHASE JITTER
$V_{DD} = V_{DDO} = 1.8$ V

NB3V8312C and Generator

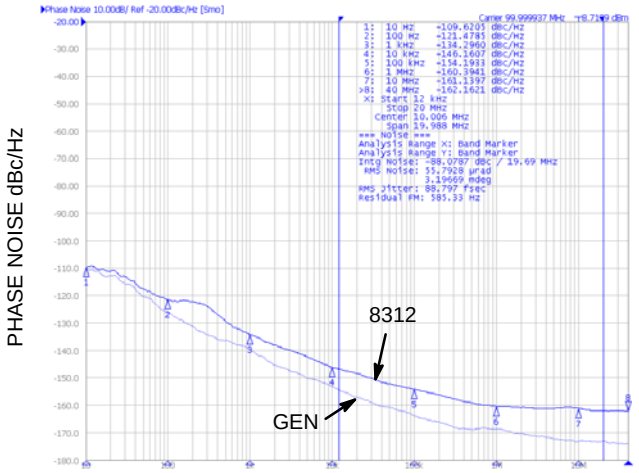

Figure 12.

Super Low Noise Soruce, Only

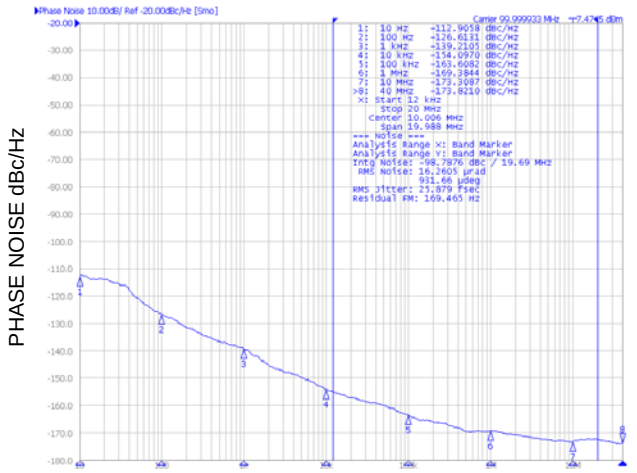

Figure 13.

For 100 MHz carrier, the NB3V8312C Additive Phase Noise (dBc/Hz) versus SSB Offset Frequency (Hz) Integrated Jitter from 12 kHz to 20 MHz (Upper Heavy Line) is 88.8 fs RMS. The Low Noise Source Generator Additive Phase Noise (Lower Lighter Line) is 25.9 fs RMS.

Conclusion

The true/actual device output phase jitter/noise floor is exposed with the super low noise floor source. See Table 2.

100 MHz ADDITIVE PHASE JITTER CALCULATIONS

(Integration Range = 12 kHz to 20 MHz)

Additive Phase Jitter can be derived by the following test method:

1. Measure the phase noise of the input clock source.
2. Then measure the phase noise of the device/buffer output.

With these individual phase noise measurements, calculating the additive phase noise of the device is accomplished using the following formula:

$$\text{RMS additive jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

The square root of the difference of the output phase noise squared and the input phase noise squared; typically referred to as RMS Random Clock Jitter.

This is the Additive Phase Jitter contributed by a buffer device with a particular input source.

If another input source were to be used, the additive phase jitter will vary.

$$\text{RMS additive jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$V_{DD} = V_{DDO} = 3.3$ V: $49.5\ \text{fs} = \sqrt{52.0\ \text{fs}^2 - 16.0\text{fs}^2}$

$V_{DD} = V_{DDO} = 2.5$ V: $50.0\ \text{fs} = \sqrt{53.4\ \text{fs}^2 - 18.7\text{fs}^2}$

$V_{DD} = V_{DDO} = 1.8$ V: $84.9\ \text{fs} = \sqrt{88.8\ \text{fs}^2 - 25.9\text{fs}^2}$

Table 1 lists the phase noise values of the NB3V8312C with Brand X source at different supply voltages.

Additive phase jitter results of the two clock sources.

Table 1. NB3V8312C WITH BRAND X SOURCE

VDD / VDDO Supply Range	NB3V8312C RMS Phase Jitter Output (fs)	Input Phase Jitter (fs)	RMS Additive Phase Jitter (fs) 12 kHz − 20 MHz
3.3 V / 3.3 V	473.0	517.8	0
2.5 V / 2.5 V	452.4	533.2	0
1.8 V / 1.8 V	524.1	597.6	0

Table 2 lists the phase noise values of the NB3V8312C with super low source at different supply voltages.

Table 2. NB3V8312C WITH SUPER LOW NOISE SOURCE

VDD / VDDO Supply Range	NB3V8312C RMS Phase Jitter Output (fs)	Input Phase Jitter (fs)	RMS Additive Phase Jitter (fs) 12 kHz − 20 MHz
3.3 V / 3.3 V	52.0	16.0	49.5
2.5 V / 2.5 V	53.4	18.7	50.0
1.8 V / 1.8 V	88.8	25.9	84.9

From Tables 1 and 2, the same device has two different additive phase jitter values depending on the input source. Therefore, **additive phase jitter is dependent on the input source**.

Table 3 lists the meaningful additive phase jitter capability of the NB3V8312C with a low noise source in a frequency range of 12 kHz to 20 MHz at fc = 100 MHz.

Table 3.

NB3V8312C	f_{offset} (Hz)								
VDD / VDDO Supply Range	10	100	1k	10k	100k	1M	10M	40M	RMS Additive Phase Jitter (fs) 12 kHz − 20 MHz
3.3 V / 3.3 V	−108.4	−127.5	−141.9	−155.6	−164.8	−168.3	−163.9	−168.9	49.5
2.5 V / 2.5 V	−108.2	−126.4	−141.7	−154.6	−163.4	−166.1	−164.5	−166.7	50.0
1.8 V / 1.8 V	−109.6	−121.5	−134.3	−146.2	−154.2	−160.4	−161.1	−162.2	84.9

Summary

First of all, this report demonstrates the exceptional low phase noise performance of the NB3V8312C of −160 dBc/Hz operating at various V_{DD}/V_{DDO} power supplies with a truly low noise input source.

The NB3V8312C overall additive phase jitter performance is approx. 50 fs RMS (typ), depending on power supply.

The quality of a Clock signal coming out of a high−performance fanout buffer device is evaluated and determined by its Additive Phase Jitter.

If the phase noise of the source is greater than the device under test output, then no additive phase jitter will be observed.

In a system where the input noise floor is > −160 dBc/Hz, such as using a Brand X input source in this study, the NB3V8312C will not contribute to the total integrated phase RMS noise jitter.

The closer the noise floor is to the DUT phase noise, the smaller the additive phase jitter is contributed by the DUT.

One would then conclude that meaningful additive phase jitter measurements must be taken with a clean input clock source that has a phase noise below the noise floor of the buffer/device itself in order for the device additive integrated phase jitter to be exposed.

The source needs to be at least 3 dB lower than the DUT in order to ensure that the source does not have an affect on the phase noise of the DUT. Any less than 3 dB of the separation and the source could mask the true phase noise performance of the DUT.

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