Universal Footprint for SO8FL Package

ON Semiconductor®

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APPLICATION NOTE

Introduction

In the past few years the need to increase power density in converter designs has made the DFN, QFN, and LFPAK packages very popular among designers of DC−DC converters. That trend was followed by every Power Semiconductor vendor and has created an interesting problem. Every vendor has come up with their own version on the industry standard 5×6 mm footprint, and although each package design meets the basic pin out requirements, each contains small variations that makes them incompatible and requires the creation for a Universal Footprint to assist the end users to accommodate more than one supplier in their designs.

Package Overview

The ON Semiconductor SO8FL package is a QFN package also known in the industry as the Power-SO8, it was created to allow a large die, basically as large as a DPAK, to fit into a standard SO8IC footprint. This package uses a lead frame design that allows the leads to stick out beyond the molded body size. This feature allows the customer to see the solder fillet during visual inspection. See Figure 1 below.

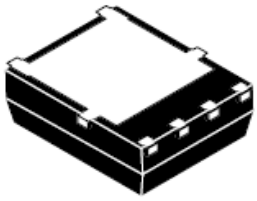


Figure 1. The Underside of an SO8FL Package

In the package the die is soldered to a large tab forming the electrical DRAIN connection and a low thermal resistance path to the PCB. A top-clip is soldered to the top of the die providing the SOURCE connection once the clip is attached to the lead frame to provide a low resistance, low inductance and also a low thermal resistance path to the PCB. At last the GATE is connected to the lead frame via a wire.

Many vendors have their own realization for this package, the common part is the attachment of the silicon die to a tab to create the DRAIN connection, then the SOURCE and GATE connections are made with Aluminum wire-bonding, Copper ribbon bonding, Copper clips and Gold bumping, Copper wire bonding, Copper clip and wire bond. Figure 2 has some examples of these connections.

An interesting variation is the LFPAK, in this package the silicon is soldered to the DRAIN tab forming the electrical DRAIN connection and a low thermal resistance path to the PCB. The top-clip is then soldered to the silicon die to provide SOURCE and GATE connections, eliminating the wires and reducing package resistance and inductance. The end result is a package that on one side looks like a standard SO8IC and the other side looks like a miniature DPAK. See Figure 2.

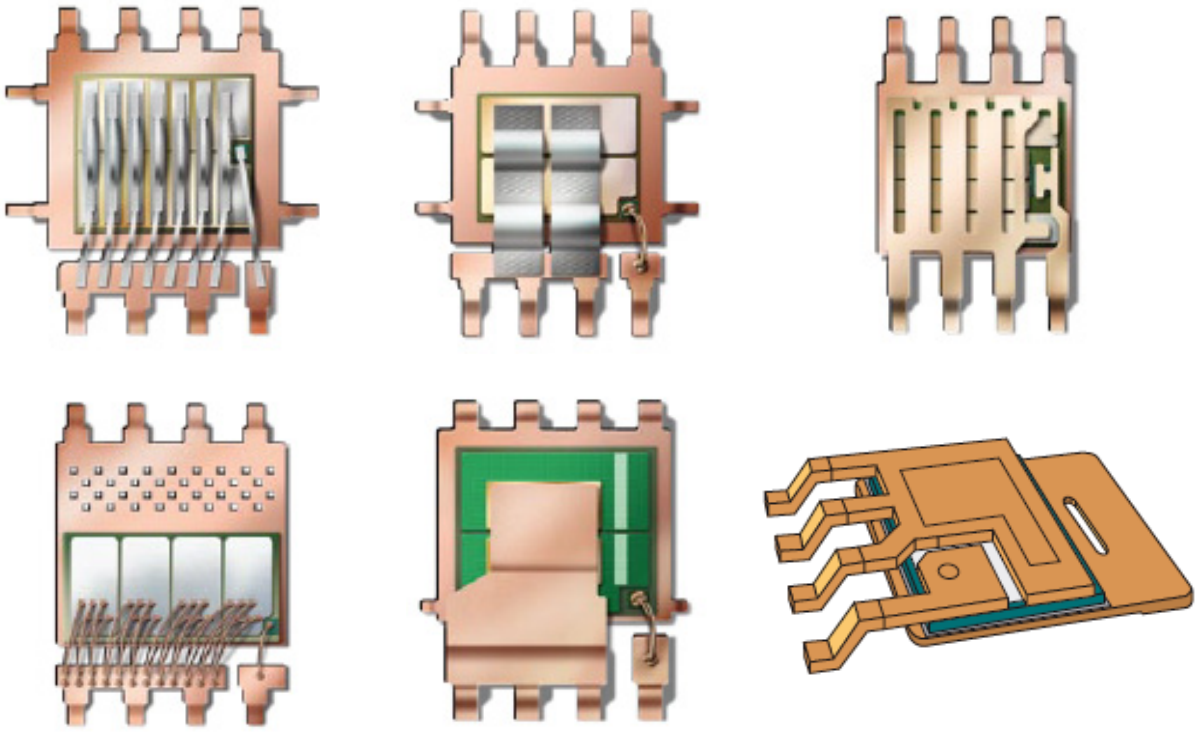


Figure 2. Al Wire, Ribbon & Wire, Cu Clip & Au Bump, Cu Wire, Cu Clip & Wire and LFPAK [1]

Below is a table listing some of the different names given to this package by different vendors.

Table 1. DIFFERENT VENDORS OFFERING THIS POWER PACKAGE WITH THEIR RESPECTIVE PACKAGE NAMES

Vishay	PowerPAK SO−8
International Rectifier	PQFN
Texas Instrument	SON 5 × 6 mm (Q5A)
Alpha and Omega	DFN 5 × 6
ST Microelectronics	PowerFLAT™ 5 × 6
Toshiba	SOP Advance
Infineon	Super SO8
NXP	LFPAK (SOT669)
Renesas	WPAK(3F) / LFPAK
Fairchild	Power 56
APEC	PMPAK 5 × 6
MagnaChip	PowerDFN56
ROHM	HSOP8
UBIQ	PRPAK56
NIKO−SEM	PDFN 5 × 6
NEC	8-pin HVSON

Soldering and Footprint Compatibility

There are many power MOSFET's available in the surface mounted power SO8 footprint. The following picture (Figure 3) shows the different package styles and each vendor has their recommended PCB footprint and each differs from each other. There is no generic JEDEC standard for Power-SO8 devices and therefore each vendor has its own "pad design". None of the manufacturers of all of these devices can guarantee with certainty that they can be interchangeable with the other devices, hence the need to come up with a footprint that will cover as many of these variations as possible.

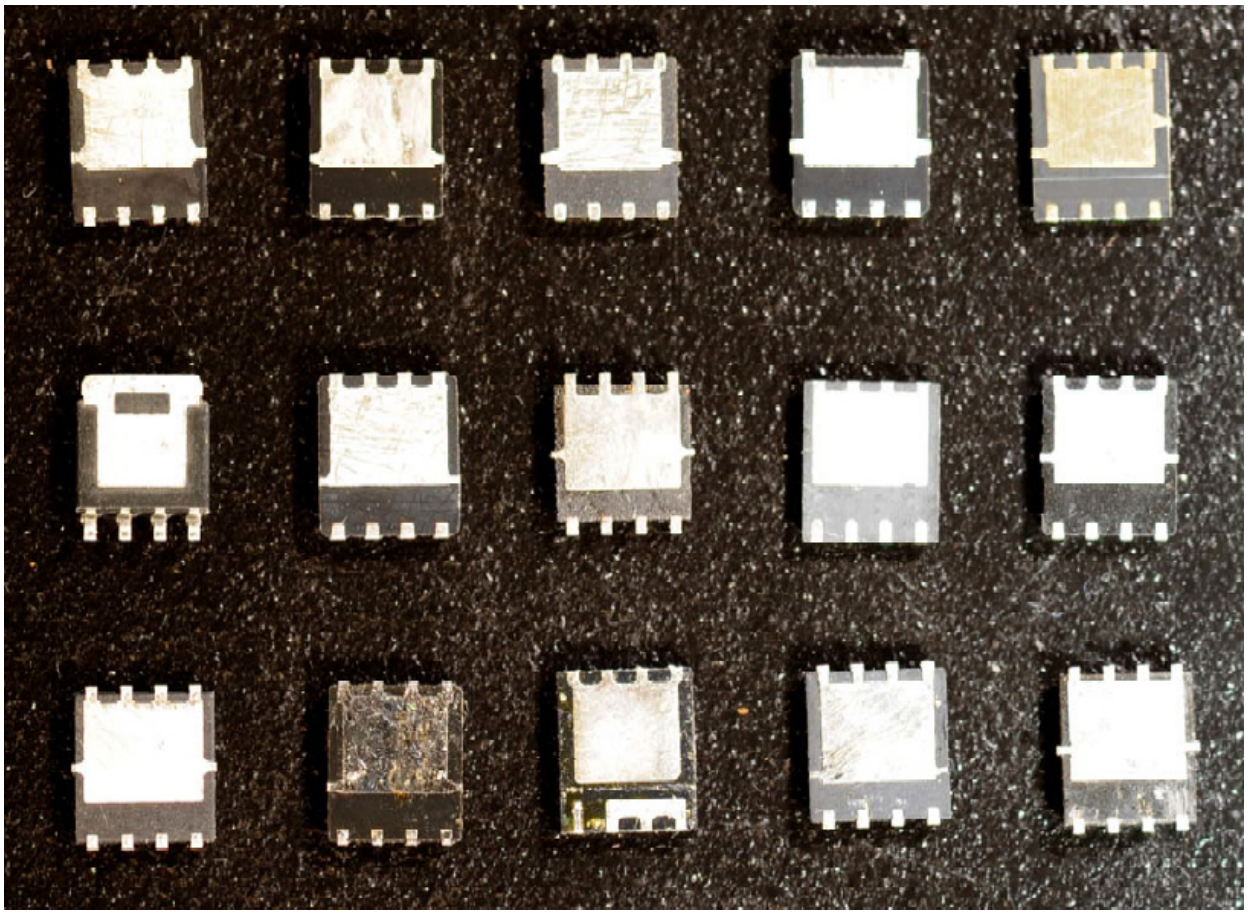


Figure 3. Several Power SO8 Package Styles Available on the Market

In an attempt to achieve footprint compatibility NXP designed the Universal Footprint [1]. This design was tested and evaluated in our packaging lab and it proved to be very good. During different evaluations, voids ranging from 6% to 22% were observed on certain packages and even in LFPAK. In order to improve these results a modification to the solder stencil was made in order to minimize voiding. The optimized solder stencil design proposed here (see Figure 4) reduced voids significantly and the results obtained provided voids ranging from 2% to 7%.

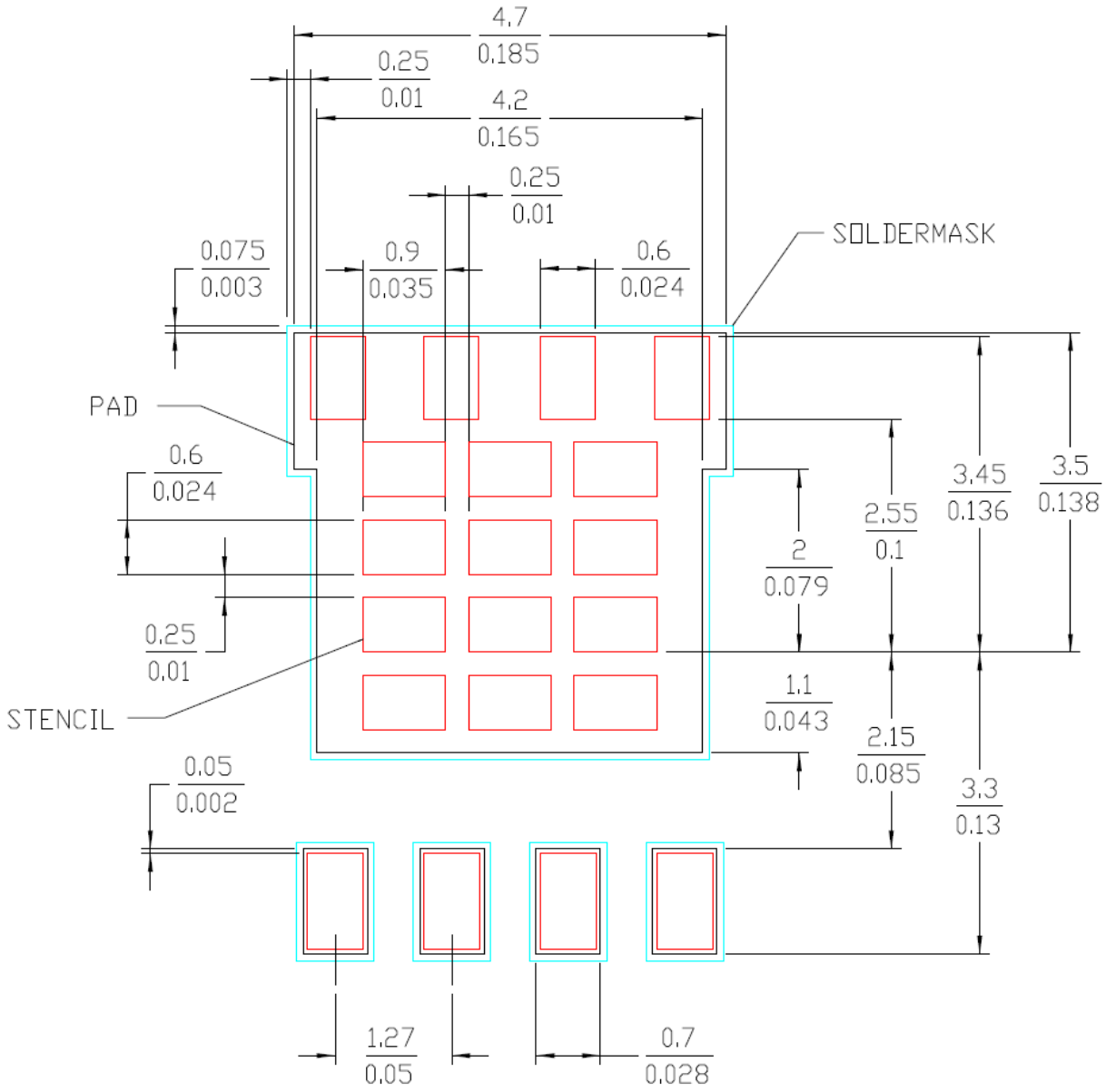
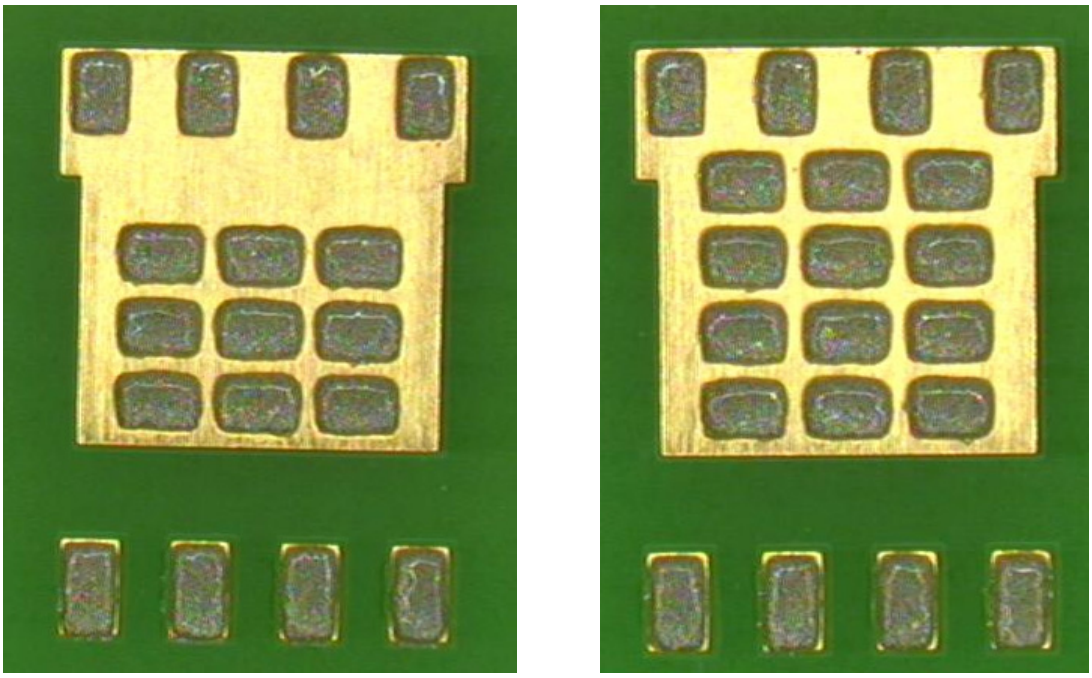


Figure 4. Universal Footprint Showing Solder Mask and Optimized Solder Stencil Details

Test Results

Using the Universal Footprint, an array of 8×4 devices per board was designed to accommodate several parts per board. Two different solder stencil patterns were evaluated and the recommended Universal Footprint with both solder paste designs is shown in Figure 5.



Original Solder Stencil Design

Optimized Solder Stencil Design

Figure 5. Universal Footprint with Solder Paste

After solder paste was applied parts placed using standard pick and place equipment. Boards were reflowed using Pb-Free solder profile. Optimized Stencil array is shown in Figure 6 below.

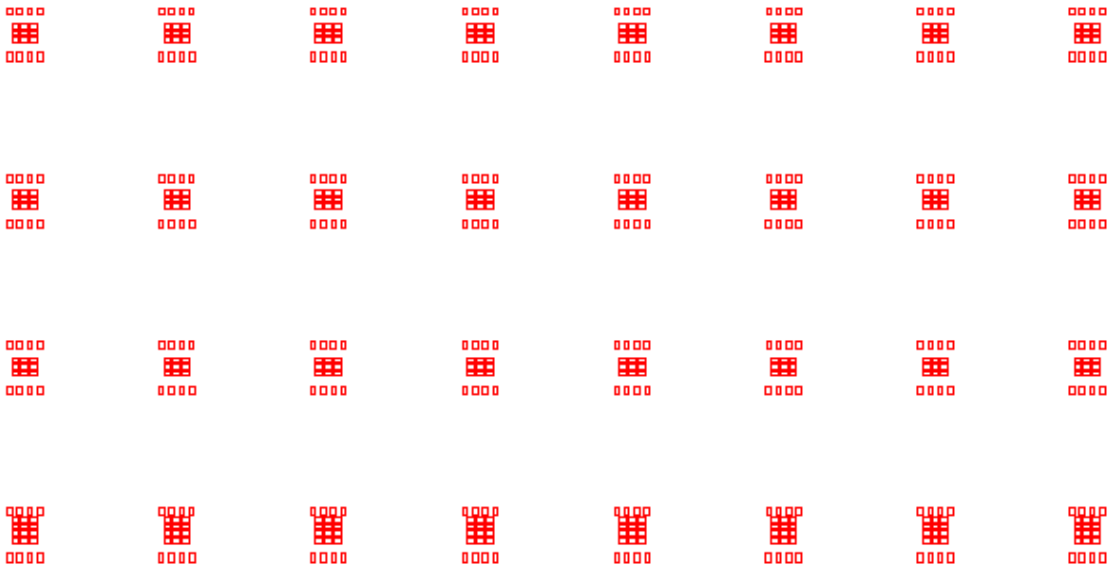


Figure 6. Universal Footprint Optimized Stencil Board Array

The results of the optimized stencil are shown in Figure 7.

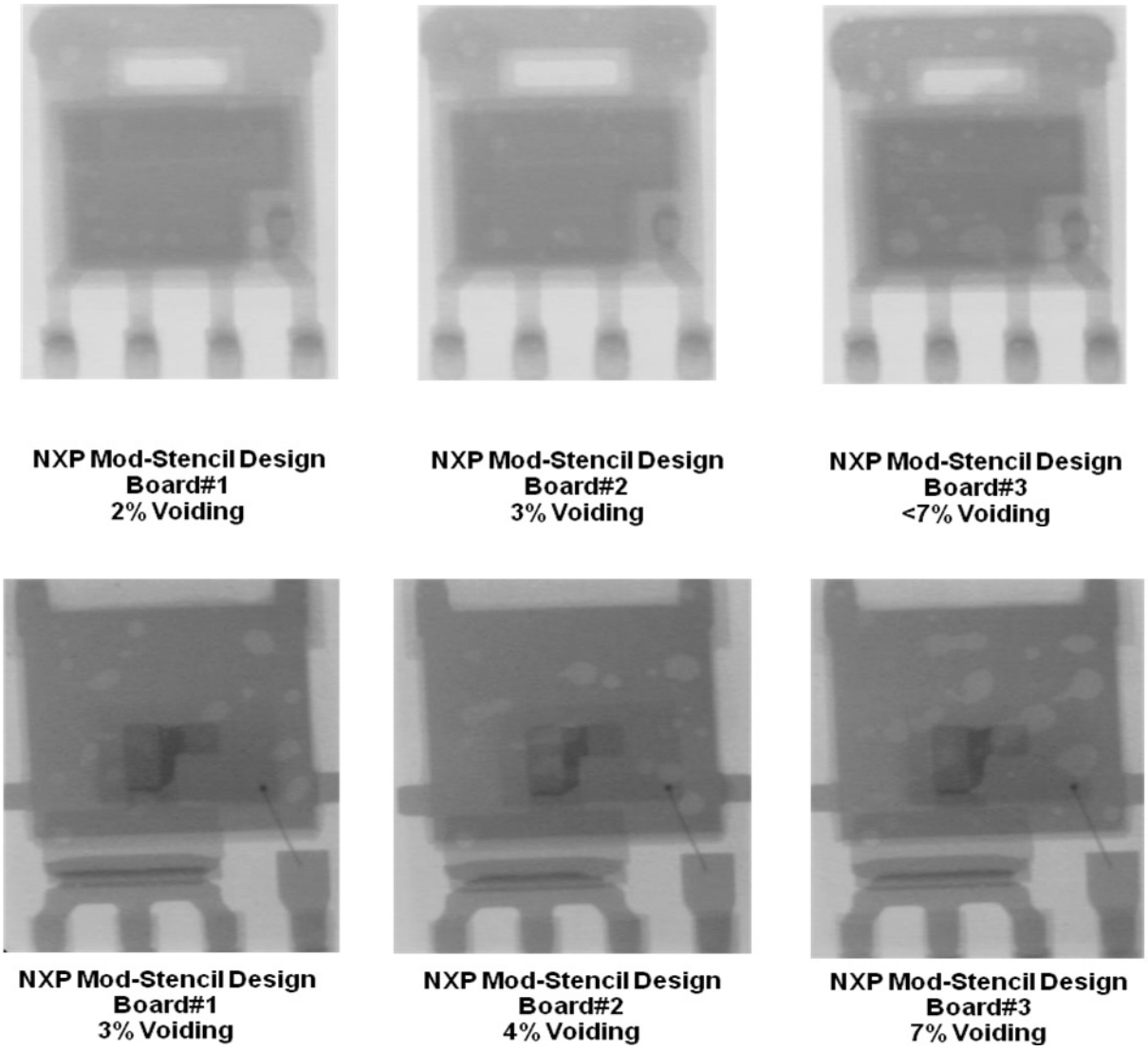


Figure 7. X-Ray Images Showing LFPAK and SO8FL Packages after Solder Reflow using Optimized Solder Stencil Pattern

Parts were cross sectioned to verify solder thickness uniformity and quality. Those results can be seen in Figures 8 and 9.

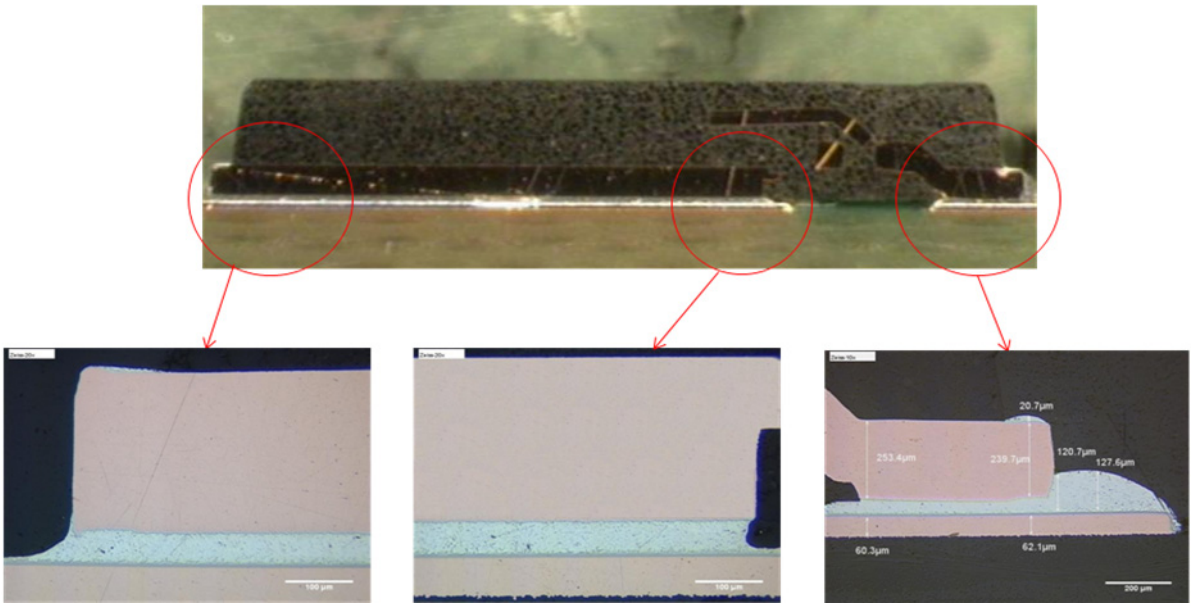


Figure 8. Cross Sections of Board Mount. Solder Thickness Variation across Package

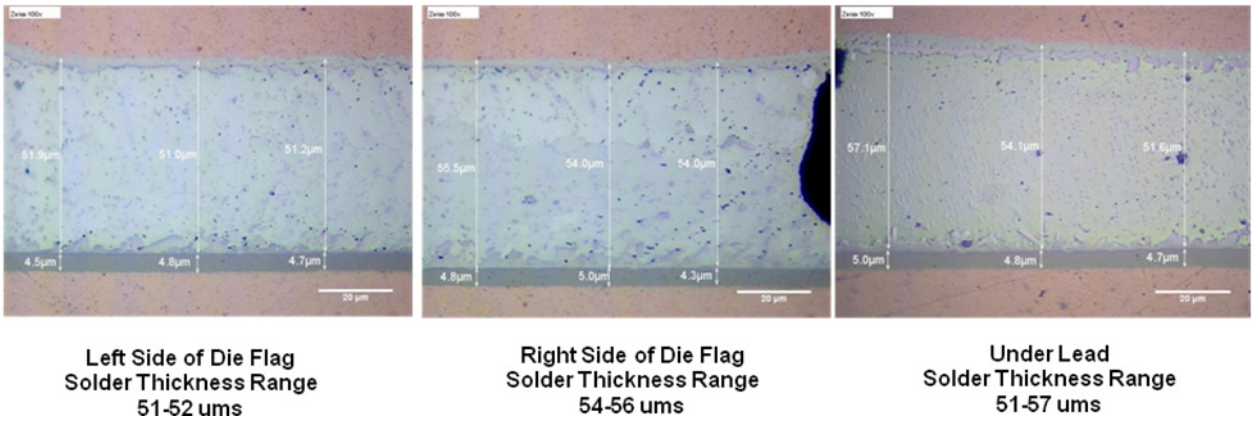


Figure 9. Detail on Solder Thickness Variation Across Package

Conclusion

The need for a footprint that can accommodate as many power SO8 versions as possible has been addressed by the creation of NXP's Universal Footprint. After evaluation of this footprint improvements to solder attach voiding were made by optimizing the solder stencil. The recommendations provided here need to be evaluated and characterized by the end user in their equipment. The exact profile will be determined by the Process Engineer based on the board density and thickness. These variations will require small changes in the profile in order to achieve an optimized process.

APPENDIX

Solder Type

Any standard lead free solder paste commonly used on the industry should work with this package. The IPC Solder Products Value Council has recommended the 96.5 Sn/3.0 Ag/0.5 Cu SAC alloy to be the lead free solder paste alloy of choice for the electronics industry. Solder paste such as Cookson Electronics P/N WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water soluble flux for cleaning. Cookson Electronics P/N C0106A can be used if a no-clean flux is preferred.

Solder Screening onto the PCB

Stencil screening the solder onto the PCB is commonly used in the industry. It is estimated that 60% of all assembly errors are due to paste printing. For a controlled, high yielding manufacturing process, it is one of the important steps of assembly. The recommended stencil thickness used is 0.127 mm (0.005 in) and the sidewalls of the stencil openings should be tapered approximately 5° along with an electro-polish finish to aid in the release of the paste when the stencil is removed from the PCB.

For a typical edge PCB terminal pad, the stencil opening should be the same size as the PCB mounting pad. However, in cases where the main device pad is soldered to the PCB, the stencil opening must be divided into a grid allowing channels for gases to vent as shown in Figure 10. Dividing the larger pad into smaller screen openings reduces the risk of solder voiding and allows the solder joints for smaller terminal pads to be at the same height as the larger ones.

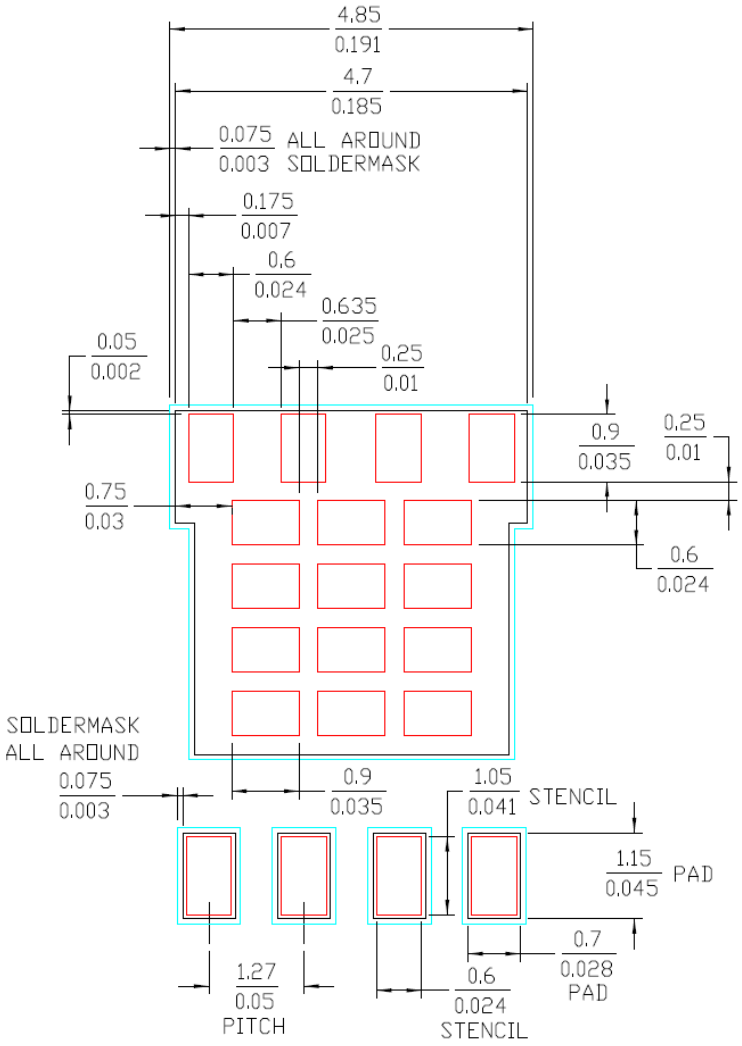


Figure 10. Solder Stencil Design Illustrating how Stencil Openings are Divided into an Array for Large Device Areas

Package Placement onto the PCB

Pick and place equipment with the standard tolerance of ±0.05 mm or better is recommended. The package will tend to center itself and correct for slight placement errors during reflow process due to surface tension of the solder.

Solder Reflow

Once the package is placed on the PCB along with the solder paste, a standard surface mount reflow process can be used to solder the part. Figures 11 is an example of standard reflow profiles for typical Lead-Free solder alloy.

The optimum reflow profile used for every product and oven is different. Even the same equipment in a different facility may require an adjustment in the profile. The proper ramp and soak rates are determined by the solder paste vendor for their specific products. Obtaining this information from the paste vendor is highly recommended since the chemistry and viscosity of the flux matrix will vary. The exact profile will be determined by the Process Engineer based on the board density and thickness. These variations will require small changes in the profile in order to achieve an optimized process.

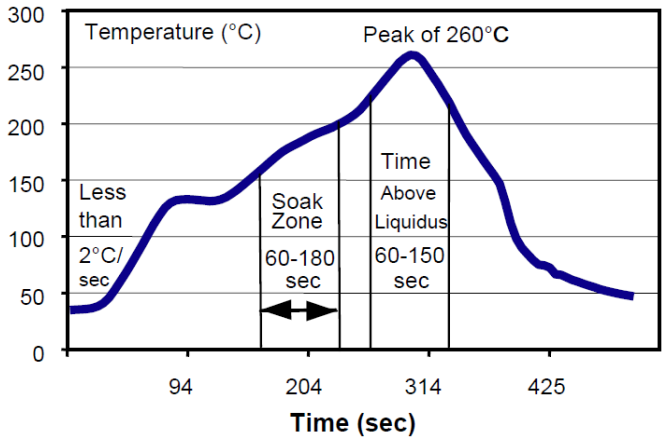


Figure 11. Typical Reflow Profile for Standard Pb-Free Solder

In general, the temperature of the part should not be raise more than 2°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last for 60 to 180 seconds for Pb-free profiles. Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquid state of the solder for 60 to 150 seconds for Pb-free depending on the mass of the board. The peak temperature of the profile should be between 245 and 260°C for Pb-free solder alloys.

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of X-Ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X-Ray inspection system. The solder joints should have enough solder volume with the proper stand-off height so that an “hour glass” shaped connection is not formed as shown in Figure 12. “Hour glass” solder joints are a reliability concern and must be avoided.

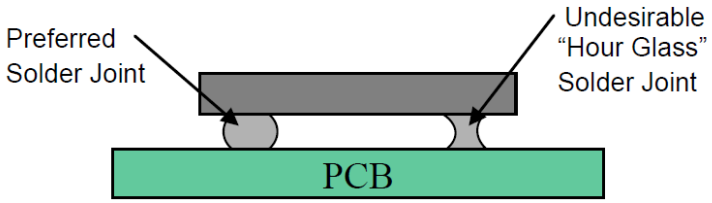


Figure 12. Side View of DFN 8 Attachment Illustrating Preferred and Undesirable Solder Joint Shapes

REFERENCES

[1] LFPAK The toughest Power SO8. NXP BV publication 2009 http://www.nxp.com/documents/reflow_soldering/sot669_fr.pdf

[2] AND8195/D Board Mounting Notes for SO8−Flat Lead. ON Semiconductor April 2007

[3] NXP Universal Footprint Evaluations done by Phil Celaya and Stephen StGermann. ON Semiconductor 8/2010 and 9/2010

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