AND9136/D

Board Mounting Notes for DFN8, 5 x 6 mm, Dual Flag (SO8FL Dual Asymmetrical)

ON Semiconductor®

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APPLICATION NOTE

INTRODUCTION

ON Semiconductor addressing the continuous market needs to increase power density is packaging several devices in an advanced power leadless package named Dual Flat No−Lead (DFN) package. The power DFN platform represents the latest in surface mount packaging technology. This technology has been increasingly used due to its low package height, excellent thermal performance, and small footprint.

In order to increase design flexibility, ON Semiconductor launched the dual asymmetrical product portfolio in industry standard SO8FL 5 x 6 mm package. This line of products co−packaged two devices, sized appropriately to be used in high current synchronous “buck” regulator circuits, saving board space and component count.

Due to its compact footprint, it is important that the design of the Printed Circuit Board (PCB) and the assembly process follow the suggested guidelines outlined in this document.

SO8FL Dual Asymmetrical Overview

The SO8FL Dual Asymmetrical package was created to allow two devices to fit into a standard SO8IC footprint that are also interconnected internally to form the power stage of a synchronous “buck” regulator. This package uses a lead frame design that allows the leads to stick out beyond the molded body size. This feature allows the customer to see the solder fillet during visual inspection. See Figure 1.

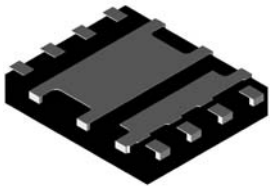


Figure 1. The Underside of a DFN8, 5 x 6 mm, Dual Flag (SO8FL Dual Asymmetrical)

This package features two devices internally connected using copper clips to maintain the package height under one millimeter by having both wire bond and clips on the same plane. When mounted, the lead and the body are directly attached to the board without a gap between the body and the board. These features provide excellent thermal dissipation and reduced electrical parasitic elements due to its efficient and compact design.

Figure 2 also illustrates how the ends of the leads go past the edge of the molded package. This configuration allows for the maximum die size within a given footprint, which in turn maximize the board space utilization. The dual package is sold in lead free finish.

Figure 2. X−Ray View and Pin Out of the Dual Asymmetrical Package

Printed Circuit Board Design Considerations

There are two different types of PCB pad configuration commonly used for surface mounted packages. These different pad defined configurations are:

1. Non−Solder Masked Defined (NSMD)
2. Solder Masked Defined (SMD)

As their names describe, the NSMD contact pads have the solder mask pulled away from the solderable metallization, in other words the pads are defined by the metal pattern exposed, while the SMD pads have the solder mask over the edge of the metallization, in other word the pads are solder mask defined openings as shown in Figure 3. With the SMD pads, the solder mask restricts the flow of solder paste to the top of the pad preventing the solder from flowing along the sides of the metal pad. This is different from the NSMD configuration where the solder will flow around both the top and the sides of the pad.

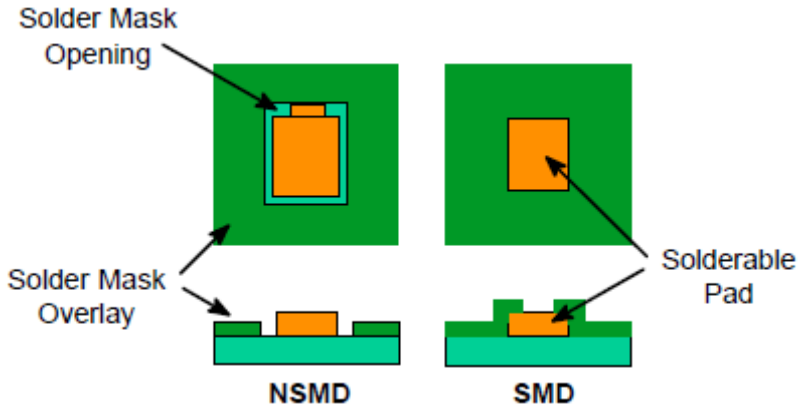


Figure 3. Examples of NSMD vs. SMD PADS

When possible the NSMD pads are preferred over the SMD configuration since defining the location and size of the copper pad is easier to control than the solder mask. This is based on the fact that the copper etching process is capable of a tighter tolerance than the solder masking process.

In addition, the SMD pads will inherently create a stress concentration point where the solder wets to the pad on top of the pattern. This stress concentration point is eliminated when the solder is allowed to flow down the sides of the pattern in the NSMD configuration.

The solder joint and pad design are the most important factors in creating a reliable assembly. The DFN8 package, falls into the category of MLP packages listed in JEDEC and a typical characteristic is that they are pre−plated and then punch separated, this process allows showing bare copper on the end of the leads. This is normal and addressed by IPC JEDEC J−STD−001C "*Bottom Only Termination*". Luckily the punching smears some of the plating over the exposed edge and that with a well designed pad and well characterized solder process often yields solder fillets over the three sides of the leads improving the reliability of the assembly. Example is shown in Figure 4.

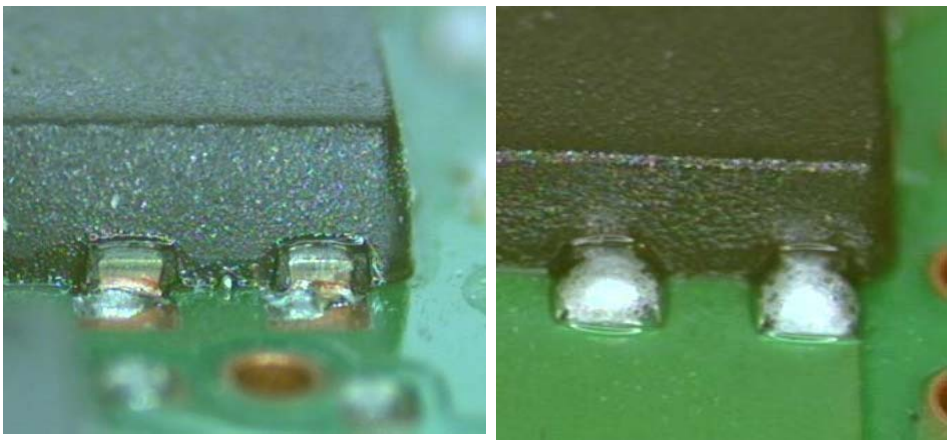
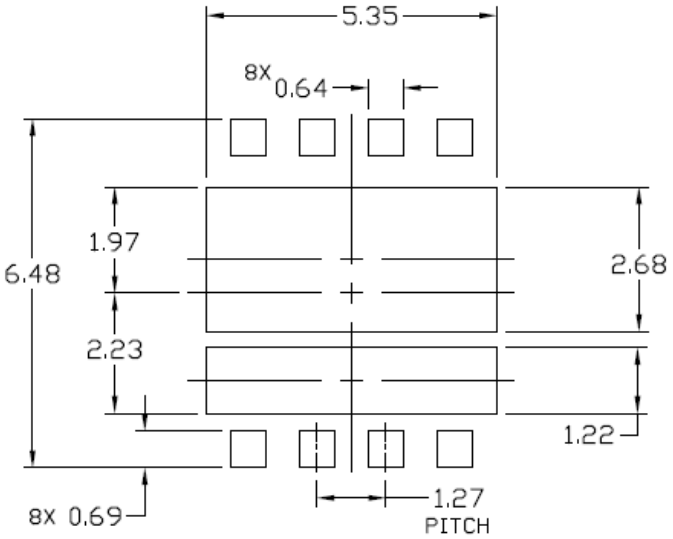


Figure 4. Example of Good Solder Pad Design plus Good Solder Reflow Process versus a Non Optimized Design

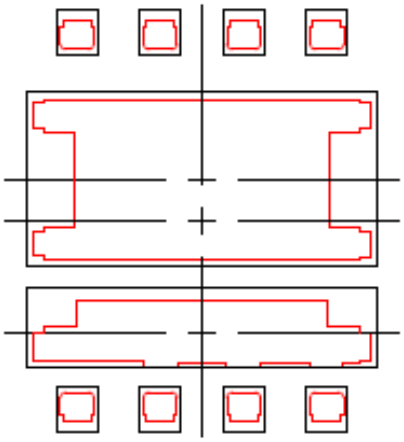
NSMD Pad Configurations

When it is dimensionally possible, the solder mask should be located at least ± 0.076 mm (0.003 in) away from the edge of the solderable pad. This spacing is used to compensate for the registration tolerances of the solder mask, as well as to insure that the solder is not inhibited by the mask as it reflows along the sides of the metal pad.

The dimensions of the solder pads should be larger than the device footprint to allow for visual inspection of solder fillet. This is shown in Figures 4 and 5. The ratio between the package's pad configuration and that of the PCB's is designed for optimal placement accuracy and reliability. These factors have already been considered for the recommended footprint given on the data sheet. It is recommended to the customer follow this guideline to assure best assembly yield, thermal performance and overall system performance.



DFN8 5x6 mm PCB Pattern



Package Footprint overlaid on PCB Pattern

Figure 5. Printed Circuit Board Layout using Non−Solder Masked Defined Pads

DFN8 5x6 mm Dual Asymmetrical Board Mounting Process

The surface mount process is optimized by first defining and controlling the following processes:

1. Creating and maintaining a solderable metallization on the PCB contacts.
2. Using via holes
3. Choosing the proper solder paste
4. Screening/stenciling the solder paste onto the PCB
5. Placing the package onto the PCB
6. Reflowing the solder paste
7. Final solder joint inspection

Recommendations for each of these processes are located below.

PCB Material and Solderable Metallization Finish

It is recommended that lead free FR−4 is used in the construction of PCB. Lower quality FR−4 can cause numerous problems with reflow temperatures seen with lead free solder compositions. If you need some guidelines please refer to IPC−4101B "specification for Base Materials for Rigid and Multilayer Printed Boards" publication for further information.

There are three common plated solderable metallization finishes which can be used for PCB surface mount devices. In any case, it is imperative that plating is uniform, conforming, and free of impurities to insure a consistent solderable system.

The first recommended metallization finish consists of plated electroless nickel over the copper pad, followed by immersion gold. The thickness of the electroless nickel layer is determined by the allowable internal material stresses and the temperature excursions the board will be subjected to through its lifetime. Even though the gold metallization is typically a self−limiting process, the thickness should be at least 0.05 μm thick, and not consist of more than 5% of the overall solder volume. Having excessive gold in the solder joint, can create gold embrittlement, which may affect the reliability of the joint.

The second recommended metallization finish consists of an Organic Solderability Preservative (OSP) coating over the copper plated pad. The organic coating assists in reducing oxidation in order to preserve the copper metallization for soldering.

The third recommended metallization finish is Immersion silver, which is a relative new PCB finish. It is considered a drop in replacement for HASL for soldering operations. The contrasting silver finish appears "white" on PCB surface makes it easy to inspect, as opposed to OSP.

Each finish has useful properties, and each has its own process details, which are beyond the scope of this

document. No one finish will be right for every application, but currently the most commonly seen in large scale commercial manufacturing, mainly because of cost, is OSP.

Using via Holes with DFN8, 5x6 mm, Dual Asymmetrical

More often than not, there is not enough copper area on one plane to increase the power handling of the device, to solve this problem the designer makes use of via holes to connect different metal planes, in multilayer designs, or connect the top side to the bottom side on two layer designs. While this is a common practice, the user should realize that via holes could cause a solder “leak” or wicking and induce voids, but if through−hole vias are used, a drill size of 0.3 mm with 1 ounce copper plating yields good performance. It is recommended to characterize the PCB and process designs with X−Ray inspection to ensure there is not a vioding problem. One basic recommendation is place the vias around the large pads, if possible, to avoid altogether the potential for voids.

Solder Type

Any standard lead free solder paste commonly used on the industry should work with this package. The IPC Solder Products Value Council has recommended the 96.5Sn/3.0Ag/0.5Cu SAC alloy to be the lead free solder paste alloy of choice for the electronics industry. Solder paste such as Cookson Electronics P/N WS3060 with a Type 3 or smaller sphere size is recommended. The WS3060 has a water soluble flux for cleaning. Cookson Electronics P/N C0106A can be used if a no−clean flux is preferred.

Solder Screening onto the PCB

Stencil screening the solder onto the PCB is commonly used in the industry. It is estimated that 60% of all assembly errors are due to paste printing. For a controlled, high yielding manufacturing process, it is one of the important steps of assembly. The recommended stencil thickness used is 0.127 mm (0.005 in) and the sidewalls of the stencil openings should be tapered approximately 5° along with an electro−polish finish to aid in the release of the paste when the stencil is removed from the PCB.

For a typical edge PCB terminal pad, the stencil opening should be the same size as the PCB mounting pad. However, in cases where the main device pad is soldered to the PCB, the stencil opening must be divided into a grid allowing channels for gases to vent as shown in Figure 6. Dividing the larger pad into smaller screen openings reduces the risk of solder voiding and allows the solder joints for smaller terminal pads to be at the same height as the larger ones. Typical solder coverage is 60 to 80% of exposed pad area. Another place to check is the following publication IPC−7525 “stencil Design Guidelines” where they give a formula for calculating the area ratio for paste release prediction:

$$\text{Area Ration} = \frac{\text{Area of Pad}}{\text{Area of Aperture Walls}} = \frac{L \cdot W}{2 \cdot (L \cdot W) \cdot T}$$

where L is the length, W the width, and T the thickness of the stencil. When using this equation and Area ratio > 0.66 should yield an acceptable paste release.

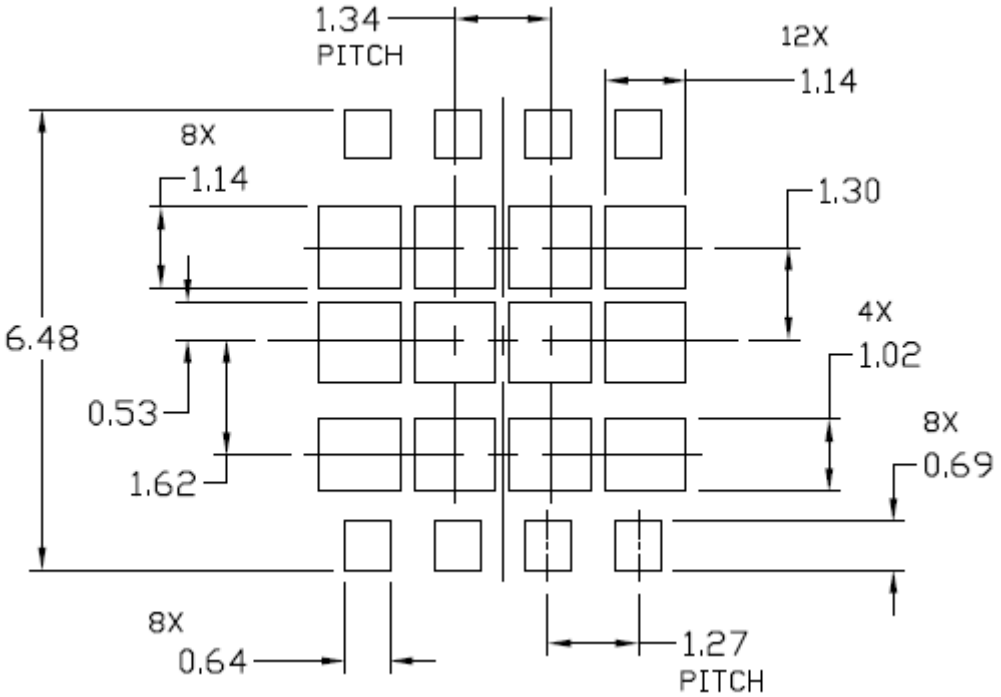


Figure 6. Solder Stencil Design Illustrating How Stencil Openings are Divided into an Array for Large Device Areas

Package Placement onto the PCB

Pick and place equipment with the standard tolerance of ± 0.05 mm or better is recommended. The package will tend to center itself and correct for slight placement errors during reflow process due to surface tension of the solder.

Solder Reflow

Once the package is placed on the PCB along with the solder paste, a standard surface mount reflow process can be used to solder the part. Figures 7 and 8 are examples of standard reflow profiles for typical Tin/Lead solder and Lead−Free solder alloys. Note the DFN8 package is qualified to meet Pb−free profile requirements per JEDEC specification J−STD−020C.

The optimum reflow profile used for every product and oven is different. Even the same equipment in a different facility may require an adjustment in the profile. The proper ramp and soak rates are determined by the solder paste vendor for their specific products. Obtaining this information from the paste vendor is highly recommended since the chemistry and viscosity of the flux matrix will vary. The exact profile will be determined by the Process Engineer based on the board density and thickness. These variations will require small changes in the profile in order to achieve an optimized process.

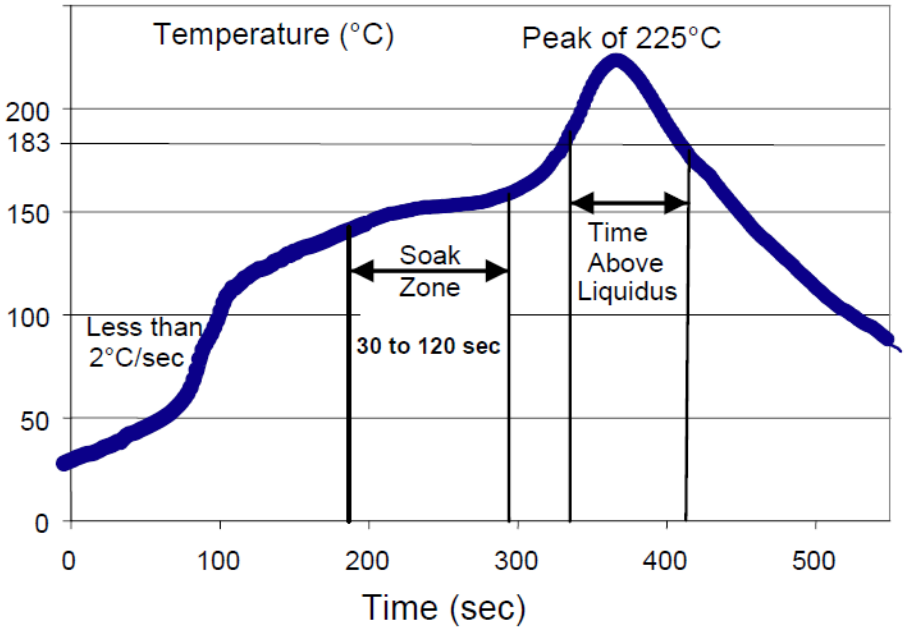


Figure 7. Typical Reflow Profile for Standard Tin/Lead (SnPb) Solder

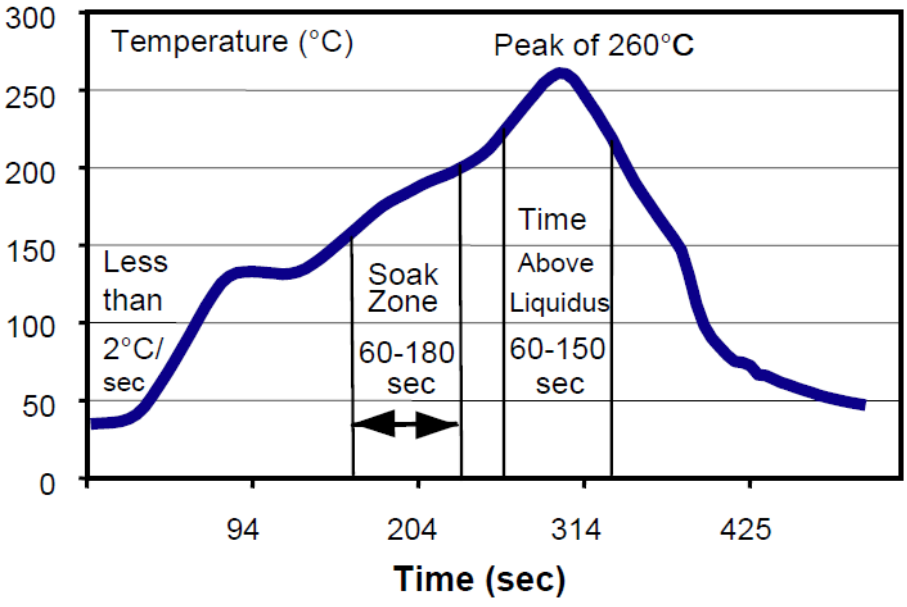


Figure 8. Typical Reflow Profile for Standard Pb−Free Solder

In general, the temperature of the part should not be raise more than 2°C/sec during the initial stages of the reflow profile. The soak zone then occurs when the part is approximately 150°C and should last for 60 to 180 seconds for Pb−free profiles (30 −120 seconds for SnPb profiles). Typically, extending the time in the soak zone will reduce the risk of voiding within the solder. The temperature is then raised and will be above the liquid state of the solder for 60 to 150 seconds for Pb−free profiles (30 to 100 seconds for SnPb profiles) depending on the mass of the board. The peak temperature of the profile should be between 245 and 260°C for Pb−free solder alloys (205 – 225°C for eutectic SnPb solders).

If required, removal of the residual solder flux can be completed by using the recommended procedures set forth by the flux manufacturer.

Final Solder Inspection

The inspection of the solder joints is commonly performed with the use of X−Ray inspection system. With this tool, one can locate defects such as shorts between pads, open contacts, voids within the solder as well as any extraneous solder.

In addition to searching for defects, the mounted device should be rotated on its side to inspect the sides of the solder joints with an X−Ray inspection system. The solder joints should have enough solder volume with the proper stand−off height so that an “hour glass” shaped connection is not formed as shown in Figure 9. “Hour glass” solder joints are a reliability concern and must be avoided.

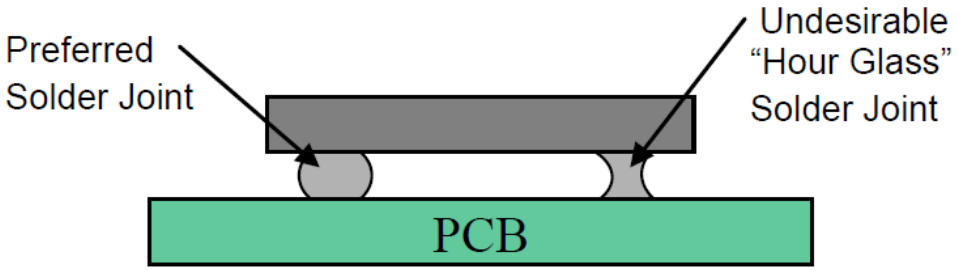


Figure 9. Side View of DFN 8 Attachment Illustrating Preferred and Undesirable Solder Joint Shapes

Rework Procedure

Because the DFN8, 5x6 mm, Dual Flag is a leadless device, the entire package must be removed from the PCB if there is an issue with the solder joints. It is important to minimize the chance of overheating neighboring devices during the removal of the package since the devices are typically in close proximity with each other. Due to the high temperatures associated with lead free reflow, it is recommended that this component not be reused if rework becomes necessary.

Standard SMT rework systems are recommended for this procedure since the airflow and temperature gradients can be carefully controlled. It is also recommended to place the PCB in an oven at 125°C for 4 to 8 hours prior to heating the parts to remove excess moisture from the packages. In order to control the region which will be exposed to reflow temperatures, the board should be heated to 100°C by conduction through the backside of the board in the location of the DFN8 Dual part. Typically, heating zones are then used, to increase the temperature locally.

Once the DFN8, Dual Flag solder joints are heated above their liquid temperature, the package is quickly removed and the pads on the PCB need to be cleaned. The cleaning of the pads is typically performed with a blade style conductive tool and with a de−soldering braid. A no−clean flux is used during this process in order to simplify the procedure.

Solder paste is then dispensed or screened onto the site in preparation of mounting a new device. Due to the close proximity of the neighboring packages in most PCB designs, a miniature stencil for the individual component is typically required. The same stencil design that was originally used to mount the package can be applied to the mini−stencil fro redressing the pad. If solder paste is dispensed an experienced technician in this type of rework is a very valuable asset.

Due to the small pad configurations of the DFN8, dual flag, and since the pads are on the underside of the package, a manual pick and place procedure without the aid of magnification is not recommended. A dual image optical system where the underside of the package can be aligned to the PCB should be used instead. If such system is not available a minimum of a stereo microscope with an X 15 eye pieces and an experienced technician will be a minimum to have a successful result.

Reflowing the component onto the board can be accomplished by either passing the board through the original reflow profile, or by selectively heating the package with the same process that was used to remove it. The benefit with subjecting the entire board to a second reflow is that the DFN8, Dual Flag will be mounted consistently and by a profile that is already defined. The disadvantage is that all of the other devices mounted with the same solder type will be reflowed for a second time. If subjecting all of the parts to a second reflow is either a concern or unacceptable for a specific application, then the localized reflow option would be the recommended procedure.

APPENDIX

Since the inception of this package, several competitors have come up with their own footprint version. The one that has really dominated the landscape in the industry is the Power 56 dual flag from Fairchild.

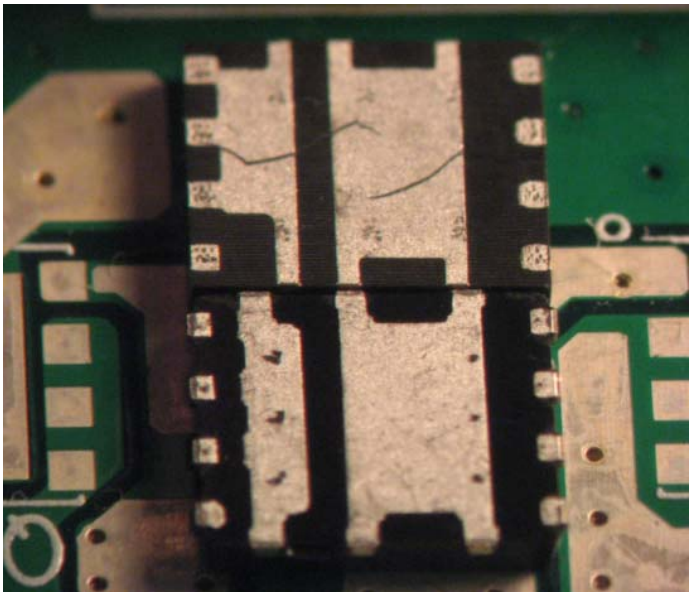


Figure A. Fairchild and ON Semiconductor Devices

In order to address compatibility and help customers define a pattern that can be conducive to both styles we have come up with the following optimized footprint and corresponding solder stencil.

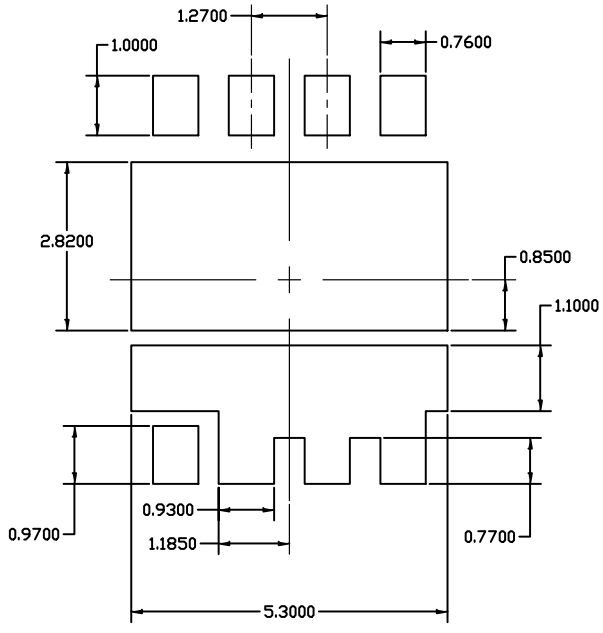


Figure B. Optimized Footprint to Accommodate Both Packages

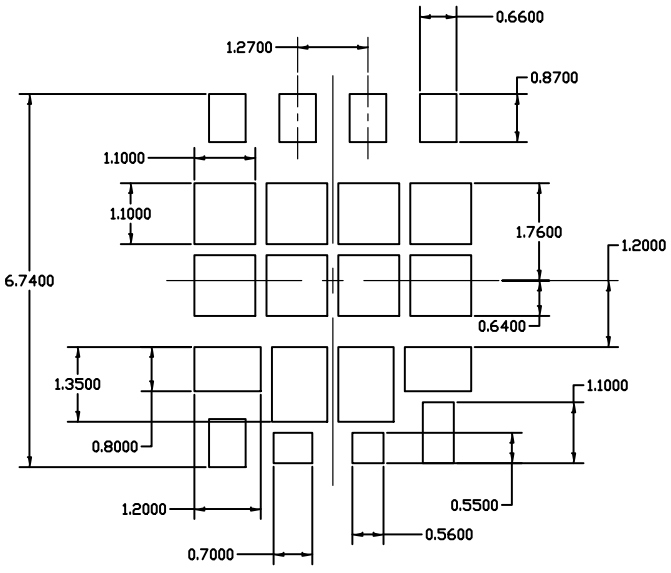


Figure C. Solder Stencil Design for Optimized Footprint

Both devices can fit on this optimized patter and it shown in the figure below overlaying each package style on top the recommended footprint

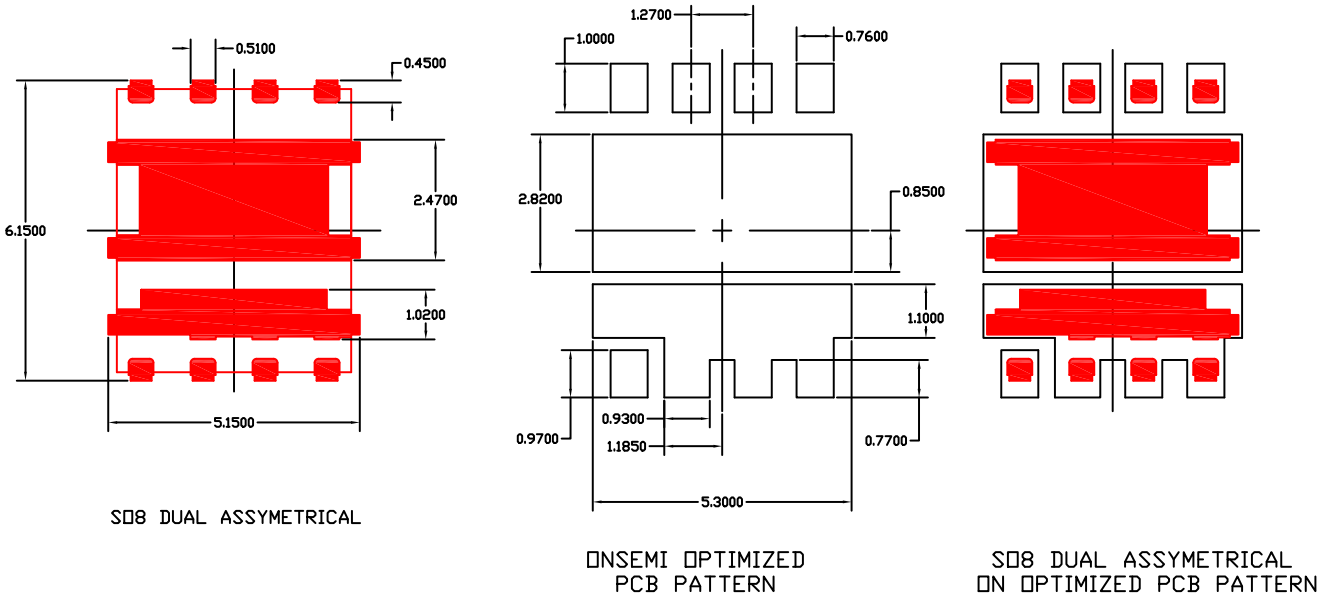


Figure D. Optimized Footprint with ON Semiconductor Dual Asymmetrical

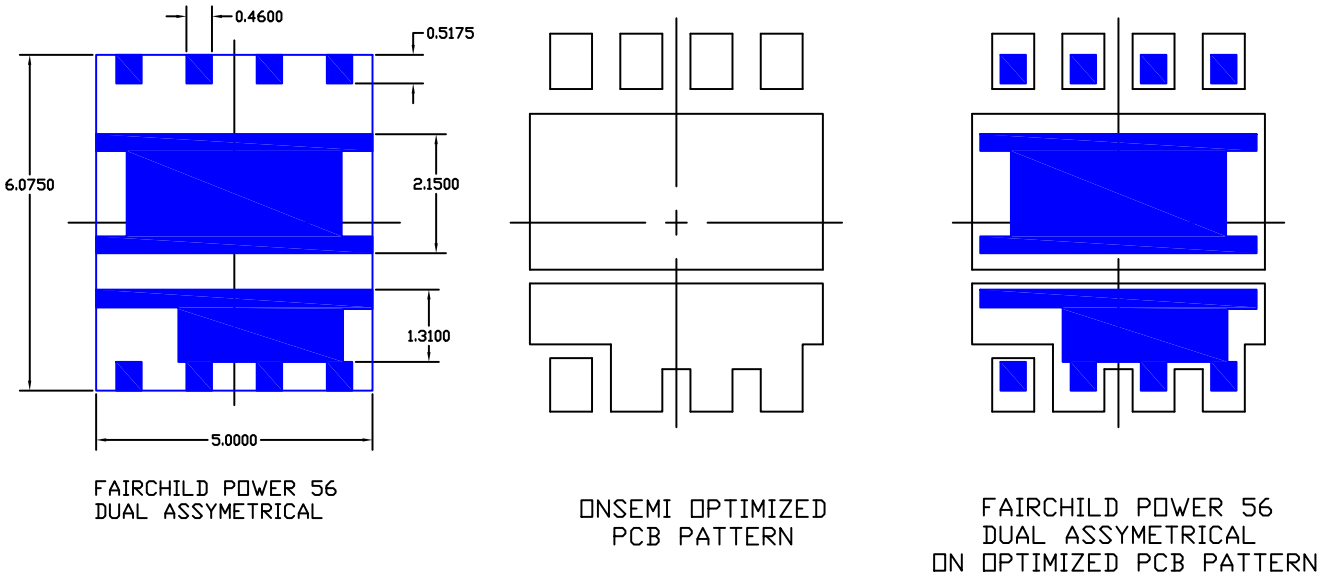


Figure E. Optimized Footprint with Power 56 Dual Flag

REFERENCES

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2. IPC J−STD−001C, “Requirements for Solder Electrical and Electronic Assemblies”, March 2000
3. IPC Solder Products Value Council, “Round Robin Testing and Analysis of Lead Free Solder Pastes with Alloys of Tin, Silver and Copper”, March 2006
4. IPC−SM−7525, Stencil Design Guidelines”, May 2000
5. IPC JEDEC−J−STD−020D.1 “Moisture/reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices”, March 2008

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