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LC Selection Guide for the DC-DC Synchronous Buck Converter

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APPLICATION NOTE

Introduction

Switched mode power converters are very prominent in industry today, and provide high efficiency solutions for a wide range of applications. Switched mode converters can be found in power supplies and battery charging circuitry for computers, electric tools, televisions, media tablets, smart phones, automobiles, and countless other electronic devices. One of the most popular converters for the consumer electronics industry is the DC:DC step−down converter, also known as the buck converter.

The synchronous buck converter is used to step a voltage down from a higher level to a lower level. With industry moving to higher performance platforms, efficiency of the power converter is critical. The design of the power converter must be optimized to maximize performance and to meet customer requirements. Because of this, it is important to understand the fundamentals of the synchronous buck converter and how to appropriately select the circuit components.

Synchronous Buck Converter Basics

The synchronous buck converter is straightforward in concept, and is used heavily in consumer electronics. A synchronous buck converter produces a regulated voltage that is lower than its input voltage, and can deliver high currents while minimizing power loss. As shown in Figure 1, the synchronous buck converter is comprised of two power MOSFETs, an output inductor and an output capacitor. This specific buck topology derives its name from the control method of the two power MOSFETs; the on / off control is synchronized in order to provide a regulated output voltage and to prevent the MOSFETs from turning on at the same time.

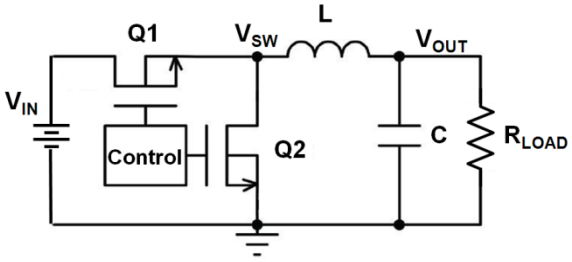

Figure 1. Synchronous Buck Converter

Q1, the high side MOSFET, is connected directly to the input voltage of the circuit. When Q1 turns on, current is supplied to the load through the high side MOSFET. During this time, Q2 is off and the current through the inductor increases, charging the LC filter. When Q1 turns off, Q2 turns on and current is supplied to the load through the low side MOSFET. During this time, the current through the inductor decreases, discharging the LC filter. The low side MOSFET provides an additional function when both MOSFETs are off. It clamps the switch node voltage via the body diode to prevent V_{SW} from going too far negative when the high side transistor first turns off.

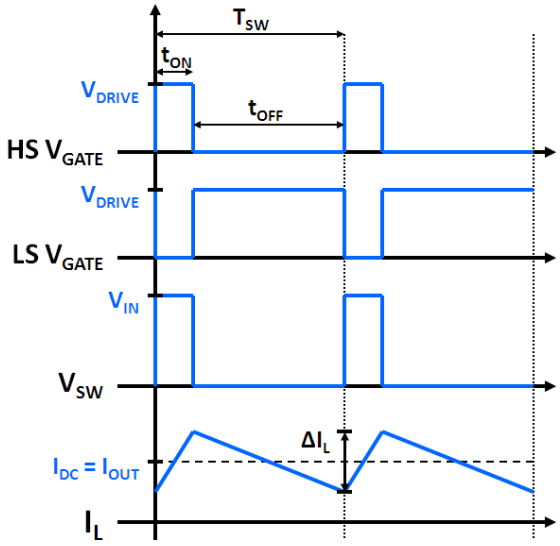

Figure 2. Synchronous Buck Converter Waveforms

Figure 2 shows the basic waveforms for the synchronous buck converter in continuous conduction mode. The total change in inductor current is known as the peak−to−peak inductor current, ΔI_L. The switch node voltage is smoothed out by the LC output stage in order to produce a regulated DC voltage at the output. The MOSFETs are controlled synchronously to prevent shoot−through. Shoot−through occurs when the high side and low side MOSFET are both on at the same time, providing a direct short to ground.

The high side MOSFET on−time determines the duty cycle of the circuit, and is defined in Equation 1.

$$D = \frac{t_{ON,HS}}{t_{ON,HS} + t_{OFF,HS}} \cong \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 1)}$$

If the duty cycle, D, is equal to 1 then the high side MOSFET is on 100% of the time and the output voltage equals the input voltage. A duty cycle of 0.1 means that the high side MOSFET is on 10% of the time, producing an output voltage that is approximately 10% of the input voltage.

Buck Converter Power Loss

The buck converter power losses are influenced by multiple factors, including the power MOSFETs, output stage, controller / driver, feedback loop, and layout of the converter itself. The duty cycle is less than 0.5 for most buck converter designs, with a standard duty cycle of 0.1 to 0.2 in the computing and server market. Design platforms are moving to higher switching frequencies, providing the ability to reduce converter size and form factors. At the same time, converters must deliver greater performance and have higher efficiency. The output stage performance greatly impacts the overall performance of the buck converter. For this reason, it is important to optimize the inductor and capacitor selection for the specific application. The rest of this application note focuses on the output stage design.

The LC Output Stage

The output stage of the synchronous buck converter is comprised of an inductor and capacitor. The output stage stores and delivers energy to the load, and smoothes out the switch node voltage to produce a constant output voltage.

Inductor selection directly influences the amount of current ripple seen on the inductor current, as well as the current capability of the buck converter itself. Inductors vary from manufacturer to manufacturer in both material and value, and typically have a tolerance of ±20%.

Inductors have an inherent DC resistance (known as the DCR) that impacts the performance of the output stage. Minimizing the DCR improves the overall performance of the converter. For applications that require a high load current, it is recommended to select an inductor with a low DCR. The DCR is smaller for lower inductor values, but there is a trade−off between inductance and ripple current; the lower the inductance, the higher the ripple current through the inductor. A minimum inductance must be met in order to meet the ripple current requirements of the specific application circuit.

The output capacitance directly affects the output voltage of the converter, the response time of the output feedback loop, and the amount of output voltage overshoot that occurs during changes in load current. A ripple voltage exists on the DC output as the current through the inductor and capacitor increases and decreases. Increasing the capacitance reduces the amount of ripple voltage present. However, there is a tradeoff between capacitance and the output response. Increasing the capacitance reduces the output voltage ripple and output voltage overshoot, but increases the time it takes the output voltage feedback loop to respond to changes in load. Therefore, a minimum capacitance must be considered, in order to meet the ripple voltage and voltage overshoot requirements of the converter, while maintaining a feedback loop that can respond quickly enough to load changes.

Capacitors also have a parasitic series resistance, known as the equivalent series resistance (ESR). The ESR impacts the output voltage ripple and the overall efficiency of the converter. Because of this, designers are moving to low ESR designs. Surface mount ceramic capacitors are becoming prevalent in systems that require high performance in a small form factor. The use of multiple capacitors in parallel allows designers to achieve the necessary capacitance for the system while greatly reducing the equivalent ESR.

Basic LC Design

When designing the buck converter output stage, it is recommended to begin with the inductor. The minimum inductance is calculated based on the target ripple current and other application circuit specifications. Once the inductor has been selected, the minimum capacitance can be determined.

Calculating Minimum Inductance

Let's begin with the basic inductor current / voltage relationship, seen in Equation 2.

$$V_L = L \cdot \frac{dI_L}{dt} \quad \text{(eq. 2)}$$

Inductor current ripple is defined as the peak−to−peak change in current during the converter on time. For the synchronous buck converter, the change in inductor current during the high side MOSFET on−time is equal to the change during the high side MOSFET off−time. In other words, the inductor current increase is equal to the inductor current decrease (refer to Figure 2).

$$\Delta I_{L(+)} = \Delta I_{L(-)} \quad \text{(eq. 3)}$$

For this reason, the inductor current ripple can simply be defined as ΔI_L and units are Amperes. The dI_L/dt term during the converter on time can be written as:

$$\frac{dI_L}{dt} = \frac{\Delta I_L}{t_{ON,HS}} \quad \text{(eq. 4)}$$

Combining Equation 2 and Equation 4 and solving for the inductance yields Equation 5.

$$L_{MIN} = \frac{V_{L(ON)} \cdot t_{ON,HS}}{\Delta I_L} \quad \text{(eq. 5)}$$

In order to solve for inductance in terms of the application circuit parameters, some additional terms must be defined first.

During the converter on time, the high side MOSFET is conducting and the low side MOSFET is off. Using Kirkhoff's voltage law, $V_{L(ON)}$ is defined as

$$V_{L(ON)} = V_{IN} - V_{HS} - V_{OUT} \quad \text{(eq. 6)}$$

where V_{HS} is the voltage drop across the high side MOSFET and is defined as:

$$V_{HS} = R_{DS(on)HS} \cdot D \cdot I_{OUT,MAX} \quad \text{(eq. 7)}$$

The duty cycle is defined as the ratio of high side MOSFET on time to the switching period of the converter. In other words,

$$D = \frac{t_{ON,HS}}{T_{SW}} = t_{ON,HS} \cdot f_{SW} \quad \text{(eq. 8)}$$

And Equation 5 becomes:

$$L_{MIN} = \frac{(V_{IN} - V_{HS} - V_{OUT}) \cdot D}{\Delta I_L \cdot f_{SW}} \quad \text{(eq. 9)}$$

The ripple current can also be expressed in terms of the inductor current ripple ratio, or LIR.

$$\Delta I_L = LIR \cdot I_{OUT,MAX} \quad \text{(eq. 10)}$$

Substituting Equation 10 into Equation 9, the minimum inductance, L_{MIN}, becomes:

$$L_{MIN} = \frac{(V_{IN} - V_{HS} - V_{OUT}) \cdot D}{LIR \cdot I_{OUT,MAX} \cdot f_{SW}} \quad \text{(eq. 11)}$$

Equation 3 can be used to calculate the duty cycle, D using $\Delta I_L(+)$ and $\Delta I_L(-)$ as defined in Equation 12 and 13 below.

$$\Delta I_{L(+)} = \frac{V_{L\_ON,HS}}{L} \cdot t_{ON,HS} \quad \text{(eq. 12)}$$

$$\Delta I_{L(-)} = \frac{V_{L\_OFF,HS}}{L} \cdot t_{OFF,HS} \quad \text{(eq. 13)}$$

where $V_{L(ON)}$ is defined in Equation 6 and $V_{L(OFF)}$ is:

$$V_{L(OFF)} = V_{OUT} + V_{LS} \quad \text{(eq. 14)}$$

The high side MOSFET t_{ON} and t_{OFF} can also be written in terms of duty cycle.

$$t_{ON,HS} = \frac{D}{f_{SW}} \quad \text{(eq. 15)}$$

$$t_{OFF,HS} = \frac{1 - D}{f_{SW}} \quad \text{(eq. 16)}$$

Setting $\Delta I_L(+)$ equal to $\Delta I_L(-)$ and substituting Equations 14, 15 and 16, the duty cycle becomes:

$$D = \frac{V_{OUT} + V_{LS}}{V_{IN} - V_{HS} + V_{LS}} \quad \text{(eq. 17)}$$

where V_{LS} the voltage drop across the low side MOSFET when it is conducting, and is defined as:

$$V_{LS} = R_{DS(on)LS} \cdot (1 - D) \cdot I_{OUT,MAX} \quad \text{(eq. 18)}$$

Therefore, the final inductance equation, L_{MIN}, becomes:

$$L_{MIN} = \left(\frac{V_{IN} - V_{HS} - V_{OUT}}{LIR \cdot I_{OUT,MAX} \cdot f_{SW}}\right) \cdot \left(\frac{V_{OUT} + V_{LS}}{V_{IN} - V_{HS} + V_{LS}}\right) \quad \text{(eq. 19)}$$

Equation 19 can be simplified by neglecting the high side and low side MOSFET voltage drops, producing a minimum inductance of

$$L_{MIN} \cong \frac{(V_{IN} - V_{OUT}) \cdot D}{LIR \cdot I_{OUT,MAX} \cdot f_{SW}} \quad \text{(eq. 20)}$$

where the duty cycle is estimated to be

$$D \cong \frac{V_{OUT}}{V_{IN}} \quad \text{(eq. 21)}$$

As can be seen, there is a tradeoff between inductance and ripple current. Lower target ripple current equates to higher minimum inductance. To optimize the output filter performance it is recommended to target 20% – 40% inductor ripple current, which translates to an LIR of 0.2 – 0.4.

Calculating Maximum ESR and Minimum Capacitance

Capacitance is required to maintain a regulated output voltage while the high side MOSFET is off, and is necessary to minimize the amount of ripple present on the output voltage. The output voltage ripple, ΔV_{PP}, can be expressed as a peak−to−peak voltage or in terms of the Capacitor Voltage Ratio, or CVR.

$$\Delta V_{PP} = CVR \cdot V_{OUT} \quad \text{(eq. 22)}$$

A CVR of 0.05, for example, equates to an output ripple voltage that is 5% of the DC output voltage.

ESR and capacitance influence the response time of the output feedback loop. The larger the output capacitance value and ESR, the longer it takes for the output to respond to changes in load. ESR also influences the output voltage ripple. The maximum ESR can be calculated using the specified maximum voltage ripple, ΔV_{PP}, and the maximum load current, as shown in Equation 23.

$$ESR_{MAX} = \frac{\Delta V_{PP}}{I_{OUT,MAX}} = \frac{CVR \cdot V_{OUT}}{I_{OUT,MAX}} \quad \text{(eq. 23)}$$

Therefore, in order to have an output voltage ripple below the specified maximum, the ESR of the output capacitance must be less than the value calculated using Equation 23.

When the high side MOSFET is on, current through the inductor and capacitor is increasing, and the output voltage increases. When the high side MOSFET is off, current through the inductor and capacitor are decreasing, and the output voltage decreases. In order to achieve a constant output voltage, the amount of capacitor current increase must be equal to the amount of capacitor current decrease. Therefore, the steady state current through the capacitor is 0 A (Figure 3).

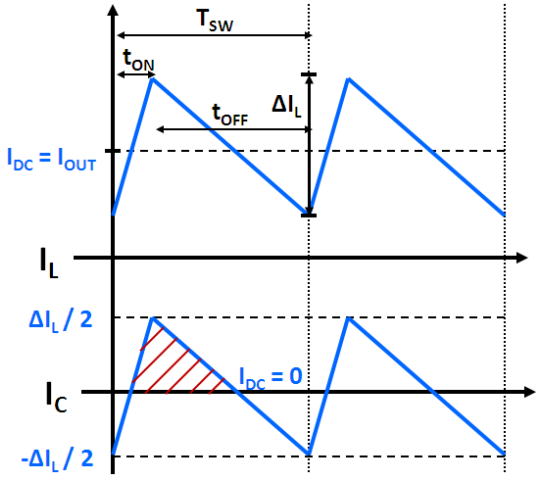

Figure 3. Inductor and Capacitor Current

The current through the capacitor is defined as:

$$I_C = C \cdot \frac{\Delta V_C}{\Delta t} \quad \text{(eq. 24)}$$

and can be re−written as:

$$\Delta t \cdot I_C = C \cdot \Delta V_C = \Delta Q_C \quad \text{(eq. 25)}$$

The area under the curve (shown in red in Figure 3) is the capacitor charge, ΔQ_C, and is defined as:

$$\Delta Q_C = \left(\frac{1}{2}\right) \cdot \Delta I_C \cdot \Delta t \quad \text{(eq. 26)}$$

where
$$\Delta t = \left(\frac{1}{2}\right) \cdot t_{ON} + \left(\frac{1}{2}\right) \cdot t_{OFF} \quad \text{(eq. 27)}$$
$$= \left(\frac{1}{2}\right) \cdot \left(\frac{D}{f_{SW}}\right) + \left(\frac{1}{2}\right) \cdot \left(\frac{1 - D}{f_{SW}}\right)$$
$$= \frac{1}{2 \cdot f_{SW}}$$

and
$$\Delta I_C = \frac{\Delta I_L}{2} \quad \text{(eq. 28)}$$

Therefore, Equation 26 can be re−written as:

$$\Delta Q_C = \left(\frac{1}{2}\right) \cdot \left(\frac{\Delta I_L}{2}\right) \cdot \left(\frac{1}{2 \cdot f_{SW}}\right) = \frac{\Delta I_L}{8 \cdot f_{SW}} \quad \text{(eq. 29)}$$

And Equation 25 becomes:

$$\frac{\Delta I_L}{8 \cdot f_{SW}} = C_{MIN} \cdot \Delta V_{PP} \quad \text{(eq. 30)}$$

The minimum output capacitance due to the output ripplve voltage can be derived by combining Equations 10, 22 and 30 and solving for capacitance.

$$C_{MIN} = \frac{LIR \cdot I_{OUT,MAX}}{8 \cdot f_{SW} \cdot CVR \cdot V_{OUT}} \quad \text{(eq. 31)}$$

The above equation only considers the affect of output ripple voltage and inductor ripple current on the output capacitance. The transient load response capability of the output stage must also be considered. The synchronous buck converter must be able to respond to changes in load current while maintaining a regulated output voltage. When the load current changes from a higher value to a lower value, the output voltage will temporarily increase until the converter is able to adjust the duty cycle to return the output voltage to its regulated value. This temporary output voltage increase is known as output voltage overshoot, V_{OV}. The worst−case overshoot will occur when the load transitions from maximum load to no load. The output capacitor must be able to handle this transient condition.

The total energy of the output stage is defined as:

$$E_{TOT} = E_C + E_L = \left(\frac{1}{2}\right) \cdot C \cdot {V_C}^2 + \left(\frac{1}{2}\right) \cdot L \cdot {I_L}^2 \quad \text{(eq. 32)}$$

The total energy prior to the load transition must be equal to the total energy after the load transition. Therefore, (eq. 33)

$$\left(\frac{1}{2}\right) \cdot C \cdot {V_{OUT}}^2 + \left(\frac{1}{2}\right) \cdot L \cdot {I_{PK}}^2 = \left(\frac{1}{2}\right) \cdot C \cdot \left(V_{OV} + V_{OUT}\right)^2$$

Solving for C, the equation becomes:

$$C_{MIN} = \frac{L \cdot {I_{PK}}^2}{(V_{OV} + V_{OUT})^2 - {V_{OUT}}^2} \quad \text{(eq. 34)}$$

where I_{PK} is defined as:

$$I_{PEAK} = I_{OUT,MAX} \cdot \frac{\Delta I_L}{2} \quad \text{(eq. 35)}$$

Both Equations 31 and 34 must be taken into consideration when selecting the output capacitance. There is a tradeoff between the output voltage transient response and output voltage ripple. These two must be balanced for the needs of the specific application.

LC Design Example

This section walks through a design example applying the equations defined in the previous section. Table 1 lists the target application requirements for this example that must be met by the converter design.

Table 1. DESIGN EXAMPLE CIRCUIT REQUIREMENTS

Parameter	Symbol	Target
Input Voltage	V_{IN}	12 V
Output Voltage	V_{OUT}	1.2 V
Switching Frequency	f_{SW}	700 kHz
Inductor Current Ripple Ratio	LIR	0.3
Capacitor Voltage Ripple Ratio	CVR	0.04
Output Voltage Max Overshoot	V_{OV}	96 mV
Maximum Output Current	$I_{OUT,MAX}$	25 A

First, the duty cycle can be estimated, using Equation 21. For this example, the duty cycle is:

$$D \cong \frac{1.2\ V}{12\ V} = 0.1 \quad \text{(eq. 36)}$$

Next, the minimum inductance is calculated using Equation 20. For this example, L_{MIN} is:

$$L_{MIN} \cong \frac{(12\ V - 1.2\ V) \cdot 0.1}{0.3 \cdot 25\ A \cdot (700 \cdot 10^3)Hz} = 0.206\ \mu H \quad \text{(eq. 37)}$$

Therefore, to obtain a ripple current that is less than 30% of the maximum output current, the inductor selected must have an inductance value higher than 0.206 μH. The inductor selected for this application must have a saturation current that is higher than the peak current requirements of the application. For this example, I_{PK} is

$$I_{PK} = 25\ A + \frac{0.3 \cdot 25\ A}{2} = 28.75\ A \quad \text{(eq. 38)}$$

The saturation current of the inductor must be greater than 28.75 A. A good rule of thumb is to select an inductor with a saturation current at least 20% higher than the application's peak current.

The minimum output capacitance is calculated using Equations 31 and 34. The minimum capacitance needed to meet the output voltage ripple ratio is:

$$C_{MIN} = \frac{0.3 \cdot 25\ A}{8 \cdot (700 \cdot 10^3\ Hz) \cdot (0.04 \cdot 1.2\ V)} = 27.9\ \mu F \quad \text{(eq. 39)}$$

The minimum output capacitance needed to achieve a maximum output voltage overshoot of 96 mV for the worst−case load transient condition is:

$$C_{MIN} = \frac{L \cdot {I_{PK}}^2}{(V_{OV} + V_{OUT})^2 - {V_{OUT}}^2} \quad \text{(eq. 40)}$$

$$C_{MIN} = \frac{0.206\ \mu H \cdot (28.75\ A)^2}{(0.096\ V + 1.2\ V)^2 - (1.2\ V)^2} = 709.6\ \mu F$$

A good rule of thumb when selecting capacitance is to choose an out capacitor value that is at least 20% higher than the minimum calculated capacitance, to account for capacitor tolerance.

LC Experiments

The buck converter output filter design affects the output current ripple, output voltage ripple, output voltage overshoot, and the transient response of the feedback loop. Component selection also impacts the efficiency of the converter. Open−loop and closed loop experiments were carried out to examine the effect of capacitance and inductance on the converter's performance.

Three inductors were selected for the experiments in order to examine the impact of inductance value and DCR on circuit performance. Two inductors with equivalent DCR but different inductance were selected to examine the impact of inductance value on circuit performance. They differed in core size and inductance, but were made from the same material and by the same manufacturer. A third inductor was selected to examine the impact of the DCR on circuit performance. It was selected from the same manufacturer, but differed in core material.

Table 2. INDUCTORS USED IN EXPERIMENTS

L (uH)	DCR	ISAT (A)	Core Size (mm)
0.30	1.0	35	10 x 10
0.82	0.9	35	13 x 13
0.30	0.29	32.5	9.6 x 6.4

Table 2 lists the inductance, DCR, saturation current and core size for the three surface mount inductors used in the experiments.

LC Filter Impact on Ripple Current and Ripple Voltage

A buck converter was tested under the conditions listed in Table 3, in an open−loop configuration, using a 5 V MOSFET driver. A signal generator was used to create the PWM pulse. The inductor current was measured using a current probe.

Table 3. TEST CONDITIONS FOR EXPERIMENTS

Parameter	Symbol	Value
Input Voltage	V_{IN}	12 V
Output Voltage	V_{OUT}	1.2 V
Switching Frequency	f_{SW}	700 kHz
Drive Voltage	V_{DRIVE}	5 V
Load Current	I_{LOAD}	0 – 25 A
LIR Maximum	ΔI_L	0.3
CVR Maximum	ΔV_{PP}	0.04

Table 4 lists the output filter parameters tested in the open−loop configurations. All waveforms were measured at a load current of 25 A.

Table 4. LC VALUES FOR OPEN−LOOP EXPERIMENTS

Test	L−Value (μH)	L−DCR (mΩ)	C−Value (μH)
1	0.30	1	1600
2	0.82	0.9	3200

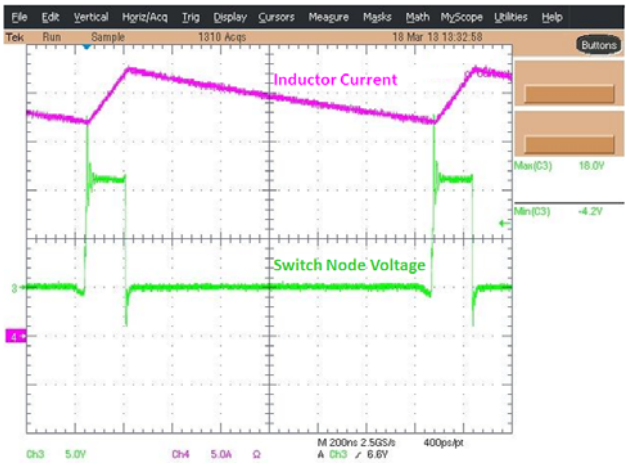

Figure 4. Ripple Current for 0.3 μH Inductor

Figure 4 shows the ripple current for the 0.30 μH / 1600 μF output filter. As can be seen, the measured output ripple current was 6 A.

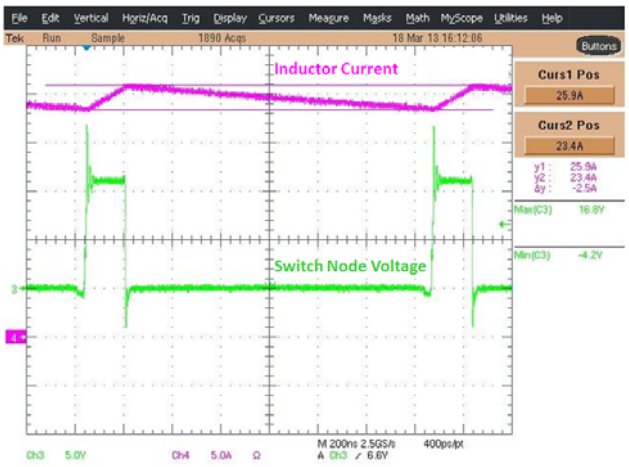

Figure 5. Ripple Current for 0.82 μH Inductor

Figure 5 shows the ripple current for the 0.82 μH / 3200 μF output filter. At a 25 A load, the measured ripple current was 2.5 A. According to the parameters specified in Table 3, the ripple current could not exceed 30% of the maximum load current (7 A). For both cases, this requirement was met. As can be seen from the experiment, using a higher inductance value reduced the measured ripple current.

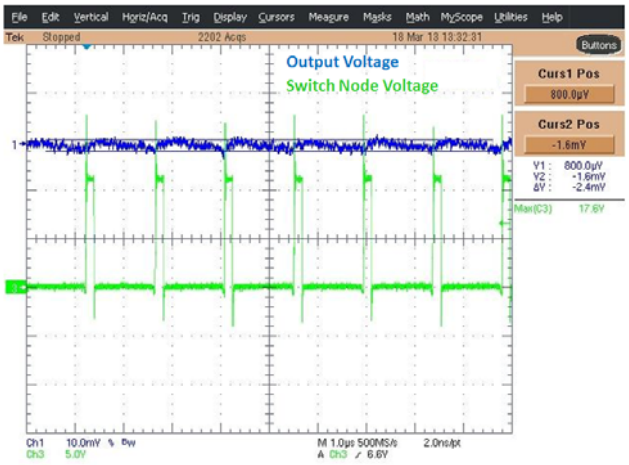

Figure 6. Ripple Voltage for 1600 µF Capacitance

Figure 6 and 7 show the output ripple voltage measured for 1600 µF and 3200 µF capacitance respectively.

As can be seen, the output ripple voltage is less for the 3200 µF capacitance.

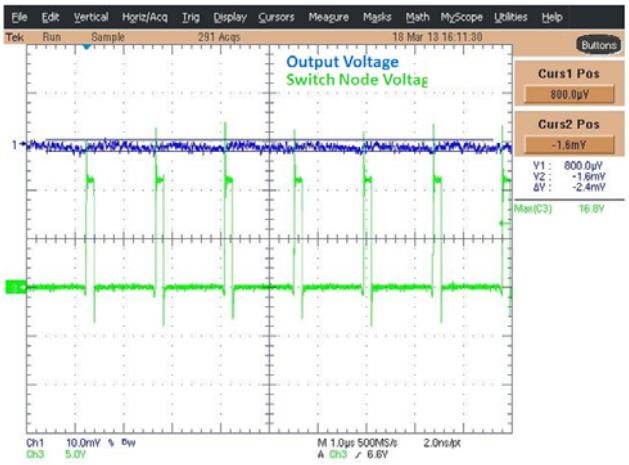

Figure 7. Ripple Voltage for 3200 µF Capacitance

The specified maximum ripple voltage requirement was 4% (48 mV). For both 1600 µF and 3200 µF capacitances, the ripple voltage limit was not exceeded.

LC Filter Impact on Efficiency

Next, closed−loop experiments were run to see the effect of the output filter on efficiency. Table 5 lists the inductor and capacitor combinations used in the experiments.

Table 5. LC VALUES FOR EFFICIENCY EXPERIMENTS

Test	L−Value (µH)	L−DCR (mΩ)	C−Value (µF)
1	0.30	1	1600
2	0.30	1	3200
3	0.30	0.29	1600

Each experiment was run under the conditions listed in Table 6. The efficiency of the test circuit was then compared between tests to see the effects of output filter on circuit performance.

Table 6. TEST CONDITIONS (Efficiency Experiments)

Parameter	Symbol	Value
Input Voltage	V_{IN}	12 V
Output Voltage	V_{OUT}	1.2 V
Switching Frequency	f_{SW}	700 kHz
Drive Voltage	V_{DRIVE}	5 V
Load Current	I_{LOAD}	1 – 25 A

First, the effect of output capacitance was examined. A 0.3 µH inductor with a 1 mΩ DCR was used for both tests. The output capacitances used were 1600 µF and 3200 µF. As can be seen in Figure 8, increasing the output capacitance slightly lowered the circuit's efficiency. In this example, doubling the output capacitance had minimal effect on the efficiency performance.

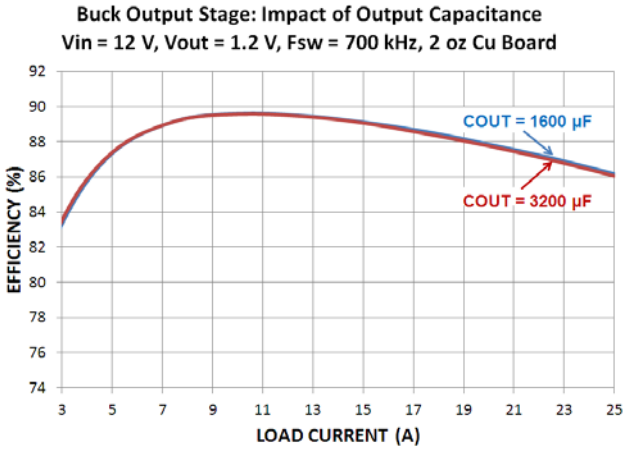

Figure 8. Effect of Capacitance on Efficiency

Next, the effect of inductor DCR was examined. Two 0.3 µH inductors, one with 1 mΩ and the other with 0.29 mΩ, were paired with 1600 µF output capacitance. As can be seen in Figure 9, DCR has a significant effect on the circuit performance, producing a 1.7% efficiency improvement at maximum load by using the inductor with 0.29 mΩ DCR.

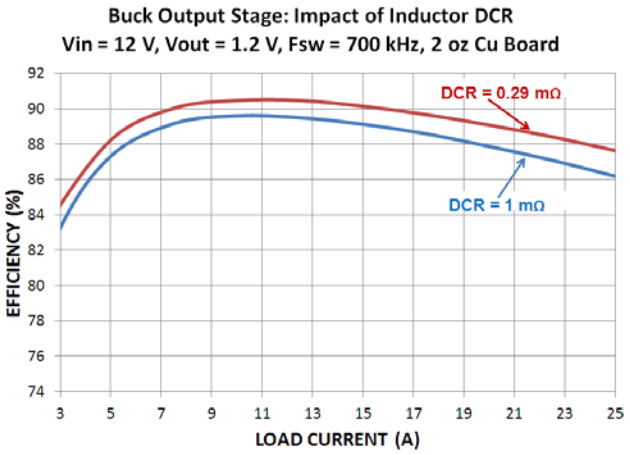

Figure 9. Effect of Inductor DCR on Efficiency

Inductance and DCR both affect the converter's efficiency. Figure 10 shows the efficiency results of four different inductors. At light load, the efficiency correlates to inductance value; the higher the inductance, the higher the light−load efficiency. As the load current increases, the DCR begins to dominate. At heavy loads, the efficiency correlates to the DCR value; the 0.29 mΩ DCR produced the highest efficiency, and the 1.56 mΩ DCR produced the lowest efficiency.

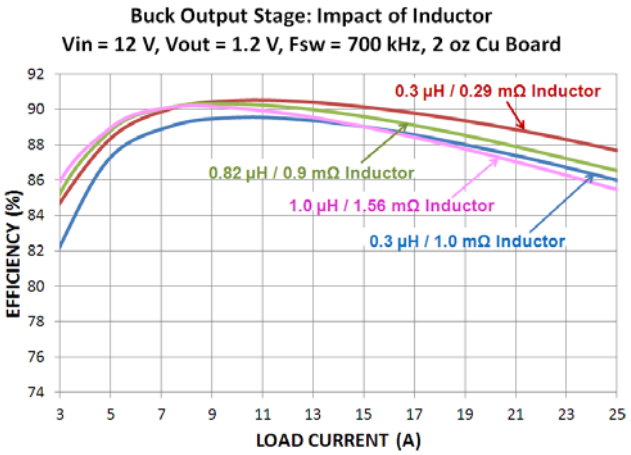

Figure 10. Effect of Inductance on Efficiency

As can be seen from the experiment, the efficiency was most impacted by the output inductor selection. Both the inductor value and DCR significantly affected the efficiency of the converter.

Conclusion

The output stage of the synchronous buck converter plays a significant role in the performance of the converter. In order to meet the target ripple current, output ripple voltage, and output voltage overshoot, a minimum inductance and capacitance must be exceeded. Additional factors must also be considered when selecting an inductor and capacitor for a specific application. The output stage can be optimized by designing for the specific application criteria that it will be operating in.

From the experiment results, it was found that the inductor value played a significant role in the output ripple current, as well as in the converter's efficiency performance. The 0.82 µH inductor ripple current was a third of the 0.3 µH inductor ripple current. Similarly, the output voltage ripple improved with a higher output capacitance.

The efficiency of the converter was greatly impacted by the DCR of the inductor. Holding the output capacitance and output inductance constant, the 0.29 mΩ DCR provided 1.7% higher efficiency at maximum load compared with the 1 mΩ DCR.

There is a tradeoff between inductance and saturation current for inductors. Therefore, to meet or exceed a ripple current requirement, the inductance must be greater than the minimum calculated inductance, and the saturation current of the inductor must be greater than the peak current of the converter at maximum load.

Capacitance also plays a significant role in the performance of the synchronous buck converter. Output capacitance directly influences the amount of voltage ripple and voltage overshoot seen on the output. Experiments showed that the capacitance had minimal effect on the efficiency performance.

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