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AND9129/D

Understanding a Digital Transistor Datasheet

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APPLICATION NOTE

Introduction

This application note will describe the common specifications of a Digital Transistor. It will also show how to use these specifications to successfully design with a Digital Transistor. Parameters from the DTC114E/D datasheet will be used to help with explanations. This datasheet describes a Digital Transistor that has an input resistor, R1, equal to 10 kΩ and a base−emitter resistor, R2, equal to 10 kΩ. Figure 1 gives a labeled schematic of a Digital Transistor. These labels will be used throughout this application note.

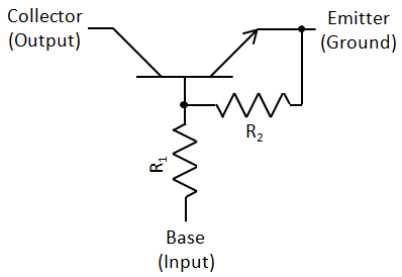

Figure 1. Labeled Schematic

For Digital Transistors it is important to realize that the transistor and resistor network is considered as one unit. An example of this is the I_{CBO} parameter. Looking at this parameter one would think that it is not possible. How could the emitter be open when R_2 connects the emitter and base of the transistor? Shouldn't it be I_{CER}? The answer is yes R_2 connects the emitter and base of the transistor, but this connection is built into the device. What is considered the emitter and base of the Digital Transistor is left open. In the case of a Digital Transistor I_{CER} would mean that there is an additional resistor placed between the emitter and base of the digital transistor. Figure 2 shows the difference between I_{CBO} and I_{CER} when referring to Digital Transistors.

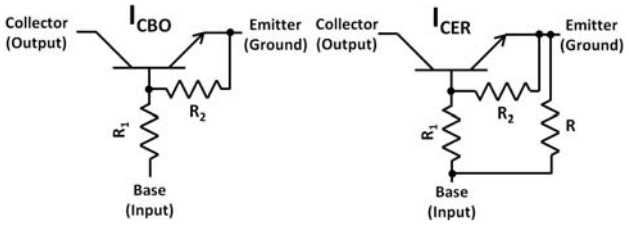

Figure 2. I_{CBO} vs. I_{CER}

Maximum Ratings

Below is the maximum ratings table that can be found in every Digital Transistor datasheet.

Table 1. MAXIMUM RATINGS

Rating	Symbol	Max	Unit
Collector−Base Voltage	V_{CBO}	50	Vdc
Collector−Emitter Voltage	V_{CEO}	50	Vdc
Collector Current – Continuous	I_C	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	40	Vdc
Input Reverse Voltage	$V_{IN(rev)}$	10	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

The first spec, V_{CBO}, states that the maximum voltage that can be applied from the collector to the base is 50 V. The Collector−Emitter Voltage, V_{CEO}, spec states the maximum voltage that can be applied from the collector to emitter is 50 V. In addition, the table specifies that the maximum DC collector current (I_C) that the device can conduct is 100 mA.

There are two maximum ratings for the input voltage, forward and reverse. The input voltage is defined as the voltage applied from the base and the emitter. The maximum input forward voltage is determined from the power capabilities of the input resistor, R_1. Figure 3 and Equations 1 and 2 describe how the maximum input forward voltage is calculated when the maximum power capability of R_1 is 220 mW. It is important to use the minimum value of R_1 because it will cause the greatest power to be dissipated on the die. The minimum value of R_1 can be found in the Electrical Characteristics Table of every Digital Transistor datasheet. In this case $R_{1(min)}$ = 7 kΩ. The resulting maximum input forward voltage is 40 V. For this particular device a voltage greater than this would result in the resistor failing.

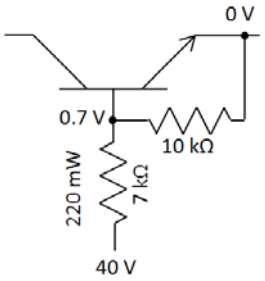

Figure 3. Input Forward Voltage

$$P_{R1} = \frac{(V_{R1})^2}{R_1} \rightarrow V_{R1} = \sqrt{P_{R1} \times R_1}$$

$$= \sqrt{0.220 \times 7000} = 39.3\ V \qquad \text{(eq. 1)}$$

$$V_{IN(max)} = V_{R1} + V_{BE} = 39.3 + 0.7 = 40\ V \qquad \text{(eq. 2)}$$

The maximum input reverse voltage is determined by the breakdown voltage of the base−emitter junction and the resistor network. The equivalent circuit in Figure 4 can be drawn when analyzing the maximum input reverse voltage and is justified by Equation 3. Looking at Figure 4 one sees that it is just a simple voltage divider. The voltage divider equation is shown in Equation 4. In applications where a large reverse voltage will be applied to the base−emitter junction it is recommended to use a Digital Transistor with a small R_2 and large R_1. This will cause the majority of the voltage to be dropped across R_1, thus a smaller voltage will be dropped across R_2 and consequently the base−emitter junction. The worst case for this spec is when R_1 is at its minimum value and R_2 is at its maximum value.

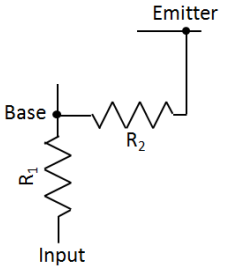

Figure 4. Input Reverse Voltage Equivalent Circuit

$$R_{Equivalent} = R_{BE}//R_2 = \left(\frac{1}{R_{BE}} + \frac{1}{R_2}\right)^{-1}$$

$$\text{When } R_{BE} \gg R_2, \frac{1}{R_{BE}} + \frac{1}{R_2} = \frac{1}{R_2} \qquad \text{(eq. 3)}$$

$$R_{Equivalent} = \left(\frac{1}{R_2}\right)^{-1} = R_2$$

$$V_B = V_E \times \left(\frac{R_1}{R_1 + R_2}\right) \qquad \text{(eq. 4)}$$

Electrical Characteristics

The first section of the Electrical Characteristics Table has specs pertaining to when the Digital Transistor is OFF. There are three leakage current parameters I_{CBO}, I_{CEO}, and I_{EBO}. For I_{CBO} and I_{CEO}, one can expect the leakage current to be below the value that is stated on the datasheet when a reverse voltage is applied between the respective junctions. However, I_{EBO} is dependent on both the input resistor and the base−emitter resistor. The resistor network path is significantly less resistive then the path through the reversed biased base−emitter junction. Ohm's Law is used to determine the I_{EBO} value. An example for a Digital Transistor with $R_{1(min)}$ = 7 kΩ, $R_{2(min)}$ = 7 kΩ, and a V_{EB} = 6 V is shown below. It is important to note that the minimum value of 7 kΩ was used instead of 10 kΩ. This is done because it will estimate the largest possible leakage.

$$I_{EBO} = \frac{6\ V}{7\ k\Omega + 7\ k\Omega} = 0.43\ mA \qquad \text{(eq. 5)}$$

Digital Transistors only specify the collector−base, $V_{(BR)CBO}$, and collector−emitter, $V_{(BR)CEO}$, breakdown voltages. These ensure that the device will have a breakdown voltage above the specified value.

The second section of the Electrical Characteristics Table describes specs for when the digital transistor is ON. Table 2 will be used as an example to help explain the following parameters. First, the DC Current Gain, h_{FE}, is a specification of how much the base current will be amplified in resulting collector current. The h_{FE} spec states that with an I_C = 5.0 mA and a V_{CE} = 10 V one can expect the gain to be around 60, but is ensured that it will be above 35. This means that the base current, I_B, will need to be 83 μA if the typical gain of 60 is used.

$$I_B = \frac{I_C}{h_{FE}} = \frac{5\ mA}{60} = 83\ \mu A \qquad \text{(eq. 6)}$$

The next parameter is the Collector−Emitter Saturation Voltage, $V_{CE(sat)}$. This parameter tells the designer the maximum voltage drop that will occur when the device is ON. In this instance a maximum of 250 mV will be dropped across the transistor when the I_C = 10 mA and the base is driven with 0.3 mA (h_{FE} = 33). The h_{FE} spec can be seen as a threshold current ratio of base drive to collector current. If the base current is greater than the collector current divided by the h_{FE} spec then the transistor begins to saturate and the collector−emitter voltage drops to the saturation voltage.

In most cases a Digital Transistor will be used as a switch. There are four parameters that characterize this operation: Input Voltage (off), Input Voltage (on), Output Voltage (on), and Output Voltage (off). The first parameter, Input Voltage (off), states that an input voltage less than 0.8 V will turn the device OFF (V_{CE} = 5 V, I_C = 100 μA). The Input Voltage (on) parameter defines that at a V_{CE} = 0.3 V and I_C = 10 mA a minimum input voltage of 2.5 V needs to be applied to turn the device ON. These two parameters also list typical values. These typical values are the measured voltages when the device is exactly at those ON and OFF conditions. It is not recommended to operate the device at these voltages if one wants to ensure the device is ON/OFF. Figure 5 gives a graphical representation of these specs.

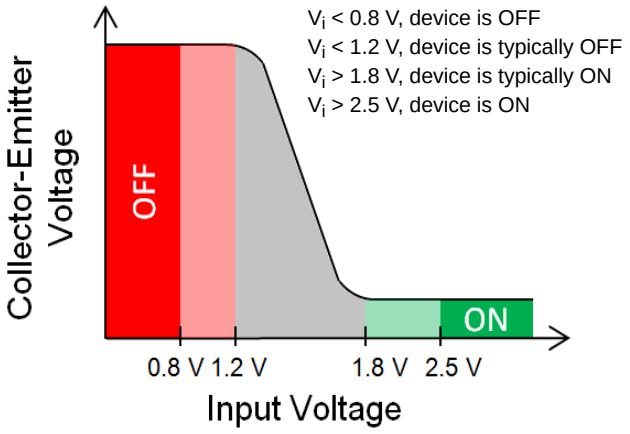

Figure 5. Output Voltage vs. Input Voltage

The output voltage of a switch is also very valuable to a designer. The Output Voltage (on), V_{OL}, spec states that the output voltage will be less than 0.2 V under the following conditions: V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ. The V_{OL} is similar to the $V_{CE(sat)}$ of the device in that they both describe the maximum voltage that will be dropped across the collector−emitter when the Digital Transistor is in saturation(ON). The conditions for the Output Voltage (off), V_{OH}, spec are: V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ. Under these conditions the output voltage will be greater than 4.9 V. Refer to Figure 6 for further understanding of the V_{OL} and V_{OH} specs.

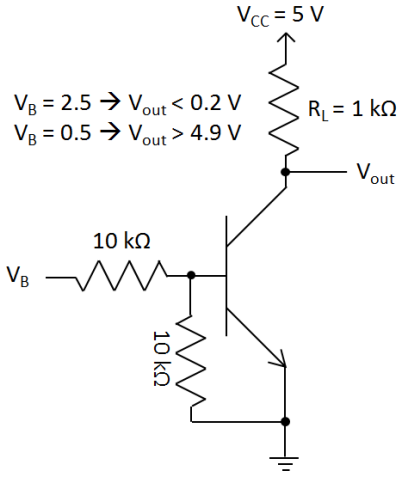

Figure 6. Output Voltage Test Schematic

Table 2. ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current (V_{EB} = 6 V, I_C = 0)	I_{EBO}	−	−	0.5	mAdc
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	−	−	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 5.0 mA, V_{CE} = 10 V)	h_{FE}	35	60	−	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)	$V_{CE(sat)}$	−	−	0.25	Vdc
Input Voltage (off) (V_{CE} = 5.0 V, I_C = 100 μA)	$V_{i(off)}$	−	1.2	0.8	Vdc
Input Voltage (on) (V_{CE} = 0.3 V, I_C = 10 mA)	$V_{i(on)}$	2.5	1.8	−	Vdc
Output Voltage (on) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	−	−	0.2	Vdc
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)	V_{OH}	4.9	−	−	Vdc
Input Resistor	R_1	7.0	10	13	kΩ
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

There are two curves present on all Digital Transistor datasheet that provide more data on the $V_{i(on)}$ and $V_{i(off)}$ parameters. The first is the Output Current vs. Input Voltage, Figure 7. This curve characterizes the $V_{i(off)}$ parameter, and the data was taken when the V_{CE} or the output voltage is 5 V. One can use this curve to determine at what voltage the current will drop rapidly, or in other words turn OFF. For this device the voltage at which the current rapidly drops off is around 1.4 V at 25°C.

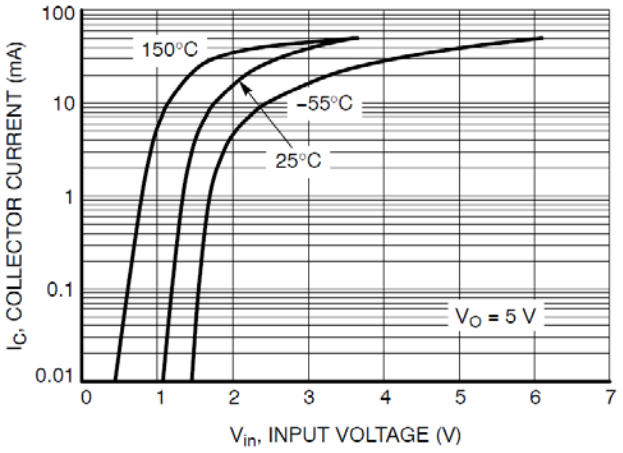

Figure 7. Output Current vs. Input Voltage

The other datasheet curve is the Input Voltage vs. Output Current, Figure 8. This curve characterizes the $V_{i(on)}$ parameter and the data was taken with the V_{CE} = 0.2 V. This chart provides the designer the voltage needed for a desired collector current while maintaining an output voltage of 0.2 V. For example, to operate the device characterized in Figure 8 at an I_C of 30 mA and a V_{CE} of 0.2 V, an input voltage of 5.3 V would need to be applied.

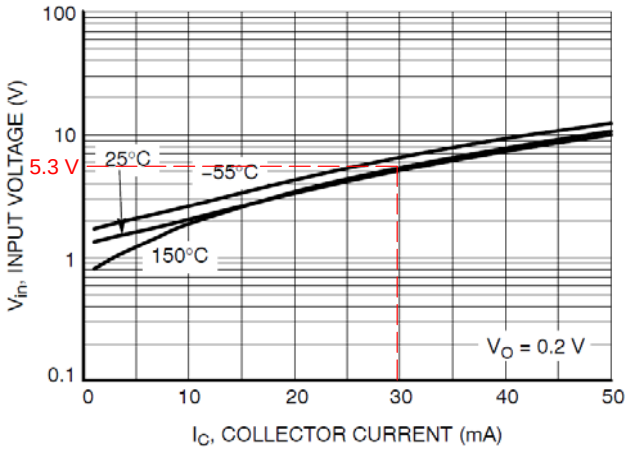

Figure 8. Input Voltage vs. Output Current

The last two parameters describe the built in resistors of the Digital Transistor. First, is the typical R_1 value along with the minimum and maximum values that are ±30% of the typical value. The typical resistor ratio of R_1/R_2 is also defined along with a minimum and maximum spec of ±20% of the typical value. The actual value of R_2 is not defined because the ratio of R_1/R_2 is more pertinent when designing with Digital Transistors. The R1/R2 ratio is what controls the critical parameters of the Digital Transistor. However, if desired it is possible to calculate the minimum and maximum values of R_2. Equations 7 and 8 help explain how to do this using the values in Table 2.

$$R_{2(min)} = \frac{R_{1(min)}}{(R_1/R_2)_{max}} = \frac{7\ k\Omega}{1.2} = 5.8\ k\Omega \quad \text{(eq. 7)}$$

$$R_{2(max)} = \frac{R_{1(max)}}{(R_1/R_2)_{min}} = \frac{13\ k\Omega}{0.8} = 16.3\ k\Omega \quad \text{(eq. 8)}$$

Example of Designing with Digital Transistor Datasheet

Design requirements:

Polarity: NPN

I_C = 10−20 mAdc

$V_{CE(max)} = V_{CB(max)}$ = 40 Vdc

$V_{IN(fwd)}$ = 20 Vdc

$V_{IN(rev)}$ = 10 Vdc

Micro controller output voltage:

Off: 0.4−0.6 V

On: 1.5−4.2 V

Micro controller max output current: 250 μA

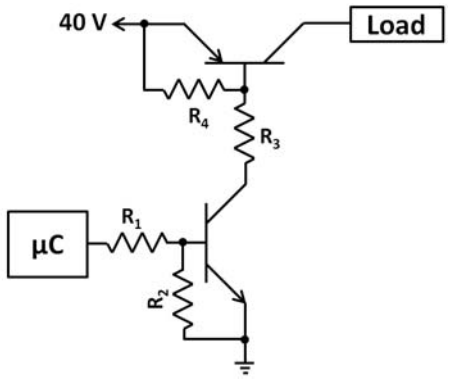

Figure 9. Schematic for Example

Now that the design requirements have been established it is time to indentify the Digital Transistor that works best for the application. Table 3 will help with this selection. The first step should be to find a Digital Transistor that meets the max current and voltage requirements. The majority of Digital Transistors within ON Semiconductors portfolio are rated at 100 mA. The remaining Digital Transistors are rated above 100 mA. Also, the majority of them have a V_{CEO} and V_{CBO} of 50 V, which will meet the above requirement.

Next, is to find a Digital Transistor that meets the forward and reverse input voltage requirements. Using Table 3 it is seen that the $V_{IN(fwd)}$ requirement of 20 V is reached by all digital transistors except for ones that have a R_1 of 1 kΩ or 2.2 kΩ. Digital Transistors with a $R_1/R_2 \geq 1$ will meet the 10 V requirement for $V_{IN(rev)}$.

The next requirement to look at is $V_{i(off)}$. In the design requirements it states that the micro controller will give a voltage of 0.4−0.6 V when it wants the Digital Transistor to be OFF. This eliminates the Digital Transistors that have a maximum $V_{i(off)}$ spec of 0.5 V because these should be supplied with a voltage of less than 0.5 V when the device is desired to be OFF.

The design requirements also state that the maximum output voltage of the micro controller is 4.2 V. A Digital Transistor needs to be selected that can provide a maximum I_C of 20 mA when the input voltage is 4.2 V. It also has to provide an I_C of 10 mA with an input voltage of greater than 1.5 V. Looking at the Input Voltage vs. Output Current charts of the four remaining Digital Transistors only two meet the input voltage requirements. They are the Digital Transistors with R_1/R_2 = 10 kΩ/10 kΩ and 22 kΩ/22 kΩ.

It is also important to consider the max output current of the controller. In this case the micro controller can source a maximum of 250 μA. For the 10 kΩ/10 kΩ digital transistor the typical voltage needed to drive an I_C of 20 mA is 3.3 V. In this case the micro controller would have to source approximately 260 μA which is above the max output current of the micro controller.

$$\frac{3.3\ V - 0.7\ V}{10\ k\Omega} = 260\ \mu A \qquad \text{(eq. 9)}$$

However, for the 22kΩ/22kΩ the typical voltage needed for an I_C of 20 mA is 3.8 V resulting in a current of 140 μA.

$$\frac{3.8\ V - 0.7\ V}{22\ k\Omega} = 140\ \mu A \qquad \text{(eq. 10)}$$

After considering all the design requirements it is found that the Digital Transistor that will work best for this specific application is the Digital Transistor with R_1/R_2 = 22 kΩ/22 kΩ. The final step would be to pick the package. ON Semiconductor offers single Digital Transistors in six packages ranging from SC−59 to SOT−1123.

Table 3. INPUT VOLTAGE SPECIFICATIONS

		$V_{IN(fwd)}$ (V)		$V_{IN(rev)}$ (V)		$V_{i(on)}$ (V)		$V_{i(off)}$ @ 0.1 mA (V)	
R1 (kΩ)	R2 (kΩ)	PNP	NPN	PNP	NPN	PNP	NPN	PNP	NPN
1	1	10	10	10	10	2.0 @ 20 mA	2.0 @ 20 mA	0.5	0.5
2.2	2.2	12	12	10	10	2.0 @ 20 mA	2.0 @ 20 mA	0.5	0.5
4.7	4.7	30	30	10	10	3.0 @ 20 mA	2.5 @ 20 mA	0.5	0.5
10	10	40	40	10	10	2.5 @ 10 mA	2.5 @ 10 mA	0.8	0.8
22	22	40	40	10	10	2.5 @ 5 mA	2.5 @ 5 mA	0.8	0.8
47	47	40	40	10	10	3.0 @ 2 mA	3.0 @ 2 mA	0.8	0.8
100	100	40	40	10	10	3.0 @ 1 mA	3.0 @ 1 mA	0.5	0.5
2.2	47	12	12	5	6	1.1 @ 5 mA	1.1 @ 5 mA	0.5	0.5
4.7	47	30	30	5	6	1.3 @ 5 mA	1.3 @ 5 mA	0.5	0.5
10	47	40	40	6	7	1.4 @ 1 mA	1.4 @ 1 mA	0.5	0.5
22	47	40	40	7	8	2.0 @ 2 mA	2.0 @ 2 mA	0.5	0.5
47	22	40	40	10	10	4.0 @ 2 mA	4.0 @ 2 mA	1.2	1.2
2.2	Inf.	12	12	5	6	1.3 @ 10 mA	1.1 @ 10 mA	0.5	0.5
4.7	Inf.	30	30	5	6	1.3 @ 10 mA	1.3 @ 10 mA	0.5	0.5
10	Inf.	40	40	5	6	1.7 @ 10 mA	1.7 @ 10 mA	0.5	0.5
47	Inf.	40	40	5	6	4.0 @ 10 mA	4.0 @ 10 mA	0.5	0.5
100	Inf.	40	40	5	6	1.5 @ 1 mA	1.5 @ 1 mA	0.5	0.5

Conclusion

Throughout this application note the characteristics of Digital Transistors have been discussed. These characteristics range from the maximum ratings to the input/output characteristics. It was shown how the resistor network of Digital Transistors determines the input voltage characteristics. ON Semiconductor understands that having a variety of resistor combinations is pivotal in helping designers fulfill their design requirements. This is why ON Semiconductor has worked to provide a complete portfolio of Digital Transistors. Please visit www.onsemi.com to explore ON Semiconductor's Digital Transistor Portfolio.

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