AND9127/D

IGBT Ruggedness

ON Semiconductor®

www.onsemi.com

APPLICATION NOTE

Introduction

This application note examines methods of evaluating the ruggedness of IGBTs offered by ON Semiconductor. The three measures discussed are the gate voltage rating, the short circuit rating and the UIS rating. Results of device testing will be reviewed and the applicability of the various tests will be explained.

Measures of Ruggedness

There are several measurements that can be used to quantify the ruggedness of an IGBT. They include the short circuit rating, the UIS rating and the gate voltage rating. All of these measures cover a different area of operation and combined, they can give insight into the survival of the IGBT during an abnormal transient event as well as provide operating limits to assure high reliability of the device.

Gate Voltage Rating

The maximum gate voltage rating is given in the Absolute Maximum Ratings table near the beginning of the data sheet. The maximum steady-state rating will be given in this table and in many cases a transient rating will also be included.

ABSOLUTE MAXIMUM RATINGS

Table 1. ABSOLUTE MAXIMUM RATINGS EXAMPLE OF GATE–EMITTER VOLTAGE TRANSIENT RATING

Rating	Symbol	Value	Units
Collector-emitter Voltage	V_{CES}	1200	V
Collector Current @ T_C = 25°C @ T_C = 100°C	I_C	 40 20	A
Pulsed Collector Current, T_{pulse} Limited by T_{Jmax}	I_{CM}	80	A
Diode Forward Current @ T_C = 25°C @ T_C = 100°C	I_F	 40 20	A
Diode Pulsed Current, T_{pulse} Limited by T_{Jmax}	I_{FM}	80	A
Gate-emitter Voltage Transient Gate-emitter Voltage (T_{pulse} = 5 μs, D < 0.10)	V_{GE}	±20 ±25	V
Power Dissipation @ T_C = 25°C @ T_C = 100°C	P_D	 333 167	W
Operating Junction Temperature Range	T_J	−40 to +175	°C
Storage Temperature Range	T_{stg}	−55 to +175	°C
Lead Temperature for Soldering, 1/8″ from Case for 5 s	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Ideally, the gate drive pulse should be a square wave with no overshoot; however, this is rarely the case. Due to electrical transients from the high di/dts combined with the parasitic capacitances and inductances in the system, transients often occur between the gate and emitter. The gate-emitter voltage rating specifies the amplitude and duration of this pulse; both the DC level and transient spike.

The voltage across the dielectric, between the gate and emitter can cause tunneling of carriers through the dielectric if it exceeds the leakage limit, especially where imperfections (traps) exist. This tunneling creates heat, which if allowed to continue for a sufficient period of time, can cause damage to the oxide which in turn creates more traps. This process can quickly increase to the point where

© Semiconductor Components Industries, LLC, 2016

significant damage occurs in the gate oxide. It should be apparent that at higher gate voltages it is necessary to limit the duration of the event to assure that the temperature rise due to the tunneling electrons does not exceed a safe level. If the oxide becomes hot enough to cause damage, that damage will be cumulative. This is why both the time and duty ratio of the transient event are included on the data sheet. Over a period of time this damage can cause the threshold to shift lower which may cause improper operation of the circuit or in extreme cases can cause a failure of the gate oxide.

ON Semiconductor IGBTs are tested in qualification testing, at levels well above the transient voltage rating to assure that this is a safe transient level for the gate-to-emitter voltage.

The DC rating is a very conservative gate voltage level and no tunneling or other degradation will occur at or below that operational level.

Short Circuit Rating

Some IGBTs have short circuit ratings while others do not. This is based on the industry demand per the specific application that each IGBT is designed for.

Some industry standard short circuit requirements are:

Motor Drives: 5 – 10 μs
White Goods: 5 μs
UPS: 0 – 5 μs
Solar Inverters: 10 μs
PFC Converters: 10 μs

This parameter is tested by applying a fixed voltage across the collector-to-emitter terminals and then biasing the gate on. For example, to evaluate a 600 volt IGBT, it is typical to apply from 300 to 400 volts from the collector-to-emitter terminals, and then bias the gate at 15 volts. The IGBT is mounted on a heat sink and stabilized at a high temperature for this test.

This is equivalent to a short circuit condition in a power converter. The short circuit rating is the time that the device can withstand the enormous power being delivered to it before it fails.

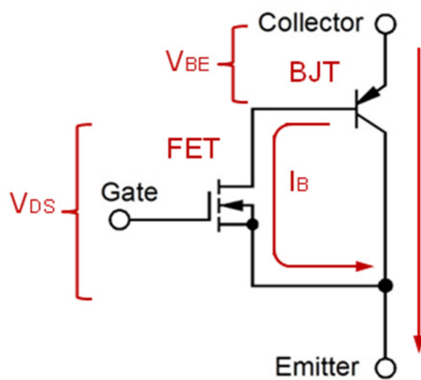


Figure 1. IGBT Current Flow

The failure mode for this test is the heating of the die to the point where it no longer functions as a semiconductor. It is a fairly simple thermodynamics problem. Power is pumped into the die and its temperature increases based on the thermal mass of the die to the failure point.

To increase the short circuit time, it is necessary to reduce the power delivered to the IGBT die during the event so that the heating occurs more slowly. Since the collector-emitter voltage and the gate-emitter voltage are fixed during the test, the only way to reduce the power is to reduce the current under the required conditions.

In order to control the current leve, the transconductance of the MOSFET is adjusted. Figure 1 shows the current flow through the BJT and FET which comprise an IGBT. When the FET is enhanced, it provides base drive to the pnp power transistor. Lowering the Rds(on) of the FET (increasing the transconductance) provides more base current to the BJT for a given V_{CE}.

High transconductance is generally desirable as it provides the lowest V_{CE}(sat) for an IGBT. At the same time, it also allows for more current to flow in the BJT under a short circuit condition. By decreasing the transconductance of the FET, the base drive current to the BJT is reduced and therefore the collector current is also reduced.

This in turn, reduces the overall power dissipation of the IGBT and increases the time that it can withstand a short condition without damage. Since lower transconductance equates to a higher Rds(on) for the MOSFET, the short circuit rating is increased at the expense of the V_{CE}(sat) rating.

ABSOLUTE MAXIMUM RATINGS

Table 2. ABSOLUTE MAXIMUM RATINGS EXAMPLE OF SHORT CIRCUIT RATING

Rating	Symbol	Value	Units
Collector-emitter Voltage	V_{CES}	600	V
Collector Current @ T_C = 25°C @ T_C = 100°C	I_C	 30 15	A
Pulsed Collector Current, T_{pulse} Limited by T_{Jmax}	I_{CM}	120	A
Diode Forward Current @ T_C = 25°C @ T_C = 100°C	I_F	 30 15	A
Diode Pulsed Current, T_{pulse} Limited by T_{Jmax}	I_{FM}	120	A
Gate-emitter Voltage	V_{GE}	±20	V
Power Dissipation @ T_C = 25°C @ T_C = 100°C	P_D	 117 47	W
Short Circuit Withstand Time V_{GE} = 15 V, V_{CE} = 400 V, $T_J \leq$ +150°C	t_{SC}	5	μs
Operating Junction Temperature Range	T_J	–55 to +150	°C
Storage Temperature Range	T_{stg}	–55 to +150	°C
Lead Temperature for Soldering, 1/8″ from Case for 5 s	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

UIS Rating

While a UIS (Unclamped Inductive Spike) rating is common for MOSFETs, it is not often used with IGBTs. This may be due to the slower switching speeds which generate lower voltage spikes, but in any event, this rating does offer some insight as to the capacity of the IGBT to absorb energy in an avalanche condition.

It should be noted that even though this seems like a redundant rating to the short circuit rating, there is a major difference in the ability of the die to deal with the energy. In the short circuit condition, the IGBT is on (gate drive is applied). Under this condition the current distribution across the surface of the die is quite uniform and the ability of the die to dissipate the energy is maximized.

In a UIS condition, the IGBT is in a non-conducting state, with no bias on the gate. Since the cells of the IGBT are not conducting, when an avalanche occurs, the current tends to conduct around the perimeter of the die, so there is not a uniform current distribution across the surface of the die. In this case, the maximum current to failure is much less than in the short circuit condition. Even though uniform current distribution does not occur, the size of the die is still the main parameter that determines the UIS for that die.

This situation becomes more complicated in the case of a co-packaged IGBT and diode. In most co-packaged devices, the diode die is smaller than the IGBT die. When a UIS event occurs, the die with the lower breakdown voltage will take most or all of the energy and will determine the UIS capability of the device. If a small diode with a lower breakdown voltage than that of the IGBT is used, the UIS rating will be that of the diode and will be considerably reduced from that of the IGBT alone.

The circuit of Figure 2 is used to test UIS. Figure 3 shows the waveforms associated with the test circuit.

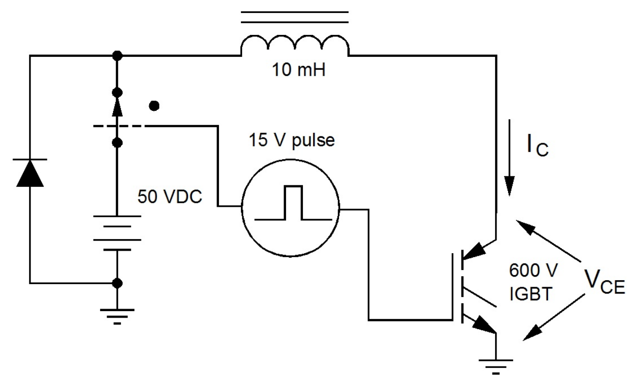


Figure 2. UIS Test Circuit

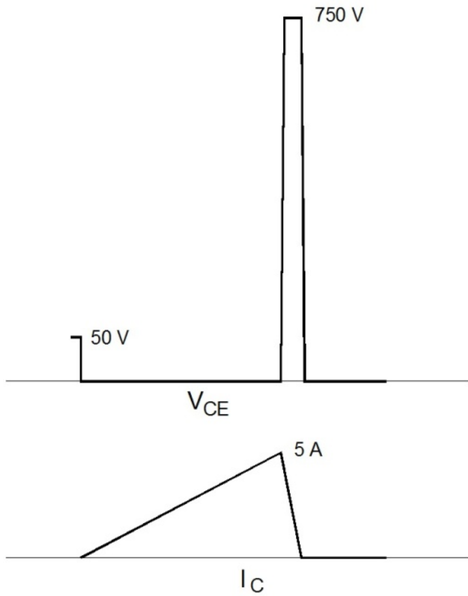


Figure 3. UIS Test Waveforms

When a pulse is applied to the gate of the IGBT, the current in the inductor ramps up, storing energy in the inductor. When the IGBT is turned off, the voltage on its collector increases to the breakdown point at which time the device avalanches and the energy from the inductor is transferred to the IGBT. If the IGBT is not damaged, the current is increased by a small increment and the test is repeated until failure. The highest energy level measured before failure is the rated UIS energy.

In this example, a 600 volt rated IGBT is connected to a 50 volt DC supply through a 10 mH inductor. The current is ramped to 5 amps and then the IGBT is turned off. The avalanche voltage for this part is 750 volts. The energy dissipated in the IGBT is that of the inductor, which can be calculated by the equation:

$$E_L = 1/2 \times L \times I^2$$

$$E_L = E_{IGBT} = 1/2 \times 10\ \text{mH} \times 5^2 = 125\ \text{mJ}$$

At this point, the device would be allowed to cool, and then would be retested at a higher current level.

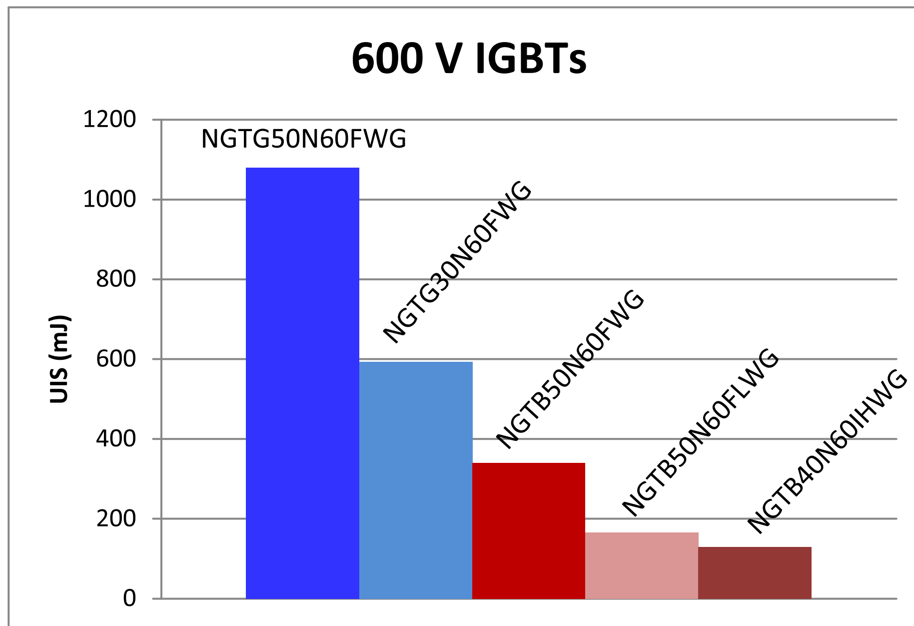


Figure 4. UIS Ratings for ON Semiconductor 600 Volt IGBTs

Figure 4 shows the UIS ratings for several 600 volt IGBTs, produced by ON Semiconductor. All of these devices can dissipate considerable amounts of energy in an avalanche condition.

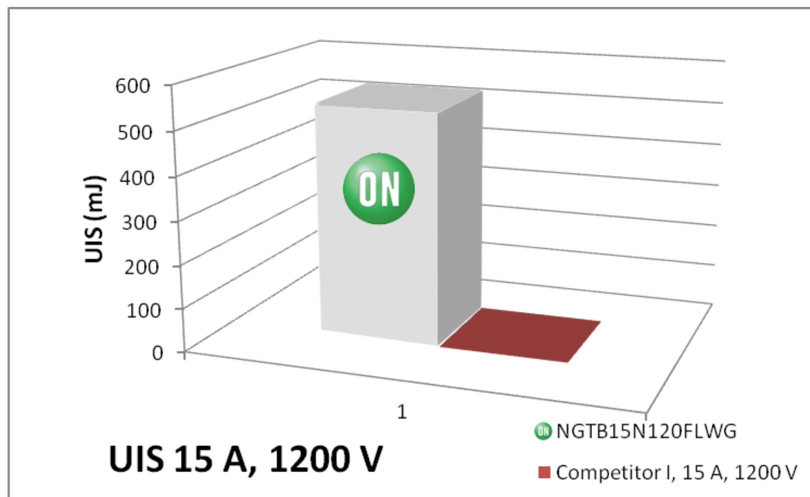


Figure 5. UIS Ratings for Competitive 1200 V IGBTs

Figure 5 demonstrates that for IGBTs with equivalent voltage and current ratings, the UIS can be significantly different. The UIS rating of the ON Semiconductor part is 537 mJ, while the competing device is 0.42 mJ. In the case, the main difference is that the competitive part has a very small diode that breaks down at a lower voltage than that of the IGBT. In this situation the ON Semiconductor part will be much more robust if an avalanche event occurs, with a very high probability of survival, while the other part would probably not survive the event.

An example of this situation would be use in an inductive heating, quasi-resonant converter. This type of converter is connected directly to the building power, which is then rectified and directly boosted at the power stage, with only a minimal EMI filter between the two points. If a transient occurs on the power line, due to a load dump, that transient will be imposed on the collector of the IGBT. The ON Semiconductor part will have a high probability of withstanding such a surge and the competitive device would most likely fail.

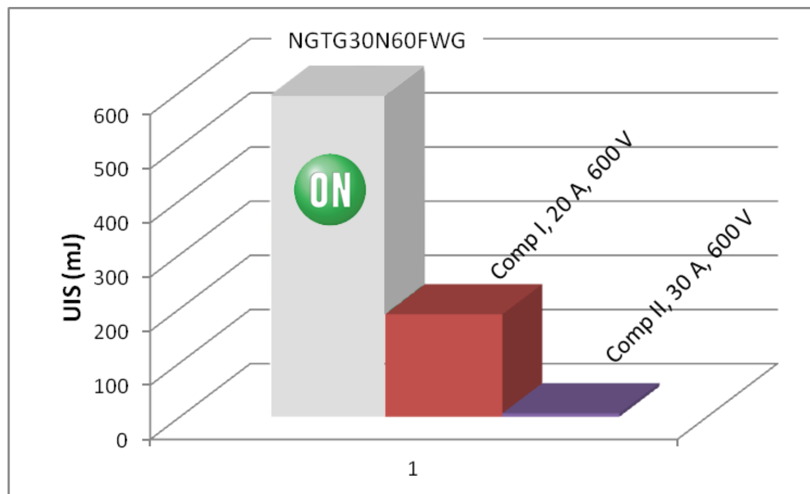


Figure 6. UIS Ratings for Competitive 600 V IGBTs

Figure 6 shows the UIS results for several 20 and 30 amp, 600 volt IGBTs. Again, there is a large difference in the UIS ratings for these devices.

Current Trends (wafer thinning)

As IGBT processes evolve, one trend that is dominant is that the thickness of the wafers is decreasing. This is done due to several advantages of a thinner die. One is that the thermal properties are improved. The thermal path from the active area on the die to the flag of the lead frame is shortened and the temperature drop between the mounting flag of the case and active die area is therefore, reduced.

Reducing the thickness of the die also reduces the parasitic capacitances associated with the device. This reduces the drive requirements and speeds up the switching speeds. It also reduces the V_{CE}(sat) of the device. All of the major losses associated with an IGBT, (switching, conduction, drive) are reduced by the use of thinner wafers.

The 600 volt IGBTs manufactured by ON Semiconductor have recently been reduced from 3.8 mils to 2.8 mils. The 1200 volt IGBTs have been reduced from 6.5 mils to 5.0 mils. It should be obvious, that higher voltages require a thicker device to withstand that voltage which is why the 1200 volt IGBTs are almost twice as thick as the 600 volt IGBTs.

In order to withstand higher voltages, IGBTs have moved to a field stop design. In this type of structure, the n buffer is highly doped with phosphorus which rapidly reduces the electric field. The field must go to zero before it reaches the boron doped p+ substrate on the back side of the die.

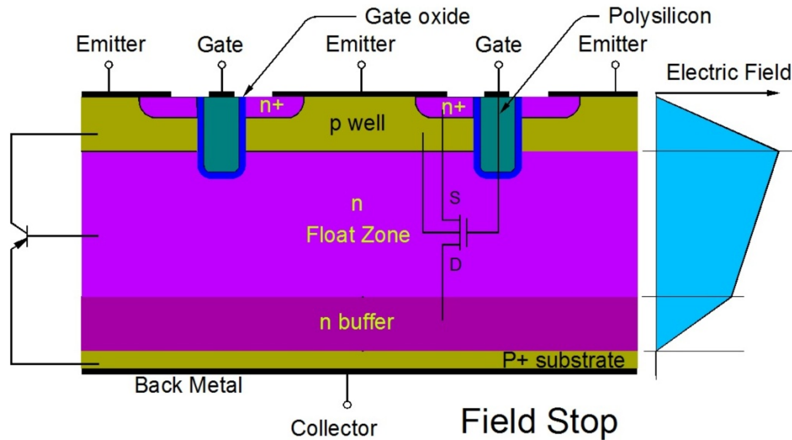


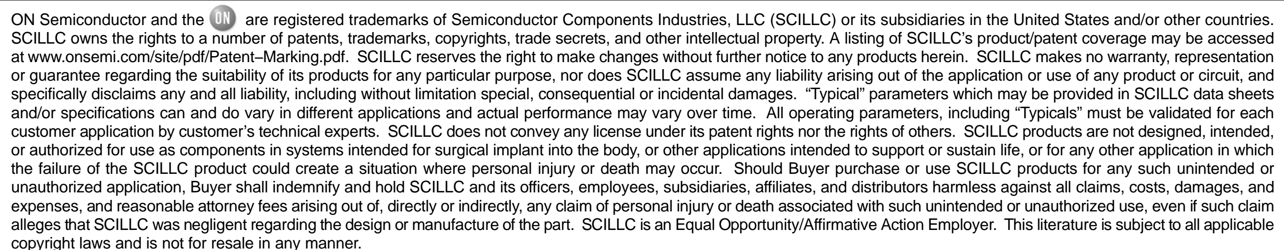
Figure 7. Field Stop IGBT Diagram

Substantial testing is conducted to assure that doping levels are adequate to stand off the rated voltage of the IGBT. This is all to assure that thinner IGBTs will be as reliable as the older, thicker devices, while offering the advantages of the thinner wafer.

Conclusion

Three measures of quantitative ruggedness for IGBTs have been explained. The gate voltage rating is an indication of the devices tolerance to the voltage stresses induced on the gate oxide by the gate-to-emitter voltage. The short circuit rating is a measure of the ability of an IGBT to withstand a surge of energy while the device is conducting current which is distributed evenly across the surface of the die. The UIS rating is a measure of the ability of the IGBT to withstand a surge of energy in an avalanche condition where current crowding near the edge of the die occurs. These three parameters offer a solid basis for evaluation of the ruggedness of an IGBT. Exceeding any of these ratings will have a negative effect on the reliability and lifetime of the device.

In addition, the issue of wafer thinning has been discussed, and the voltage stresses across the thickness of the die explained. Wafer thickness does not decrease the reliability or lifetime of the device.


ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent–Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5817–1050

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative