AND9108/D

M-BUS Design Changes Between TSS721A and NCN5150

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APPLICATION NOTE

NCN5150 is a drop in replacement of the TSS721A for all designs using a VDD capacitor larger than 1 μF. The NCN5150 M−BUS transceiver (in SOIC version) is pin−to−pin compatible with the TSS721A from Texas Instruments™ and can replace this component with no changes to the PCB layout on a typical implementation. Some minor differences between both parts are detailed in this document.

Summary of Differences

- No transistor required on STC for fast start−up
- Minimum required decoupling capacitance on VDD

External PMOS Transistor on STC

The TSS721A requires an external PMOS transistor (BSS84) in series with the STC capacitor if this capacitor is larger than 50 μF in order to meet the maximum start−up time requirement by the M−BUS standard. The NCN5150 does not require this transistor (Q_{STC}), and allows the STC capacitor to be connected directly to the STC pin. Optionally, for existing PCB layouts where no possibility exists to bypass the transistor footprint, the transistor can be kept in place without any problem.

VDD Decoupling Capacitor

The NCN5150 requires a minimum total decoupling capacitance (C_{VDD}) of 1 μF on the output of the 3.3 V regulator to remain stable. Typical designs with the TSS721A will use a 100 nF capacitor.

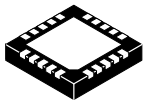
Related Standards:

European Standard

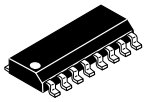
EN 13757−2
EN 1434−3

For more information visit www.m−bus.com

PACKAGE PICTURES

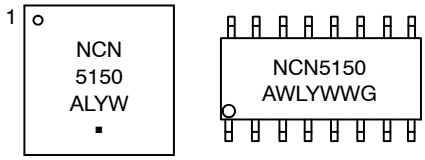


QFN20
CASE 485E



SOIC−16
CASE 751B−05

MARKING DIAGRAMS



A = Assembly Location
(W)L = Wafer Lot
YW(W) = Year / Work Week
G / ▪ = Pb-Free Package

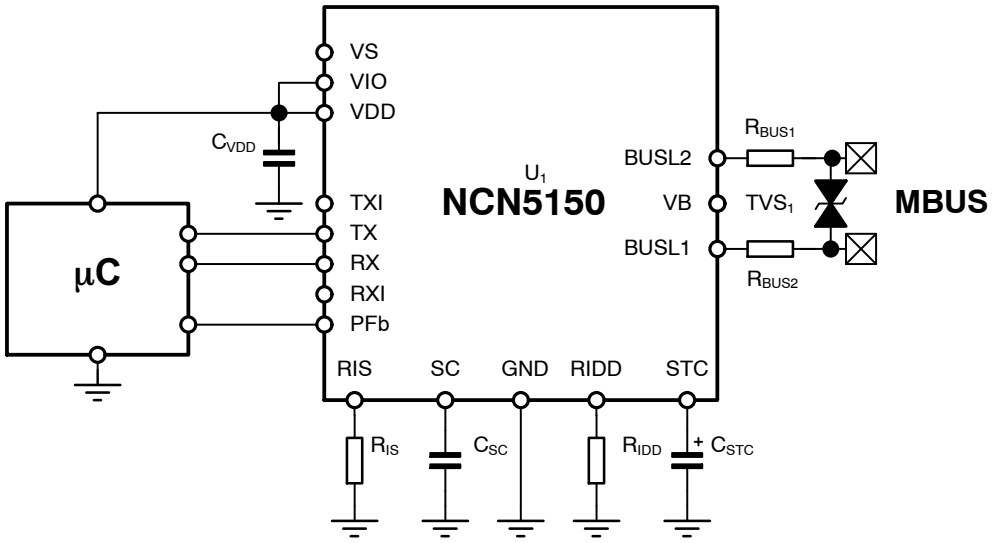


Figure 1. General Application Schematic – NCN5150

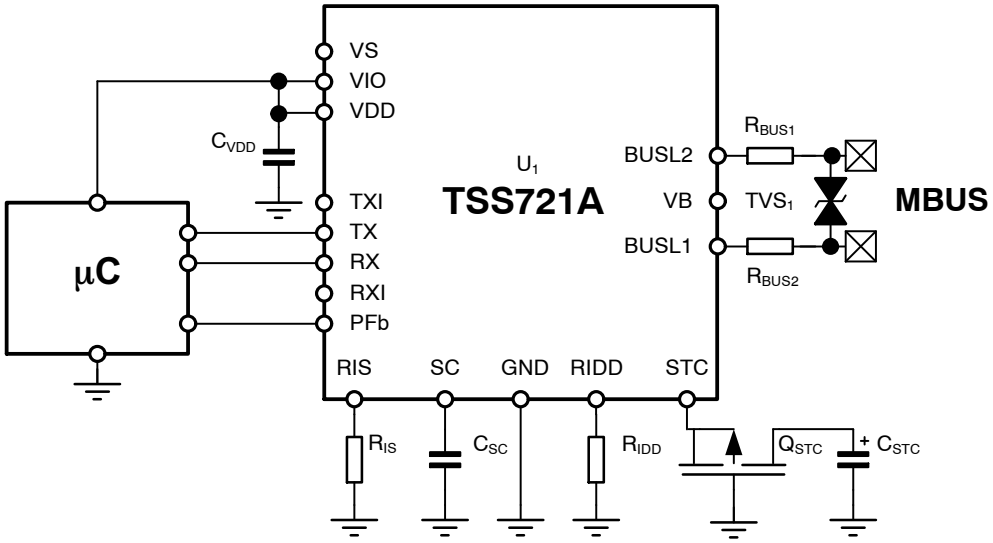


Figure 2. General Application Schematic – TSS721A

Table 1. GENERAL APPLICATION SCHEMATIC BOM DIFFERENCES

Reference Designator	TSS721A	NCN5150
U_1	TSS721A	NCN5150
C_{VDD}	100 nF	1 µF
R_{IS}	100 Ω	100 Ω
R_{IDD}	30 kΩ (1UL) 13 kΩ (2UL)	30 kΩ (1UL) 13 kΩ (2UL)
C_{SC}	220 nF (typ.)	220 nF (typ.)
Q_{STC}	BSS84L	BSS84L (optional)
C_{STC}	up to 470 µF	up to 470 µF
R_{BUSL1}, R_{BUSL2}	220 Ω	220 Ω
TVS1	1SMA40CAT3G	

Start-up and Shut-down

Shown in figures 3, 4, 5 and 6 is the start-up and shutdown of the NCN5150 next to the corresponding waveforms captured from the TSS721A (both with and without STC transistor). We can see clearly that the startup of the TSS721A is much longer without the STC transistor, and will not comply with the M-BUS standard defined maximum start-up time of 3 s for the same STC capacitor value. The solution in this case is to add an extra PMOS in series with the STC capacitor.

While this technique reduces the startup to similar time as the NCN5150 at the cost of an extra component, it also causes a 700 mV step on VDD if no load is present on VDD. If a sufficient external load is present, this step will not occur, however in this case a strange effect can be seen on PF, where this pin rises along with the STC voltage until the VDD regulator is turned on, as shown in figure 6. This can cause the PF pin to rise above the recommended voltage rating of the microcontroller it is connected to. During start-up of the NCN5150 no unwanted step is present on VDD and all of the IO pins are turned on only when VDD is turned.

Shutdown of both components is shown in figures 7, 8 and 9. We can see the PFb pin (green) go from logic high to low. This happens immediately after the bus voltage collapses. The VDD is disconnected later. All these figures were taken with an external load on VDD, because otherwise the VDD capacitor would retain its charge for a long time.

However, when the load on VDD is removed after the voltage has collapsed (as is the case for digital circuits) the TSS721A will charge back to ~300 mV, which can be undesirable for certain circuits. The NCN5150 does not have this behavior.

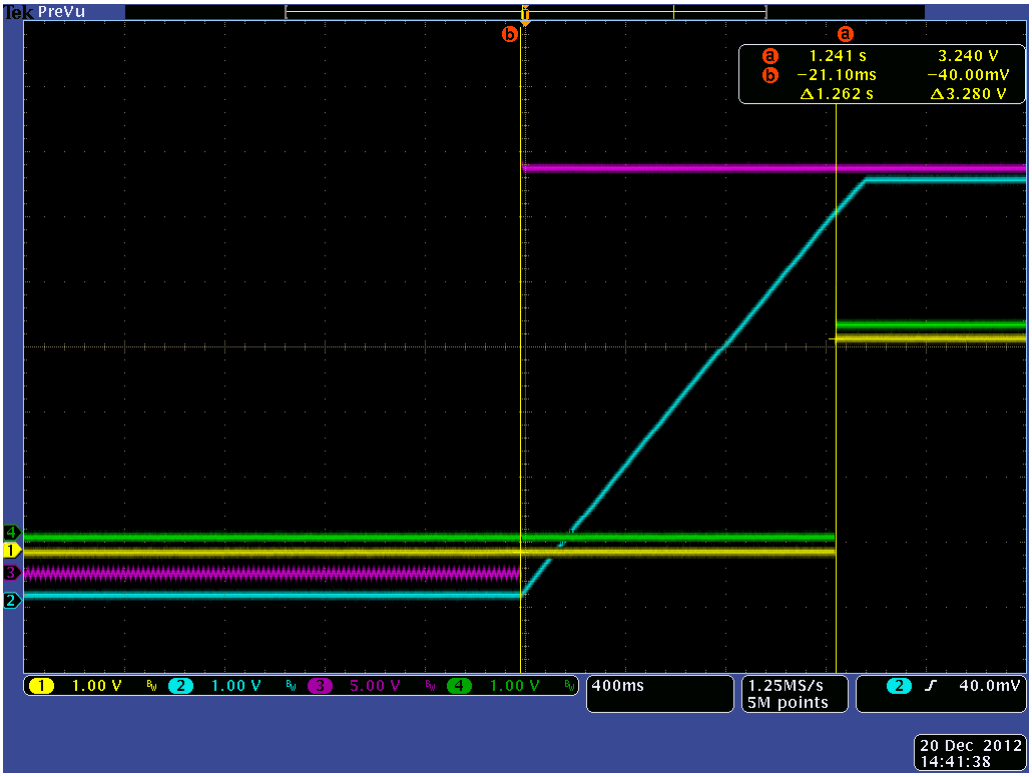


Figure 3. NCN5150 Startup (C_{STC} = 220 μF, 1 Unit Load, no STC transistor) (purple = BUSL1, blue = STC, yellow = VDD, green = PFb)

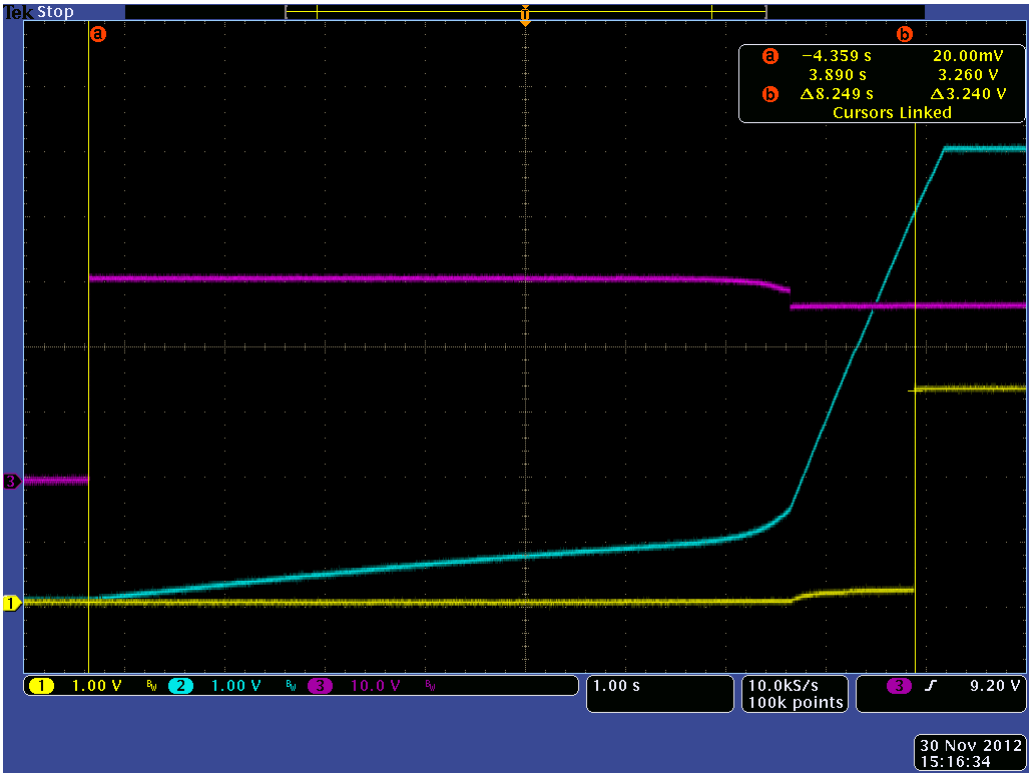


Figure 4. TSS721A Startup (C_{STC} = 220 μF, 1 Unit Load, no STC transistor)
(purple = BUSL1, blue = STC, yellow = VDD)

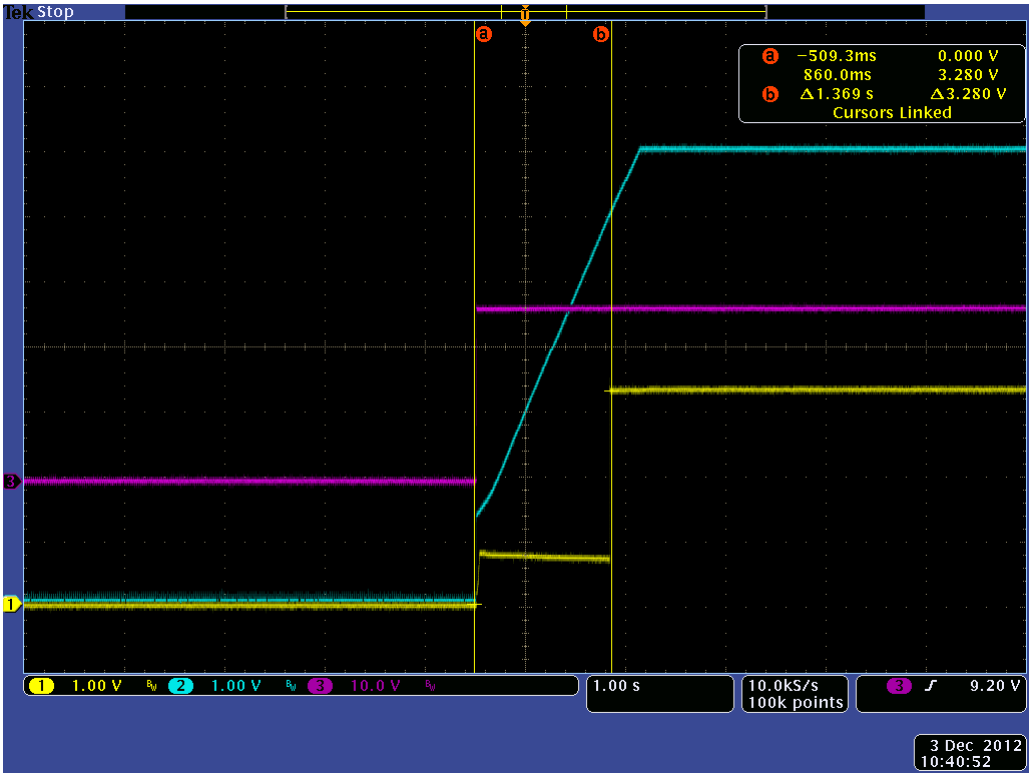


Figure 5. TSS721A Startup (C_{STC} = 220 μF, 1 Unit Load, BSS84L, no external load)
(purple = BUSL1, blue = STC, yellow = VDD)

Figure 6. TSS721A Startup (C_{STC} = 220 μF, 1 Unit Load, BSS84L, external load of 8 kΩ) (purple = BUSL1, blue = STC, yellow = VDD, green = PFb)

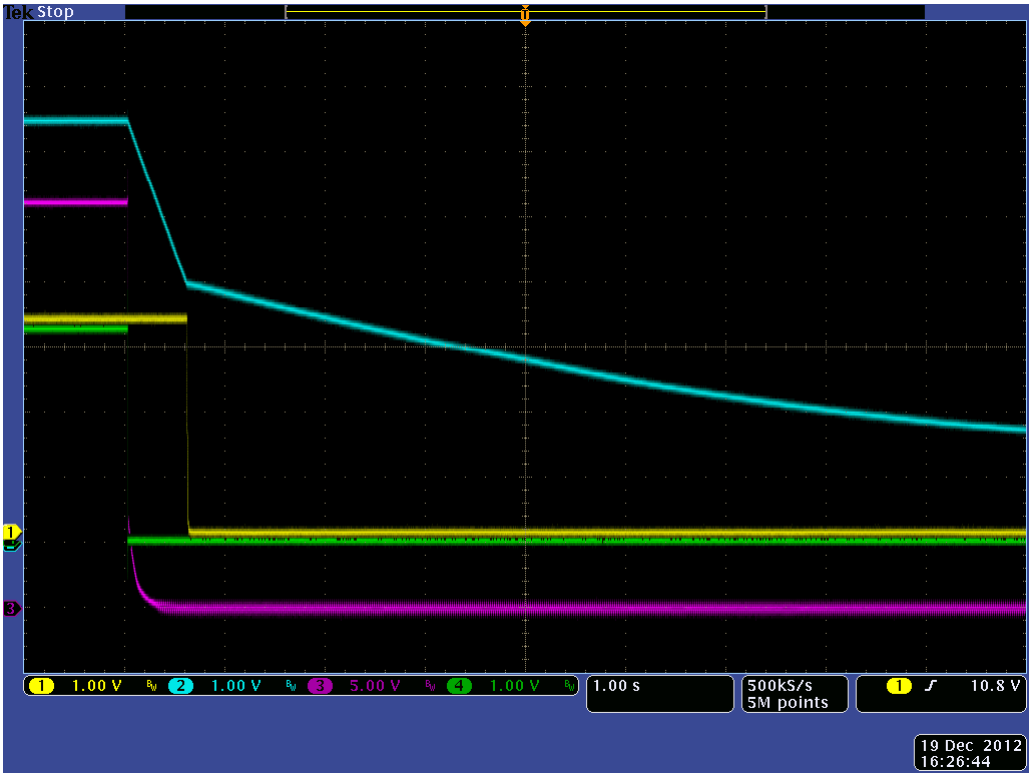


Figure 7. NCN5150 Shutdown (C_{STC} = 220 μF, 1 Unit Load, external load of 8 kΩ) (purple = BUSL1, blue = STC, yellow = VDD, green = PFb)

Figure 8. TSS721A Shutdown (C_{STC} = 220 μF, 1 Unit Load, external load of 8 kΩ) (purple = BUSL1, blue = STC, yellow = VDD, green = PFb)

Figure 9. TSS721A Shutdown (C_{STC} = 220 μF, 1 Unit Load, external load of 8 kΩ disconnected on shutdown) (purple = BUSL1, blue = STC, yellow = VDD, green = PFb)

Minimum STC capacitor value

For applications where the external circuit is not powered by the bus, it can make sense to choose a low value capacitor for STC. The lower limit on this capacitor is determined by two factors that apply equally to the TSS721A and the NCN5150.

The first lower limit is determined by the charge transfer to the VDD capacitor when the device is starting up. To achieve a clean startup, the voltage drop incurred by this charge transfer should not cause the STC voltage to drop below the turn-off threshold.

For both parts, this limits the STC voltage drop ΔV_{STC} to 1.3 V. This leads us to a minimum ratio between the capacitor values on VDD and STC of:

This equation does not take into account the tolerances on capacitor value, which can be up to −80% or +20%. Therefore, for practical purposes, a ratio of at least 6 times between the nominal values is recommended. The effect of choosing a lower STC capacitor value at startup is shown in figure 10. You can see the STC voltage dropping when charge is transferred to the VDD capacitor. In this case, the value of the STC capacitor is low enough for the STC voltage to drop below the disable threshold of the VDD regulator, resulting in the VDD capacitor being charged in steps. This can have potential bad effects when the microcontroller already starts up at a lower voltage. In that case, the microcontroller will be powered solely from the small charge on the VDD capacitor, and the VDD voltage will collapse, resulting in a cycle of microcontroller reboots.

Choosing a low STC capacitor value will also severely reduce the shutdown time.

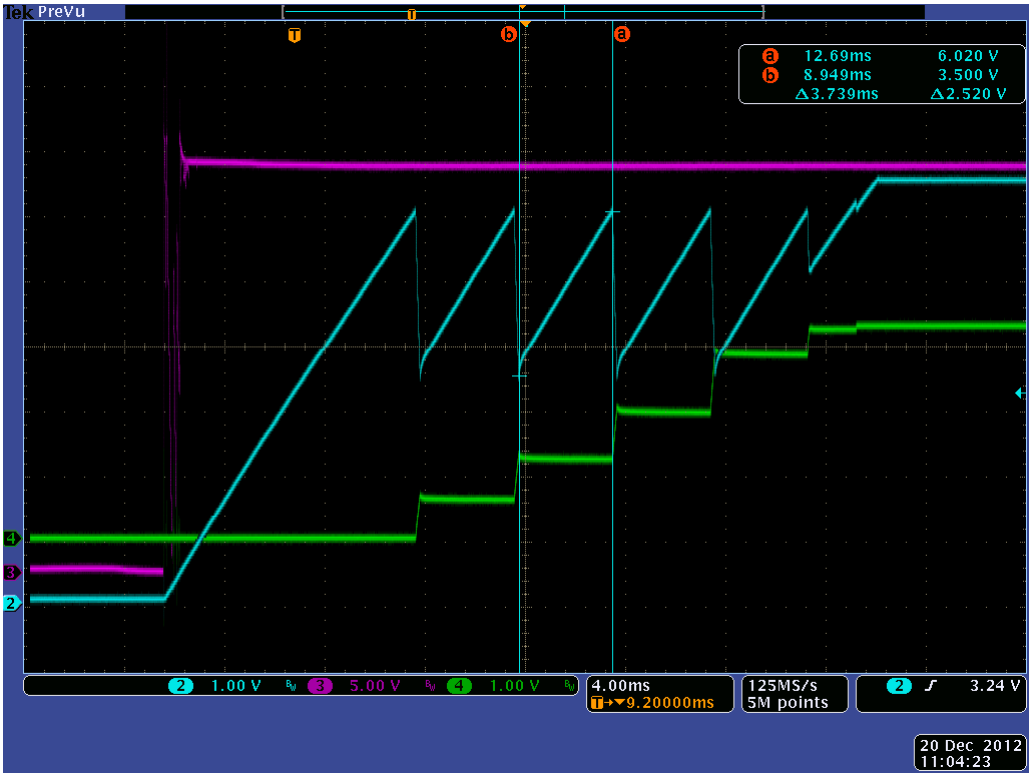


Figure 10. Charge Transfer Instability (NCN5150, C_{STC} = 2 µF, C_{VDD} = 1 µF, 1 Unit Load, no external load) (purple = BUSL1, blue = STC, green = VDD)

However, there is also another factor that is usually stricter in determining the minimum capacitance on C_{STC}. The value of C_{STC} has an influence on the stability of the bus current regulator. For values of C_{STC} that are too small, the bus current regulator will become unstable and an oscillation will become visible on the bus current. To ensure stable operation under all environmental conditions and sample variation, a minimum C_{STC} capacitor value of 10 µF is required.

Current available for application (during transmit)

Thanks to the internal operation of the NCN5150, the application has an extra 200 µA (typical) available to be drawn from VDD or STC when the transceiver is sending a space. This extra current is on top of the expanded current budget offered by the NCN5150 due to its reduced power consumption. This may ease the design of an isolated application. On the TSS721A, the current available is constant.

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