AND9101/D

The Importance of Compensation Capacitors on the eFuse Power Line

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APPLICATION NOTE

Introduction

ON Semiconductor produces a wide variety of silicon based protection products including current limiting devices such as Electronic Fuses (eFuses). During an over−current stress, eFuses can limit the current applied to a load as well as remove power from the load entirely. This fundamental feature of the eFuse makes it an easy choice to protect against inrush currents which can be seen on power lines of hard−disk drive (HDD) and enterprise−server systems during hot−plug operation or load−fault conditions. During the eFuse current limiting operation, the threat exists of an inductive spike on the power line (V_{CC}) at the point of device turn−off due to thermal shutdown. This Application Note will discuss the failure mechanism this threat exposes the eFuse to, and will explain how to combat it by adding compensation capacitors onto the power line when using the auto−retry (MN2) version of the eFuse.

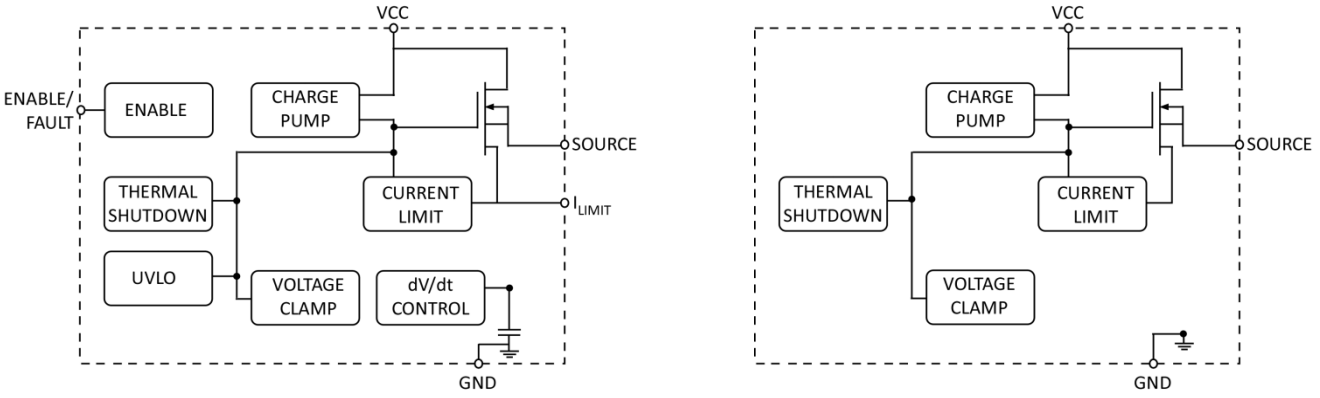

Figure 1. Block Diagram for a Full−Featured eFuse on the Left and a Reduced−Feature eFuse on the Right

eFuse Block Diagram and Operation

Simplified block diagrams of a full−featured eFuse and a reduced−feature eFuse are shown in Figure 1. The main element of the eFuse is a SENSEFET MOSFET. The SENSEFET is a power MOSFET made up of a large MOSFET to carry most of the current and a small MOSFET in parallel for current sensing. The SENSEFET provides an easy way of sensing the output current of the eFuse (the load current) through the use of a low−cost board−level resistor. The sensed current is used internally in the eFuse to control the gate of the SENSEFET and thereby control the output current. The fully−featured eFuse shown on the left of Figure 1 is a resettable fuse with two options for transitioning from the off state to the normal conducting state: the “latch” (MN1) and “auto−retry” (MN2) versions. The “latch” version is resettable through a power cycle or the toggling of the EN pin while in the “auto−retry” version, the eFuse automatically resets after thermal cycling. Upon resetting and entering the conducting state, the auto−retry eFuse may once again immediately encounter the load−fault that originally caused it to turn off in the first place, and lead it to once again enter self−protecting thermal shut−down and turn off. This on−off−on cycle can continue indefinitely if the load−fault is not independently resolved. Note; that for the reduced−feature eFuse shown in the right side of Figure 1, in the absence of an Enable/Fault pin only the auto−retry (MN2) version can be possible. An example of a reduced−feature eFuse is NIS2402MN2, developed for 12 V power buses. In the remaining part of this document we use measurements from NIS2402 to illustrate several points.

Cause for Concern

In the event of an inductive voltage spike, the “auto−retry” version, due to its constant turn on/turn−off action, will experience the spike with a repetition rate in the kHz range. A sample oscilloscope screenshot of the eFuse under current

limit, thermal shutdown and subsequent assertion of its "auto−retry" function is shown in Figure 2. Output voltage and current are represented by CH1 and CH3 respectively. The output current can be seen dropping to zero some time after the overload current condition happens (t = 0 ms). At this point, the eFuse has reached the thermal limit and shuts down, as indicated by the output current and voltage dropping to zero. After a cooling period, when the temperature has decreased 40°C below thermal limit, both the output voltage and current can be seen rising back to the level seen in the short−circuit condition. Since the fault on the output is still present, the eFuse shuts down again and the pattern repeats as shown in Figure 2.

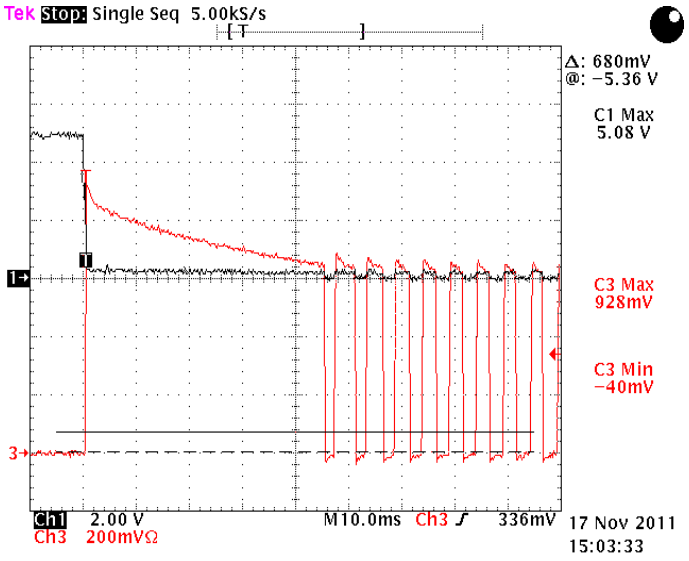

Figure 2. eFuse Current Limit Operation for NIS2402, a Reduced−Feature eFuse

As shown in the previous figure, the "auto−retry" function will continue to reassert as long as the short condition has not been lifted (eliminated). The frequency of this on/off behavior is dependent on the self−heating of the eFuse and its internal thermal switch tripping off and back on after a cooling period. Due to a built−in 100 μs turn−on delay and the eFuse's built−in controlled voltage ramp, the turn−on of current by the eFuse is controlled. However, the turn−off process does not have such a controlled ramp, and the fall time of the output current dropping to zero is less than 1 μs in most cases. External inductance in the circuit, represented by board traces, connecting wires, etc., will induce a voltage spike on V_{CC} during this fast turn−off. The magnitude of this spike is determined by the principal relationship in Equation 1.

$$V = -L * (dI/dt) \qquad \text{(eq. 1)}$$

Where: V is the voltage spike on V_{CC}
L is the external inductance and
dI/dt is the rate of change in current

Just before thermal shutdown, the eFuse is in short circuit operation with no change in current occurring through the external inductor and therefore the induced voltage is equal to zero. Figure 3 shows the circuit under this condition.

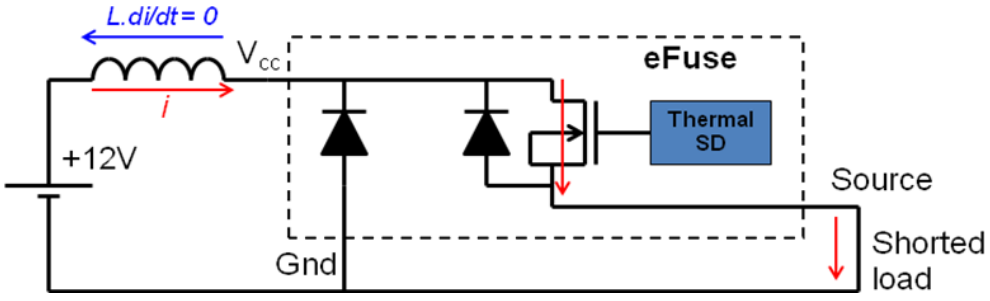

Figure 3. Circuit Condition Just Before Turn−off. All Circuit Inductance has been Lumped into a Single Element

Thermal shutdown results in a rapid drop in current from the eFuse's short circuit level to zero current. Due to the change in current, a voltage spike will occur on the V_{CC} line with a magnitude that may be large enough to break down the drain−to−source junction (body diode) as well as the TVS junction between the V_{CC} pin and the GND pad of the eFuse. Figure 4 shows the circuit under this condition.

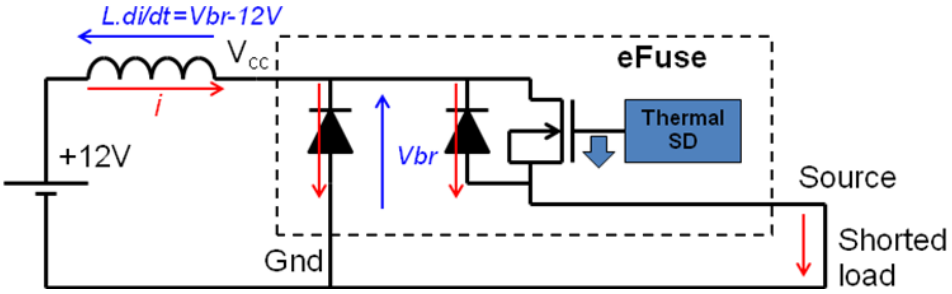

Figure 4. Circuit Condition Just After Turn−off

Once conducting, these junctions will clamp the V_{CC} spike and conduct the inductive current in reverse breakdown until the energy is dissipated. This energy may exceed the power handling capability of either or both junctions, thus causing irreversible failure of the eFuse. Once this happens, a direct path from V_{CC} to GND will be present, with the power supply carrying high enough current to cause internal bond wire melting on V_{CC} and GND pins, thereby causing irrecoverable damage.

Adding Compensation Capacitors

To address the issue of inductive current breaking down the internal junctions of the eFuse, capacitors can be placed on the V_{CC} line, in physical proximity to the eFuse. These capacitors "compensate" for the added external inductance and thus reduce the magnitude of the voltage spike on V_{CC} after turn−off.

In order to test this theory, inductive switching evaluations with both uncompensated and compensated circuits were performed. The set−up included a voltage source with a source inductance caused by connecting cables. The first test circuit had a 10 μF capacitor on the V_{CC} line to compensate for the source inductance and a "test inductance" placed on the V_{CC} line downstream of the capacitor, as shown in Figure 5. The value of L_{test} was varied from 0 μH to 11.7 μH in order to study its effect on the peak of the V_{CC} spike. Here L_{test} represents trace inductance on the application board; a poorly designed board will have a higher value of L_{test}.

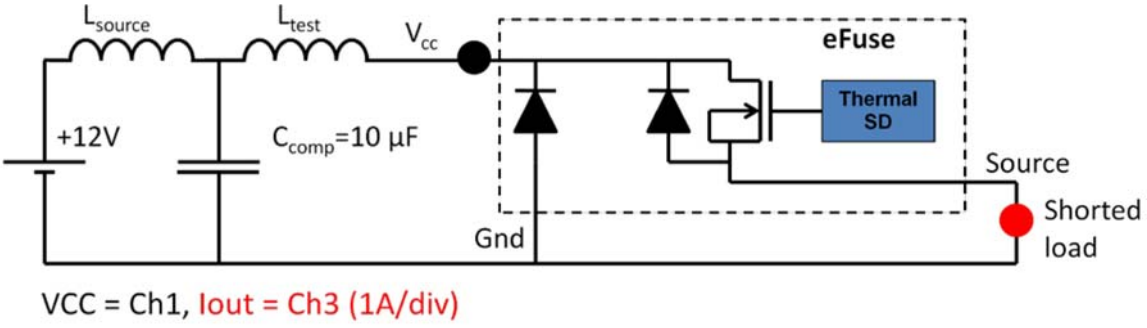

Figure 5. Test Circuit for "Uncompensated" Inductive Switching

The second test circuit included the 10 μF capacitor placed downstream from the test inductor and closer to the eFuse, in order to compensate for both L_{source} and L_{test}, as shown in Figure 6. Once again, the test inductance value was varied from test to test in order to show the effect the compensation capacitor had on the peak of the V_{CC} spike.

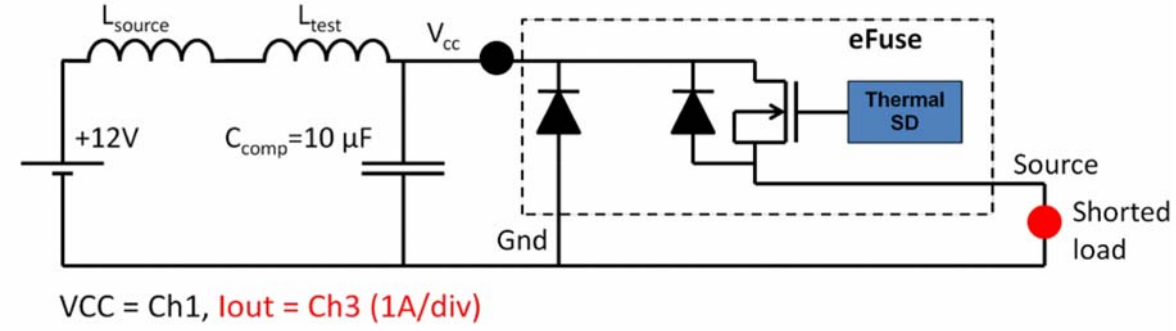

Figure 6. Test Circuit for "Compensated" Inductive Switching

Oscilloscope screenshots were taken to capture the turn−on and turn−off properties of the eFuse and how the inductance and capacitance affects this behavior. As seen in Figures 7 and 8, the V_{CC} voltage trace (CH1) and output current trace (CH3) are shown for the 11.7 μH test inductance on the uncompensated circuit.

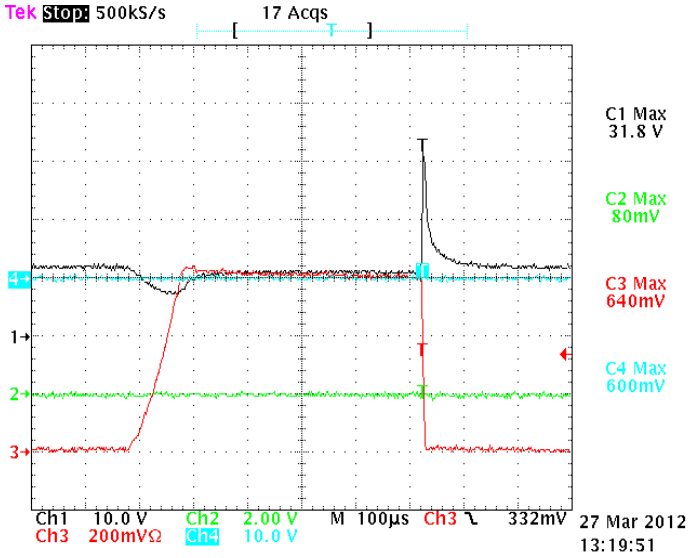

Figure 7. Scope Trace for the First (Uncompensated) Circuit with L_{test} = 11.7 μH

In Figure 7, it is shown that when the circuit is switched on, the current increases slowly since the current is limited by the eFuse's turn−on ramp. The current ramp is eventually clamped when it reaches the eFuse's short circuit limit. There is a small, negative going inductive peak during turn on, but its size is minimal due to the slow current ramp. The situation is very different during thermal shutdown when the fall time is much faster. The inductive spike can clearly be seen on V_{CC} as the eFuse turns off after it has been in short circuit current limiting mode for ~400 μs.

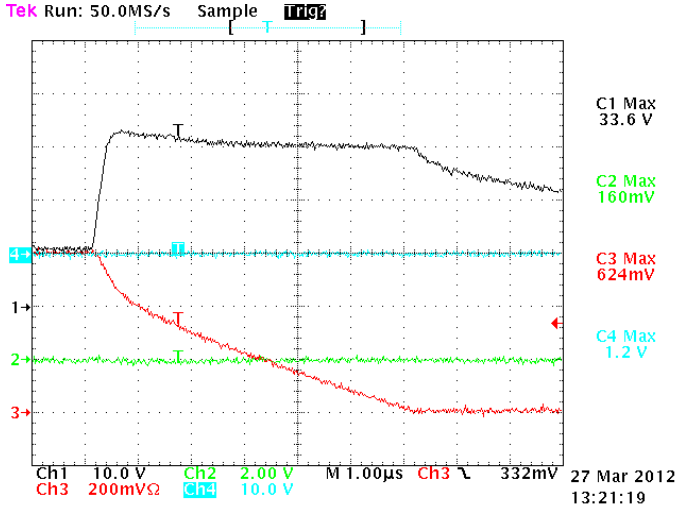

Figure 8. Zoomed Scope Trace for the First (Uncompensated) Circuit with L_{test} = 11.7 μH

A zoomed in view of the turn−off, Figure 8, shows that for an 11.7 μH inductance, a V_{CC} voltage peak of 33.6 V is achieved. The V_{CC} voltage peak exceeds the 25 V transient max limit for the eFuse (see datasheet) and is severely damaging to the device. The relatively flat output voltage during the ramp down of the current is caused by the clamping of the TVS diode and/or the diodes of the SENSEFET in the eFuse. This deposits considerable energy into the eFuse and can cause permanent damage.

The evaluations using the second (fully compensated) test circuit were performed for two high values of L_{test}, namely 4.3 μH and 11.7 μH. Figures 9 and 10 show the scope traces for L_{test} = 11.7 μH for 100 μs and 200 ns timescales respectively.

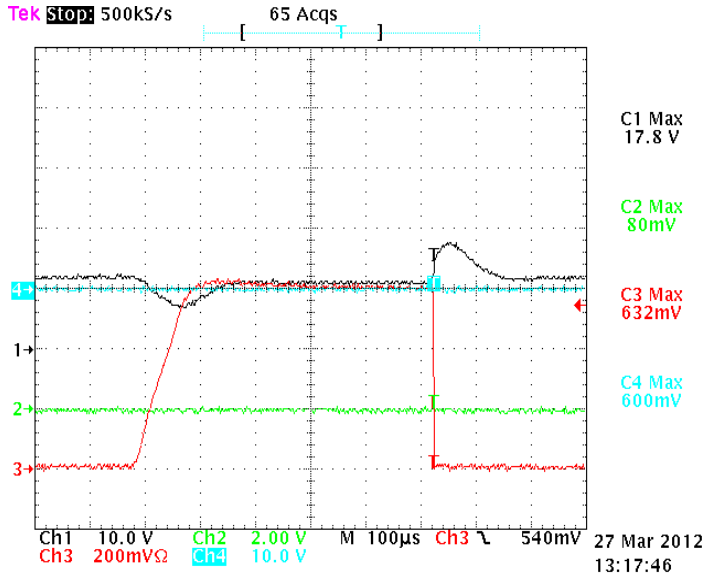

Figure 9. Scope Trace for the Second (Compensated) Circuit with L_{test} = 11.7 µH

As in Figure 7, the circuit is switched on and the eFuse reacts by going directly into current limiting. The inductive spike can still be seen on V_{CC} as the eFuse turns off after it has been in short circuit current limiting mode for ~400 µs. However, the spike is of much lower magnitude than seen in the previous (uncompensated) circuit.

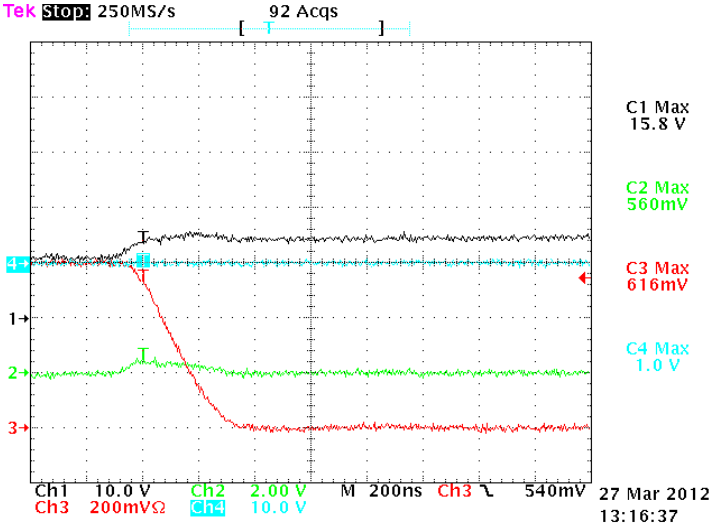

Figure 10. Zoomed Scope Trace for the Second (Compensated) Circuit with L_{test} = 11.7 µH

A zoomed−in view of the turn−off, Figure 10, shows a V_{CC} voltage peak of 15.8 V and a turn−off time as short as 400 ns. With the addition of the 10 µF compensation capacitor, the V_{CC} voltage peak is reduced by a factor of 2 and is within the 25 V transient capability for the eFuse thus ensuring that damage is eliminated. Table 1 shows the complete results of the inductive switching evaluations.

Table 1. INDUCTIVE SWITCHING RESULTS FOR BOTH COMPENSATED AND UNCOMPENSATED TEST CIRCUITS

Compensation	L_{test} (μH)	I_{SC} (A)	Turn−off Time (ns)	V_{CC} Spike (V)
NO	1.0	3.12	350	15.8
NO	1.1	3.12	480	24.0
NO	4.3	3.10	1800	34.4
NO	11.7	3.12	6000	33.6
NO	11.7	4.74	10500	32.4
YES	4.3	3.10	400	16.0
YES	11.7	3.08	400	15.8

Summary

This Application Note has explained the threat an inductive voltage spike on the V_{CC} line poses during eFuse turn−off under thermal shutdown, and how to combat it with the addition of compensation capacitors. The inductive switching evaluation for an uncompensated circuit shows that the peak voltage of the inductive spike can reach up to 33 V, which greatly exceeds the transient voltage max limit of 25 V rated for the eFuse. Not only is the peak voltage damaging, but the current lasts for several μs which deposits considerable energy into the eFuse. The eFuse failure mode for a sustained inductive spike like this is the breakdown of the internal drain−source junction as well as the TVS junction on the V_{CC} pin of the eFuse. The same inductive switching test with 10 μF of compensation capacitance added shows that the peak of the inductive spike is reduced to 16 V and the energy dissipation time is greatly reduced, down to the ns timescale range. These evaluations show the need for adding suitable compensation capacitors on the V_{CC} line. The capacitor needs to be placed close to the eFuse V_{CC} pin in order to help compensate for the external inductance in the circuit right up to the device pin. A 10 μF or lower value capacitance is suggested, which allows the implementation of a low cost capacitor on the board.

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