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Operation of NCP5252 in Low Dropout Applications

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APPLICATION NOTE

Introduction

The NCP5252 is a single−phase buck regulator with integrated Power MOSFETs. The device is able to deliver up to 2 A current at an externally adjustable output voltage, which range is from 0.6 V to 5.0 V. The operation range of the input supply voltage is from 4.5 V to 13.2 V. To provide a design guide for low dropout applications, detailed operation behavior of the NCP5252 is described in this application note. Both measurement and calculation results of a 5 V−output application are provided.

Low Dropout PWM Operation

As a non−isolated buck converter, the input supply voltage V_{IN} of the NCP5252 needs to be higher than the output voltage V_{OUT} to provide a sustainable current to a load. In applications where V_{IN} is much higher than V_{OUT}, the NCP5252 operates in a selected fixed−frequency in CCM. When the input voltage V_{IN} drops to be close to the output voltage V_{OUT}, it is possible to see other two operation modes with the NCP5252. Figure 1 is a plot that illustrates key signals in these operation modes.

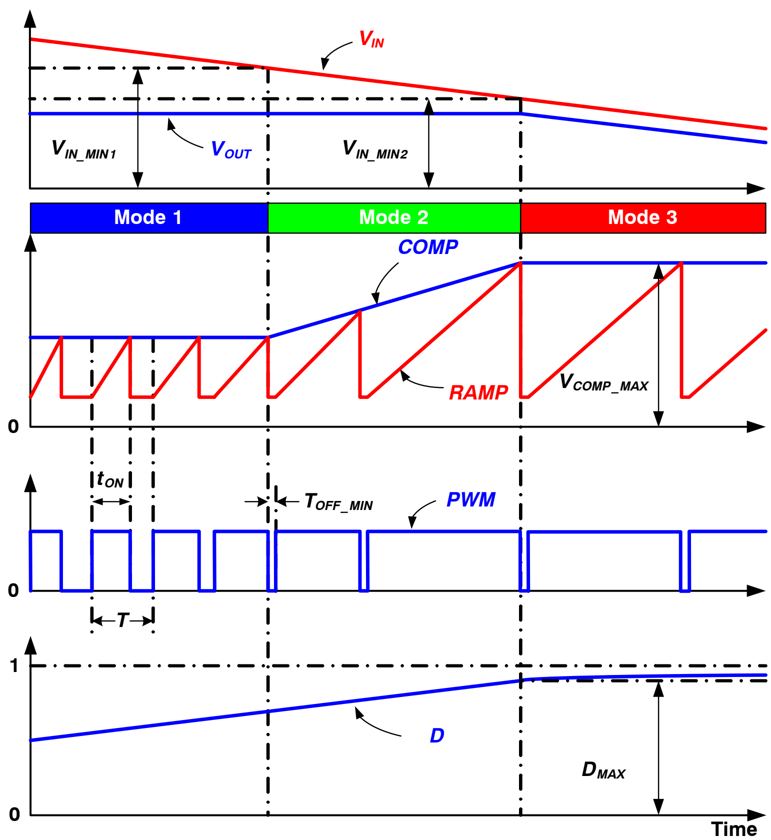


Figure 1. PWM Regulation Modes with the NCP5252

Mode 1 – Fixed−Frequency Operation

As shown in Figure 1, the NCP5252 operates in Mode 1 when the input supply voltage V_{IN} is higher than a minimum required voltage V_{IN_MIN1}. It is a fixed−frequency operation mode with an externally programmed frequency at FREQ_SET pin. The duty ratio of the PWM signal can be estimated by

$$D = \frac{V_{OUT} + I_{OUT} \cdot \left(R_{DS\_L} + DCR\right)}{V_{IN} - I_{OUT} \cdot \left(R_{DS\_H} - R_{DS\_L}\right)} \quad \text{(eq. 1)}$$

where I_{OUT} is the load current, DCR is the DC resistance of the output filter inductor L, R_{DS_H} is the conduction resistance of the integrated high−side MOSFET, and R_{DS_L} is the conduction resistance of the integrated low−side MOSFET. To simplify analysis, the diode voltage drops of MOSFETs during dead times have not been taken into account in this calculation.

To ensure good stability and line transient response, a V_{IN} feedforward function has been implemented in the NCP5252's ramp generator. The slew rate SR_{RAMP} of the ramp signal is proportional to both the input voltage V_{IN} and the nominal switching frequency F_{SW}.

$$SR_{RAMP} = 0.25 \cdot V_{IN} \cdot F_{SW} \quad \text{(eq. 2)}$$

As a result of the input feedforward function, the voltage level V_{COMP_M1} of the error signal COMP does not change much with the input voltage V_{IN}, having a value of

$$V_{COMP\_M1} = D \cdot T \cdot SR_{RAMP} + V_{RAMP\_OFFSET}, \quad \text{(eq. 3)}$$

where V_{RAMP_OFFSET} is the offset/valley voltage (0.4 V typical) of the ramp signal.

When the input voltage V_{IN} drops, the duty ratio D increases to maintain the output regulation with the fixed switching frequency until the off time of the PWM signal reaches its minimum limit T_{OFF_MIN} (225 ns typical in datasheet, but it would be better to use 260 ns in calculation to cover dead times of gate drivers.). The minimum required voltage V_{IN_MIN1} can be obtained by

$$V_{IN\_MIN1} = \frac{V_{OUT} + I_{OUT} \cdot \left(R_{DS\_L} + DCR\right)}{1 - F_{SW} \cdot T_{OFF\_MIN}} + I_{OUT} \cdot \left(R_{DS\_H} - R_{DS\_L}\right). \quad \text{(eq. 4)}$$

Mode 2 – Frequency−Deduction Operation

If the input voltage drops below V_{IN_MIN1}, the off time of the PWM signal cannot be reduced further due to T_{OFF_MIN}. This forces the NCP5252 to reduce switching frequency to maintain the output regulation. The switching frequency in Mode 2 operation is

$$F_{SW\_M2} = \frac{1 - D}{T_{OFF\_MIN}}. \quad \text{(eq. 5)}$$

The control loop pushes the COMP voltage to a higher level V_{COMP_M2} to get a wider on time T_{ON_M2}.

$$V_{COMP\_M2} = T_{ON\_M2} \cdot SR_{RAMP} + V_{RAMP\_OFFSET} \quad \text{(eq. 6)}$$

$$T_{ON\_M2} = \frac{T_{OFF\_MIN}}{\frac{V_{IN} + I_{OUT} \cdot \left(R_{DS\_L} - R_{DS\_H}\right)}{V_{OUT} + I_{OUT} \cdot \left(R_{DS\_L} + DCR\right)} - 1} \quad \text{(eq. 7)}$$

The maximum on time is limited by the maximum voltage level V_{COMP_MAX} of the COMP signal, which typical value is 3.5 V. A corresponding minimum input voltage V_{IN_MIN2} to maintain the target regulation voltage can be calculated by:

$$V_{IN\_MIN2} = \frac{V_{OUT} + I_{OUT} \cdot \left(R_{DS\_H} + DCR\right)}{1 - \frac{0.25 \cdot F_{SW} \cdot T_{OFF\_MIN}}{V_{COMP\_MAX} - V_{RAMP\_OFFSET}} \cdot \left(V_{OUT} + I_{OUT} \cdot \left(R_{DS\_L} + DCR\right)\right)} \quad \text{(eq. 8)}$$

Mode 3 – Maximum−Duty Operation

If the input voltage drops below V_{IN_MIN2}, the COMP signal is clamped to V_{COMP_MAX}, and thus the NCP5252 reaches its limitation in the on time T_{ON_M3}.

$$T_{ON\_M3} = \frac{V_{COMP\_MAX} - T_{RAMP\_OFFSET}}{SR_{RAMP}} \quad \text{(eq. 9)}$$

The switching frequency F_{SW_M3} in Mode 3 does not decrease as much as that in Mode 2 when VIN drops.

$$F_{SW\_M3} = \frac{1}{T_{ON\_M3} + T_{OFF\_MIN}} \quad \text{(eq. 10)}$$

The NCP5252 reaches its maximum limitation in the duty ratio, which has a value D_{MAX} when the input voltage is equal to V_{IN_MIN2}.

$$D_{MAX} = \frac{1}{1 + \frac{0.25 \cdot V_{IN\_MIN2} \cdot F_{SW} \cdot T_{OFF\_MIN}}{V_{COMP\_MAX} - V_{RAMP\_OFFSET}}} \quad \text{(eq. 11)}$$

In Mode 3, the output voltage drops as input voltage drops. The output voltage can be calculated by

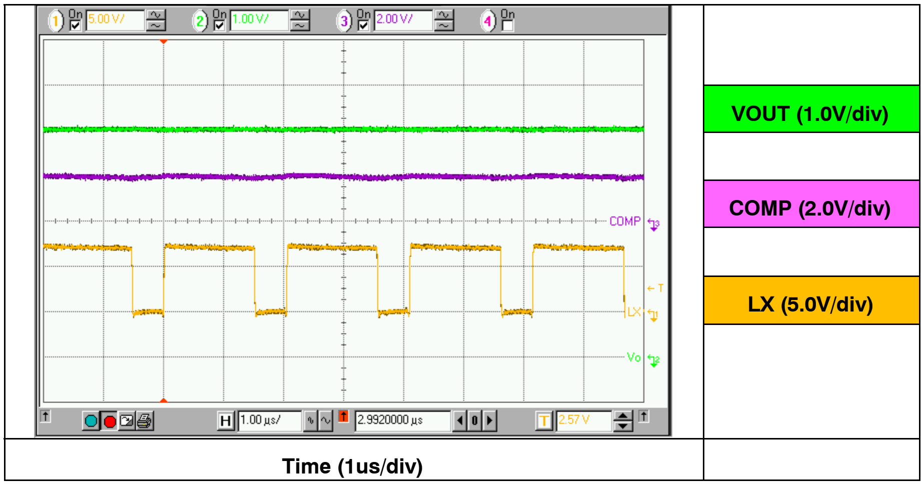
$$V_{OUT\_M3} = \frac{V_{IN} - I_{OUT} \cdot \left(R_{DS\_H} - R_{DS\_L}\right)}{1 + \frac{0.25 \cdot V_{IN} \cdot F_{SW} \cdot T_{OFF\_MIN}}{V_{COMP\_MAX} - V_{RAMP\_OFFSET}}} - I_{OUT} \cdot \left(R_{DS\_L} + DCR\right) \quad \text{(eq. 12)}$$

The voltage drop between V_{IN} and V_{OUT} increases as I_{OUT} increases.

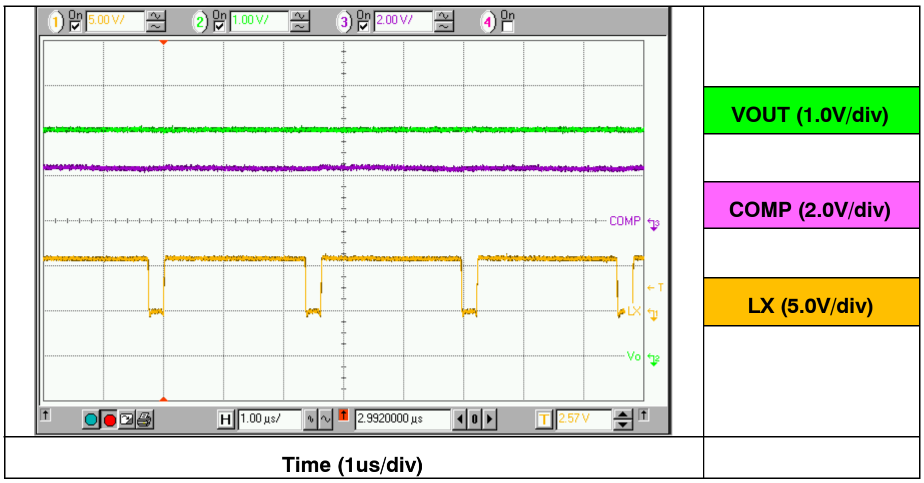
5 V−Output Application

To verify the operation of the NCP5252 in a low dropout application, a 5 V−output regulator has been built on a NCP5252 demo board. Three plots in Figure 2 show waveforms of three key signals (V_{OUT}, COMP, and LX) under the three operation modes when V_{IN} is close to V_{OUT}. The load current is 1 A and the selected nominal frequency is 500 kHz in this test. The switching frequency drops smoothly as V_{IN} drops. The minimum required input voltage for the 5 V/1 A output is about 5.5 V. The NCP5252 still be able to provide current to the output when V_{IN} drops further, but the output voltage starts to drop below the 5 V target.

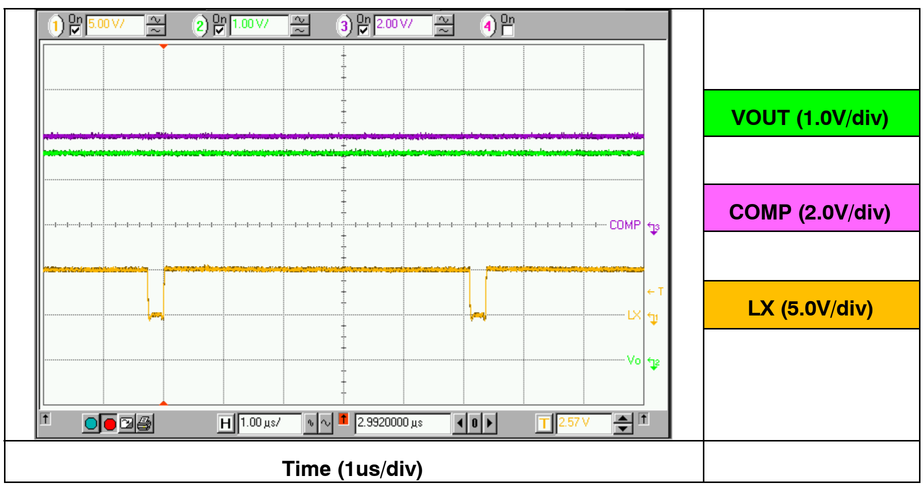
Figure 3 shows measurement results with a 1 A load current and three nominal switching frequency options. The higher the nominal frequency is selected, the higher V_{IN_MIN2} is required to maintain the 5 V output voltage. V_{IN} Figure 4 shows measurement results of the switching frequency changing with the input voltage for three nominal frequency options. The NCP5252 is able to have about 60% off in switching frequency in this application. The 333 kHz frequency option is able to support the lowest minimum input voltage in the low dropout applications.



(a) V_{IN} = 7.0 V (Mode 1)



(b) V_{IN} = 5.75 V (Mode 2)



(c) V_{IN} = 5.0 V (Mode 3)

Figure 2. PWM Operation Waveforms vs. Input Voltage (V_{OUT} = 5 V, I_{OUT} = 1 A, 500 kHz Option)

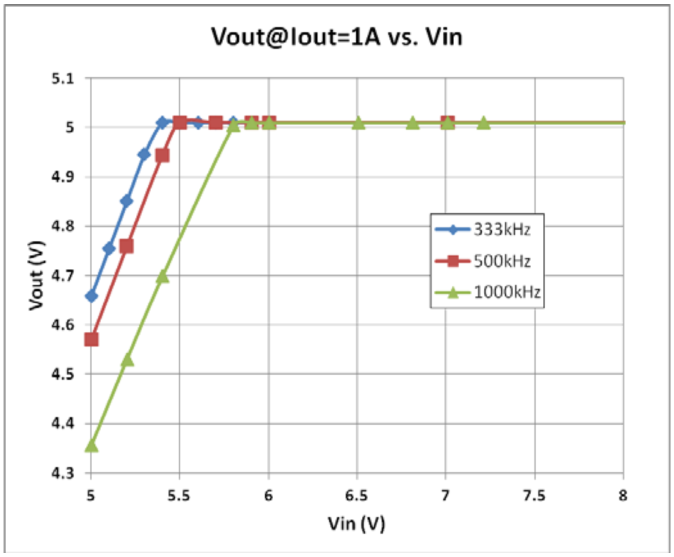


Figure 3. Output Regulation V_{OUT} vs. Input Voltage V_{IN}

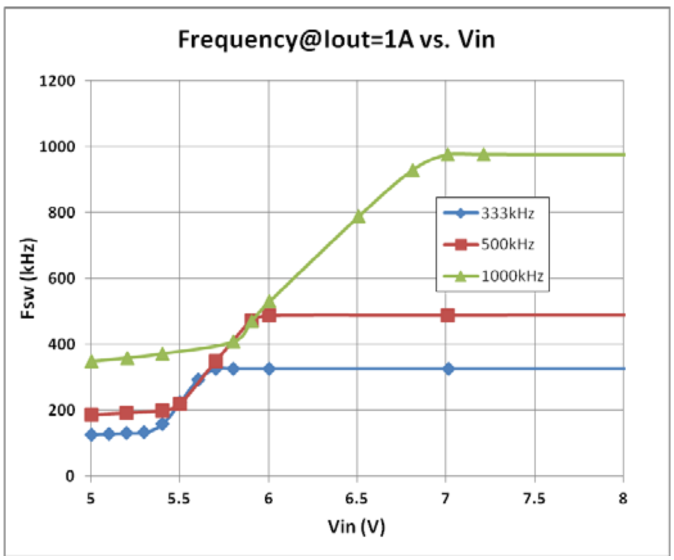


Figure 4. Switching Frequency F_{SW} vs. Input Voltage V_{IN}

As shown in Figure 5, a result comparison between measurements and calculations has been done on the minimum required input voltage V_{IN_MIN2} to maintain 5 V output voltage under different load current conditions. Both results address that higher minimum input voltage is required for higher load current. Difference between the measurements and the calculations grows with an increasing in the load current, which may be caused by some omitted factors in the calculations such as body diode forward voltage during dead times, conduction resistance variations regarding to temperatures of inductor and MOSFETs, and other power lose factors.

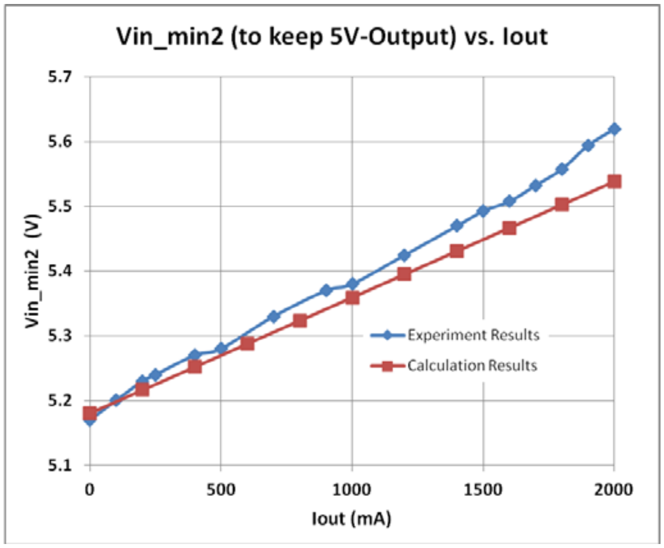


Figure 5. Minimum Input Voltage V_{IN_MIN2} vs. Load Current I_{OUT} (333 kHz Option)

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