AND9065/D

5 Key Steps to Design a Compact, High-Efficiency PFC Stage Using the NCP1612

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APPLICATION NOTE

This paper describes the key steps to rapidly design a Discontinuous Conduction Mode PFC stage driven by the NCP1612. The process is illustrated in a practical 160 W, universal mains application:

- Maximum Output Power: 160 W
- Rms Line Voltage Range: from 90 V to 265 V
- Regulation Output Voltage: 390 V
- Frequency Fold-back when the Line Current is Less than 450 mA

Introduction

Housed in a SO−10 package, the NCP1612 is designed to optimize the efficiency of your PFC stage throughout the load range. Incorporating protection features for rugged operation, it is ideal in systems where cost-effectiveness, reliability, low stand-by power and high efficiency are key requirements:

- *Current Controlled Frequency Fold-back (CCFF):* The circuit operates in Critical conduction Mode (CrM) when the instantaneous line current is medium or high. When this current is lower than a preset level, the frequency linearly decays to about 20 kHz. CCFF maximizes the efficiency at both nominal and light loads[1]. In particular, stand-by losses are minimized.
- *Skip Mode:* To further optimize the efficiency, the circuit skips cycles near the line zero crossing where the power transfer is particularly inefficient. If superior power factor is needed, this feature can be inhibited by forcing a minimum 0.75 V voltage.
- *Low Start-Up Current and Large V_{CC} Range:* The extra low start-up consumption of the B version (NCP1612B) allows the use of high-impedance resistors for charging the V_{CC} capacitor. The A version (NCP1612A) is targeted in applications where the circuit is fed by an auxiliary power source. Its start-up level is lower than 11.25 V to allow the circuit to be powering from a 12 V rail. Both versions feature a large V_{CC} operating range (9.5 V to 35 V).
- *Fast Line/Load Transient Compensation (Dynamic Response Enhancer and Soft OVP):* Due to the slow loop response of traditional PFC stages, abrupt changes in the load or in the input voltage may cause significant over or under-shoots. This circuit drastically limits these possible deviations from the regulation point.
- *Safety Protections:* NCP1612 features make the PFC stage extremely robust. Among them, we can mention the Brown-out Detection block[2] that stops operation when the ac line is too low and the 2 level Current Sensing, that forces a low duty-ratio operation mode in the event that the current exceeds 150% of the current limit which may be caused by the inductor saturation or by a short of the bypass or boost diode.
- *“Master PFC”:* Forward or half-bridge converters take advantage of a narrow input voltage range. The NCP1612 dynamic response enhancer and its soft OVP help minimize the bulk voltage deviation. In addition, the NCP1612 grounds its pfcOK pin to disable the downstream converter until the bulk voltage has reached its target level and whenever the NCP1612 detects a fault. In particular, the downstream converter is disabled if the NCP1612 “FOVP/BUV” pin detects that the bulk voltage has dropped below 76% of its regulation level.
- *Latched off Capability:* The NCP1612 pfcOK pin is in high-impedance state when the PFC stage is in nominal operation. The circuit latches off if the pin is pulled-up above 7.5 V and cannot recover until a brown-out situation is detected or until V_{CC} drops below its reset level (5 V typically).

[1]Like in **FCCrM** controllers, internal circuitry allows near-unity power factor even when the switching frequency is reduced.

[2]The voltage of the Brown-out detection block input pin (“V_{SENSE}”) is also used to detect the line range and reduce the loop gain in high-line conditions (2-step feed-forward).

- *Eased Manufacturing and Safety Testing:* Elements of the PFC stage can be accidentally shorted, badly soldered or damaged as a result of manufacturing or handling incidents, excessive operating stress or other troubles. In particular, adjacent pins of controllers can be shorted, a pin, grounded or badly connected. It is often required that such open/short situations do not cause fire, smoke nor loud noise. The NCP1612 integrates enhanced functions that help address requirement, for instance, in case of an improper pin connection (including GND) or of a short of the boost or bypass diode. Application note AND9046/D details the behavior of a NCP1612-driven PFC stage under safety tests [1].

PFC Stage Dimensioning

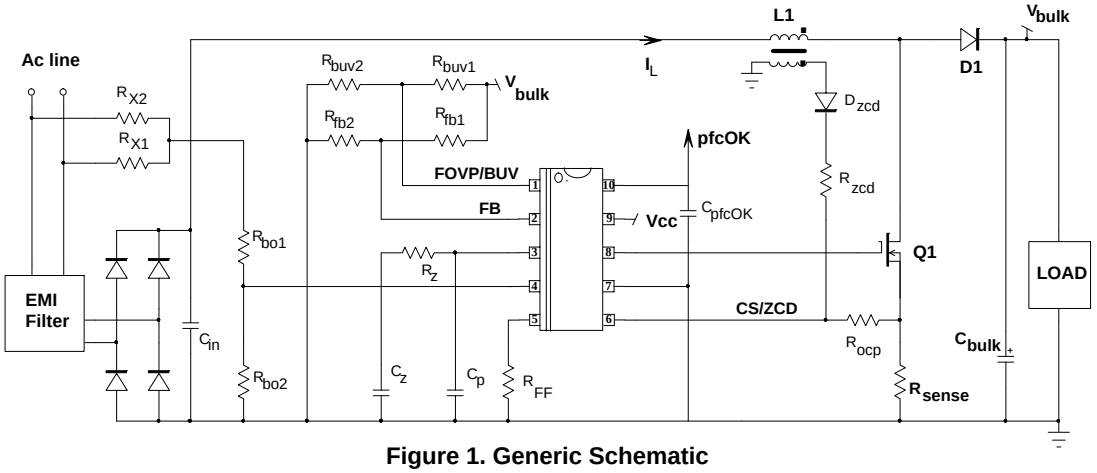


Figure 1. Generic Schematic

Step 1: Define the Key Specifications

- f_{line}*:* Line frequency. 50 Hz/60 Hz applications are targeted. Practically, they are often specified in a range of 47 − 63 Hz and for calculations such as hold-up time, one has to factor in the lowest value specified.
- $(V_{line,rms})_{LL}$*:* Lowest level of the line voltage. This is the minimum rms input voltage for which the PFC stage must operate. Such a level is usually 10−12% below the minimum typical voltage which could be 100 V in many countries. We will take: $(V_{line,rms})_{LL}$ = 90 V
- $(V_{line,rms})_{HL}$*:* Highest level for the line voltage. This is the maximum input rms voltage. It is usually 10% above the maximum typical voltage (240 V in many countries). We select: $(V_{line,rms})_{HL}$ = 264 V.
- $(V_{line,rms})_{boH}$*:* Brown-out line upper threshold. The circuit prevents operation until the line rms voltage exceeds $(V_{line,rms})_{boH}$. The NCP1612 offers a 10% hysteresis. Hence, if no specific action is taken, it will detect a brown-out situation and stop operation when the rms line voltage goes below$(V_{line,rms})_{boL}$ that equates(90% $(V_{line,rms})_{boH}$). In our application, we target:
  - $(V_{line,rms})_{boH}$ = 90% $(V_{line,rms})_{LL}$ = 81 V
  - $(V_{line,rms})_{boL}$ = 90% $(V_{line,rms})_{boH}$ ≅ 73 V
- $V_{out,nom}$*:* Nominal output voltage. This is the regulation level for the PFC output voltage (also designated bulk voltage). $V_{out,nom}$ must be higher than $(\sqrt{2} \cdot (V_{line,rms})_{HL})$. 390 V is our target value.
- $(\delta V_{out})_{pk-pk}$*:* Peak-to-peak output voltage ripple. This parameter is often specified in percentage of output voltage. It must be selected equal or lower than 8% to avoid triggering the Dynamic Response Enhancer (DRE) in normal operation.
- $t_{HOLD-UP}$*:* Hold-up time. This parameter specifies the amount of time the output will remain valid during line drop-out. One line cycle is typically specified. This requirement requires knowing the minimum voltage on the PFC stage output necessary for the proper operation in your application ($V_{out,min}$). We have assumed ($V_{out,min}$ = 350 V) is high enough to provide the downstream converter with a sufficient input voltage.
- P_{out}*:* Output power. This is the power consumed by the PFC load.
- $P_{out,max}$*:* Maximum output power. This is the maximum output power level, that is, 160 W in our application.
- $(P_{in,avg})_{max}$*:* Maximum input power. This is the maximum power that can be absorbed from the mains in normal operation. This level is obtained at full load, low line. Assuming an efficiency of 95% in these conditions, we will use: $(P_{in,avg})_{max}$ = 160/95% ≅ 170 W
- $I_{line,max}$*:* Maximum line current obtained at full load, low line.
- $\rho_{FF(\%)}$*:* Line Current Threshold below which the circuit reduces the frequency (CCFF) expressed as a percentage of $I_{line,max}$. If this parameter is higher than

100%, the PFC stage will permanently operates with a reduced frequency. Conversely, if $\rho_{FF(\%)}$is close to zero, the PFC stage will function in CrM (no frequency fold-back) in almost the whole power range. This parameter is normally selected in the range of 10 to 20%.

Step 2: Power Components Selection

In heavy load conditions, the NCP1612 operates in **Cr**itical conduction **M**ode (CrM). Hence, the inductor, the bulk capacitor and the power silicon devices are dimensioned as usually done with any other CrM PFC. This chapter does not detail this process, but simply highlights key points.

Inductor Selection

The on-time of the circuit is internally limited. The power the PFC stage can deliver, depends on the inductor since *L* will determine the current rise for a given on-time. More specifically, the following equation gives the power capability of the PFC stage:

$$(P_{in,avg})_{HL} = \frac{V_{line,rms}{}^2}{2L} \cdot T_{on,max} \qquad \text{(eq. 1)}$$

The smaller the inductor, the higher the PFC stage power capability. Hence, *L* must be low enough so that the full power can be provided at the lowest line level:

$$L \leq \frac{(V_{line,rms})_{LL}{}^2}{2 \cdot (P_{in,avg})_{max}} \cdot T_{on,max} \qquad \text{(eq. 2)}$$

Like in traditional CrM applications, the following equations give the other parameters of importance:

- Maximum Peak Current:

$$(I_{L,pk})_{max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{line,rms})_{LL}} \qquad \text{(eq. 3)}$$

- Maximum rms Current:

$$(I_{L,rms})_{max} = \frac{(I_{L,pk})_{max}}{\sqrt{6}} \qquad \text{(eq. 4)}$$

In our application, the inductor must then meet the following requirements:

$$L \leq \frac{90^2}{2 \cdot 170} \cdot 20\mu = 476\ \mu H$$

$$(I_{L,pk})_{max} = 2\sqrt{2} \cdot \frac{170}{90} \cong 5.3\ A \qquad \text{(eq. 5)}$$

$$(I_{L,rms})_{max} = \frac{5.3}{\sqrt{6}} \cong 2.2\ A$$

($T_{on,max}$ = 20 μs) is the minimum value for *Ton,max* (the typical value being 25 μs). ($T_{on,max}$ = 20 μs) is hence, used in Equation 5 since this is the worst case when calculating *L*. It is in addition, recommended to select an inductor value that is at least 25% less than that returned by Equation 5 for a healthy margin.

A 200 μH/6 A_{pk} inductor (ref: 750370081 from WÜRTH ELEKTRONIK) is selected. It consists of a 10:1 auxiliary winding for zero current detection.

One can note that the switching frequency in CrM operation depends on the inductor value:

$$f_{SW} = \frac{V_{line}(t)^2 \cdot (V_{out} - V_{line}(t))}{4 \cdot P_{in,avg} \cdot V_{out} \cdot L} \qquad \text{(eq. 6)}$$

For instance, at low line, full load (top of the sinusoid), the switching frequency is:

$$f_{SW} = \frac{(\sqrt{2} \cdot 90)^2 \cdot (390 - \sqrt{2} \cdot 90)}{4 \cdot 170 \cdot 390 \cdot 200 \cdot 10^{-5}} \cong 80\ kHz \qquad \text{(eq. 7)}$$

Power Silicon Devices

Generally, the diode bridge and the power MOSFET are placed on the same heat-sink.

As a rule of the thumb, one can estimate that the heat-sink will have to dissipate around:

- 4% of the Output Power in Wide Mains Applications (95% being generally the targeted minimum efficiency)
- 2% of the Output Power in Single Mains Applications

In our wide-mains application, about 6.4 W are then to be dissipated. We selected a low-profile heat-sink from COLUMBIA−STAVER (reference: TP207ST/120/12.5/NA/SP/03) whose thermal resistance has been measured to be in the range of 6°C/W.

Among the sources of losses that contribute to this heating, one can list:

- The diodes bridge conduction losses that can be estimated by the following equation:

$$P_{bridge} = 2 \cdot V_f \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta}}{V_{line,rms}} \approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta} \qquad \text{(eq. 8)}$$

where V_f is the forward voltage of the bridge diodes.

- The MOSFET conduction losses are given by:

$$(\rho_{on}) = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot \left(V_{line,rms}\right)_{LL}} \right) \cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,nom}} \right) \qquad \text{(eq. 9)}$$

In our application, we have:

- P_{BRIDGE} = 3.4 W, assuming that V_f is 1 V
- $(\rho_{on})_{max} = 3.4 \cdot R_{DS(on)}$. In our application, a low $R_{DS(on)}$ MOSFET (0.25 Ω @ 25°C) is selected to avoid excessive MOSFET losses. Assuming that $R_{DS(on)}$ doubles at high temperature, the maximum conduction losses are about 1.7 W

The total conduction losses can then be as high as about 5.1 W.

Switching losses cannot be easily computed. We will not attempt to predict them. Instead, as a rule of the thumb, we will assume a loss budget equal to that of the MOSFET conduction ones. Experimental tests will check that they are not under-estimated.

One can anyway note that the MOSFET turn off can be accelerated using the schematic of Figure 2, where the Q_1 NPN transistor (TO92) amplifies the MOSFET turn off gate current. This enhancer is implemented in our demo-board.

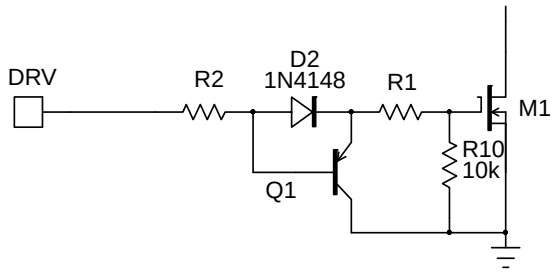


Figure 2. Q1 Speeds Up the MOSFET Turn Off

The boost diode is the source of the following conduction losses: ($I_{out} \cdot V_f$), where I_{out} is the load current and V_f the diode forward voltage. The maximum output current being nearly 0.4 A, the diode conduction losses are in the range of 0.4 W (assuming V_f = 1 V). P_{DIODE} = 0.4 W

Output Bulk Capacitor

There generally are three main criteria/constraints when defining the bulk capacitor:

- Peak-to-Peak Low Frequency Ripple:

$$(\delta V_{out})_{pk-pk} = \frac{P_{out,max}}{C_{bulk} \cdot \omega \cdot V_{out,nom}} \qquad \text{(eq. 10)}$$

where ($\omega = 2\pi \cdot f_{line}$) is the line angular frequency. This ripple must keep lower than ±4% of the output voltage (8% peak-to-peak). Taking into account the line frequency minimum value (47 Hz), this leads to:

$$C_{bulk} \geq \frac{160}{8\% \cdot 2\pi \cdot 47 \cdot 390^2} \cong 45\ \mu F \qquad \text{(eq. 11)}$$

- Hold-up Time Specification:

$$C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}{}^2 - V_{out,min}{}^2} \qquad \text{(eq. 12)}$$

Hence, a 10 ms hold-up time imposes:

$$C_{bulk} \geq \frac{2 \cdot 160 \cdot 10m}{390^2 - 350^2} \cong 108\ \mu F \qquad \text{(eq. 13)}$$

- Rms Capacitor Current:

The rms current depends on the load characteristic. Assuming a resistive load, we can derive the following approximate expression of its magnitude[3]:

$$(I_{c,rms})_{max} = \qquad \text{(eq. 14)}$$

$$= \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{(P_{in,avg})_{max}}{\sqrt{(V_{line,rms})_{LL} \cdot V_{out,nom}}}\right)^2 - \left(\frac{P_{out,max}}{V_{out,nom}}\right)^2}$$

In our application, we have:

$$I_{c,rms} \cong \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{170}{\sqrt{90 \cdot 390}}\right)^2 - \left(\frac{160}{390}\right)^2} \qquad \text{(eq. 15)}$$

$$\cong \sqrt{1.318 - 0.168} \cong 1.1\ A$$

Step 3: Bulk Voltage Monitoring and Regulation Loop

As shown by Figure 1, the feed-back arrangement consists of:

- A resistor divider that scales down the bulk voltage to provide pin 8 with the feedback signal. The upper resistor of the divider generally consists of three or four resistors for safety considerations (see R_8, R_9 and R_{10} of Figure 7). If not, any accidental shortage of this element would apply the output high voltage to the controller and destroy it.
- A filtering capacitor that is often placed between pin 8 and ground to prevent switching noise from distorting the feedback signal. A 1 nF capacitor is often implemented. Generally speaking, the pole it forms with the feedback resistors must remain at a very high-frequency compared to the line one. Practically,

$$C_{fb} \leq \frac{1}{150 \cdot (R_{fb1} \parallel R_{fb2}) \cdot f_{line}}$$

  generally give good results.
- A type-2 compensation network. Consisting of two capacitors and of one resistor, this circuitry sets the crossover frequency and the loop characteristic.

In steady-state the feedback being in the range of the 2.5 V regulation reference voltage, the feedback bottom resistor (R_{fb2} of Figure 1 or R_{11} of Figure 7) sets the bias current in the feedback resistors as follows:

$$I_{FB} = \frac{V_{REF}}{R_{fb2}} = \frac{2.5}{R_{fb2}} \qquad \text{(eq. 16)}$$

Trade-off between losses and noise immunity dictates the choice of this resistor. Resistors up to 56 kΩ ($I_{FB} \cong 50\ \mu A$) generally give good results. Higher values can be considered if allowed by the board PCB layout. Please note anyway that a 250 nA sink current (500 nA max. on the −40°C to 125°C temperature range) is built-in to ground the feedback pin and disable the driver if the pin is accidentally open. If I_{FB} is set below 50 μA, the regulation level may be significantly impacted by the 250 nA sink current.

[3]It remains wise to verify the bulk capacitor heating on the bench!

When the bottom resistor is selected, select the upper resistor as follows:

$$R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1 \right) \qquad \text{(eq. 17)}$$

In our application, we select a 27 kΩ for R_{fb2} ($I_{FB} \cong 92\ \mu A$). As for R_{fb1}, two 1800 kΩ resistors are placed in series with a 560 kΩ one. These normalized values precisely give: ($R_{fb1} = 4.16\ M\Omega$), leading to a nominal 388 V regulation level, which is acceptable.

Compensating the Loop

The loop gain of a PFC boost converter is proportional to the square of the line magnitude if no feed-forward is applied. Hence, this gain almost varies of an order of magnitude in universal mains conditions. The V_{SENSE} pin voltage is representative of the line voltage value. The NCP1612 uses this information to perform a discrete feed-forward function: in high-line that is detected when the pin voltage happens to exceed 2.2 V, the PWM gain is divided by 3 compared to a low-line state (which is set if V_{SENSE} is less than 1.7 V for 25 ms − see Figures 3 and 5).

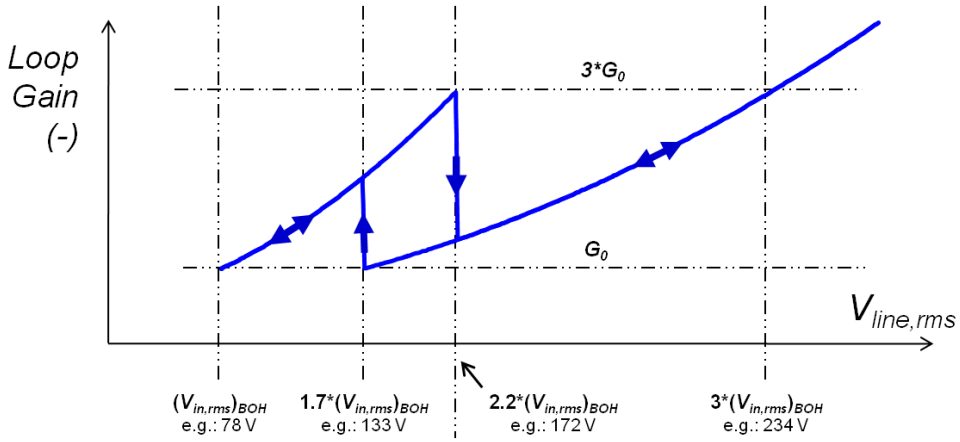


Figure 3. 2-step Feed-forward Limits the Loop Gain Variation with Respect to Line

Using the method described in [1] and [2], we can easily derive two small-signal transfer functions of our PFC stage (one for high line, one for low line):

- Low-line Transfer Function:

$$\frac{\hat{v}_{out}}{\hat{v}_{control}} = \frac{V_{in,rms}^{\ 2} \cdot R_{load}}{640000 \cdot L \cdot V_{out,nom}} \cdot \frac{1}{1 + s \cdot \frac{R_{load} \cdot C_{bulk}}{2}} \qquad \text{(eq. 18)}$$

- High-line Transfer Function:

$$\frac{\hat{v}_{out}}{\hat{v}_{control}} = \frac{V_{in,rms}^{\ 2} \cdot R_{load}}{1920000 \cdot L \cdot V_{out,nom}} \cdot \frac{1}{1 + s \cdot \frac{R_{load} \cdot C_{bulk}}{2}} \qquad \text{(eq. 19)}$$

Where:

- C_{bulk} is the Bulk Capacitor
- R_{load} is the Load Equivalent Resistance
- L is the PFC Coil Inductance
- $V_{out,nom}$ is the Regulation Level of the PFC Output

PFC stages must be slow. More practically, high PF ratios require the low regulation bandwidth to be in the range of 20 Hz or lower. Hence, sharp variations of the load result in excessive over and under-shoots. These deviations are effectively contained by the NCP1612 ***dynamic response enhancer*** together with its accurate over-voltage protection.

Still however, a type-2 compensation is recommended as shown in the following figure:

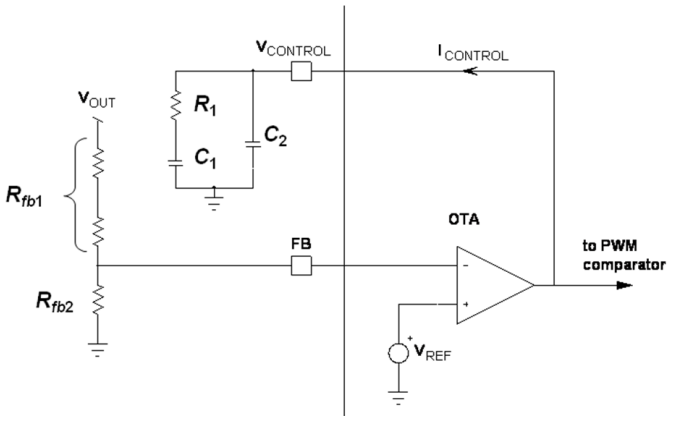


Figure 4. Regulation Trans-conductance Error Amplifier, Feed-back and Compensation Network

The output to control transfer function brought by the type-2 compensator is:

$$\frac{\hat{v}_{control}}{\hat{v}_{out}} = \frac{1 + sR_1C_1}{sR_0(C_1 + C_2)\left(1 + sR1\frac{C_1 \cdot C_2}{C_1 + C_2}\right)} \quad \text{(eq. 20)}$$

Where $R_0 = (V_{out,nom})/(V_{ref} \cdot G_{EA})$, G_{EA} being the 200 μS error amplifier trans-conductance gain, $V_{out,nom}$, the bulk nominal voltage and V_{REF}, the OTA 2.5 V voltage reference.

Applying the compensation method described in [2] and [3], we obtain the following dimensioning equations:

$$G_0 = \frac{\left(V_{line,rms}\right)_{LL}^{\ 2} \cdot R_{load,min}}{640000 \cdot L \cdot V_{out,nom}}$$

$$C_2 = \frac{G_0 \cdot \tan\left(\frac{\pi}{2} - \phi_m\right)}{2 \cdot \pi^2 f_c^{\ 2} \cdot R_{load,min} \cdot C_{bulk} \cdot R_0} \quad \text{(eq. 21)}$$

$$C_1 = \frac{G_0}{2 \cdot \pi \cdot f_c \cdot R_0} - C_2$$

$$R_1 = \frac{R_{load,min} \cdot C_{bulk}}{2 \cdot C_1}$$

Where:

- $(V_{in,rms})_{LL}$ is the rms Voltage of the Line when at its Lowest Level (90 V in our case)
- G_0 is Static Gain at the Lowest level of the Line ($(V_{line,rms})_{LL}$)
- ϕ_m is Phase Margin (in radians)
- f_c is the Targeted Crossover Frequency
- $R_{load,min}$ is the Load Equivalent Resistor at Full Load

$$R_{load,min} = \frac{V_{out,nom}^{\ 2}}{P_{out,max}} = \frac{390^2}{160} \cong 950$$

The crossover frequency is selected as low as possible but higher or equal to the PFC boost stage pole at full load

$$\left(f_p = \frac{1}{\pi \cdot R_{load,min} \cdot C_{bulk}} \cong 2.4\ \text{Hz}\right)$$

The phase margin is generally set between 45 and 70 degrees. In our application, if we target a 15 Hz crossover frequency and a 60 degree phase margin (π/3 in radians), we have:

$$G_0 = \frac{90^2 \cdot 950}{640000 \cdot 200 \cdot 10^{-6} \cdot 390} \cong 154$$

$$C_2 = \frac{154 \cdot \tan\left(\frac{\pi}{2} - \frac{\pi}{3}\right)}{2 \cdot \pi^2 \cdot 14^2 \cdot 950 \cdot 136 \cdot 10^{-6} \cdot 780 \cdot 10^{-3}}$$

$$\cong 200\ \text{nF} \Rightarrow \text{let's choose } 220\ \text{nF} \quad \text{(eq. 22)}$$

$$C_1 = \frac{154}{2\pi \cdot 15 \cdot 780 \cdot 10^{-3}} - C_2$$

$$\cong 1.9\ \mu\text{F} \Rightarrow \text{let's choose } 2.2\ \mu\text{F}$$

$$R_1 = \frac{950 \cdot 136 \cdot 10^{-6}}{2 \cdot 2.2 \cdot 10^{-6}} \cong 29\ \text{k}\Omega$$

FOVP and BUV Sensing Network:

These functions check that the output voltage is within the proper window:

- The fast Over-voltage Protection trips if the bulk voltage reaches abnormal levels. When the feedback network is properly designed and correctly connected, the bulk voltage cannot exceed the level set by the soft OVP function ($V_{out,sovp} = 105\% \cdot V_{out,nom}$). This second protection offers some redundancy for a higher safety level. The FOVP threshold is set 2% higher than the soft OVP comparator reference so that the same portion of the output voltage can be applied to both the FOVP/BUV and feedback input pins (pins 1 and 2).
- The BUV comparator trips when V_{pin1} drops below 76% of the 2.5 V reference voltage ($V_{BUV} = 76\% \cdot V_{REF}$). In the case, the circuit grounds the pfcOK pin (to disable the downstream converter), disables the driver and gradually discharges the $V_{CONTROL}$ signal

until the SKIP level is obtained. When the $V_{CONTROL}$ discharge is complete, the circuit can attempt to recover operation.

However, the BUV function has no action whenever the pfcOK pin is in low state, not to inappropriately interrupt start-up phases.

The LOVP and BUV functions are designed so that a sensing network with the same scale-down factor as for that of the feedback resistors divider, can be used. So, unless your application requires specific needs:

$$R_{buv1} = R_{fb1}$$
$$R_{buv2} = R_{fb2} \quad \text{(eq. 23)}$$
$$C_{buv} = C_{fb}$$

Step 4: Input Voltage Sensing

The NCP1612 monitors the line voltage. In general, resistors are placed between the two line wires to discharge the X2 capacitors (safety requirements). These resistors, $\boldsymbol{R_{X1}}$ and $\boldsymbol{R_{X2}}$ of Figures 1 and 5, scale down the input voltage that can then be easily sensed by the controller.

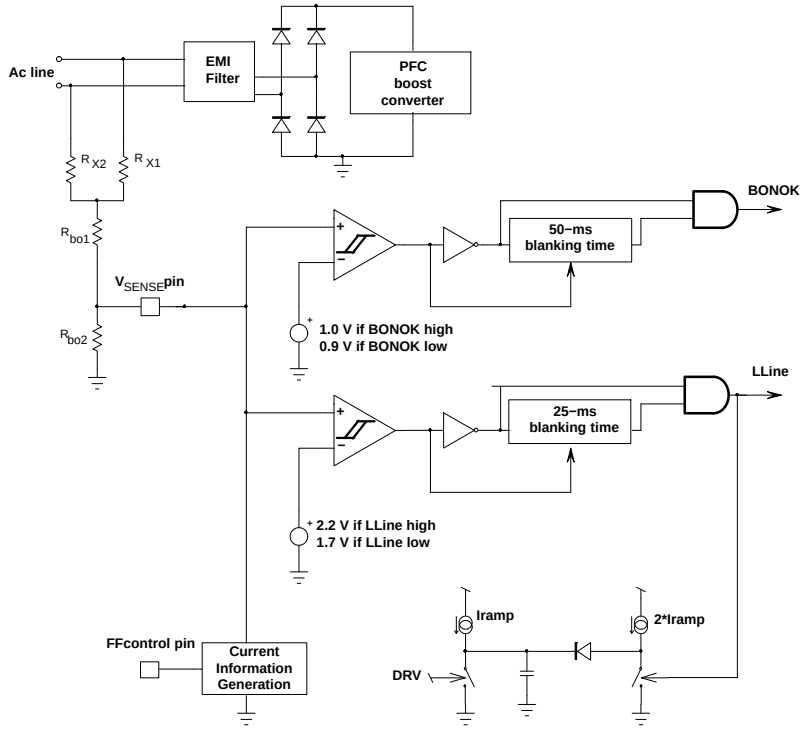


Figure 5. Brown-out and Line Range Detection Block

Assuming these resistors exhibit the same $\boldsymbol{R_X}$ resistance, the voltage applied to V_{SENSE} pin is:

$$V_{SENSE} = \frac{R_{bo2}}{R_{bo1} + R_{bo2}} \cdot \frac{(R_{bo1} + R_{bo2}) \parallel R_x}{R_x + (R_{bo1} + R_{bo2} \parallel R_x} \cdot V_{line}(t) \quad \text{(eq. 24)}$$

This expression simplifies as follows:

$$V_{SENSE} = \frac{R_{bo2}}{R_x + 2R_{bo1} + 2R_{bo2}} \cdot V_{line}(t) \quad \text{(eq. 25)}$$

The brown-out comparator detects a brown-out situation if the $\boldsymbol{V_{SENSE}}$ pin voltage remains lower than (V_{boL} = 0.9 V) for more than 50 ms. In this case, the circuit gradually discharges the control signal until the skip “staticOVP” level is reached and hence, the circuit stops operating.

Operation resumes as soon as the $\boldsymbol{V_{SENSE}}$ pin voltage exceeds (V_{boH} = 1.0 V).

If $(V_{line,rms})_{boH}$ is the minimal rms voltage of the line to enter operation and $(V_{line,rms})_{boL}$ the maximum voltage leading to a Brown-out fault, we have:

$$(V_{line,rms})_{boH} = \frac{R_x + 2R_{bo1} + 2R_{bo2}}{\sqrt{2} \cdot R_{bo2}} \cdot V_{boH} \quad \text{(eq. 26)}$$

$$(V_{line,rms})_{boL} = \frac{R_x + 2R_{bo1} + 2R_{bo2}}{\sqrt{2} \cdot R_{bo2}} \cdot V_{boL} \quad \text{(eq. 27)}$$

Where:

- V_{boH} is the 1.0 V Upper Brown-out Internal Threshold
- V_{boL} is the 0.9 V Lower Brown-out Internal Threshold

R_{X1} and R_{X2} are implemented for safety considerations. In general, they must be selected so that the R_{X1}, R_{X2} series combination ($R_{X1} + R_{X2} = 2R_X$) forms with the X2 EMI capacitors, a time constant less than 1 s. In our case, two 1 MΩ resistors ($R_{X1} = R_{X2} = R_X$ = 1 MΩ) are implemented that together with the selected X2 capacitors, lead to a 1.8 s discharge time constant, which may be too long for most applications (even when considering R_{bo1} and R_{bo2}

resistors that slightly lower the actual X2 capacitors discharge impedance). **In this case, appropriately reduce R_{x1} and R_{x2}.**

Low stand-by losses and noise immunity are the considerations when dimensioning R_{bo1} and R_{bo2}. The first criterion leads to high-impedance resistors to limit the bias current drawn from the line since it can significantly impact the light load losses. On the other hand, very large values can cause noise issues. In practice, (R_{bo2} = 120 kΩ) generally gives good results.

R_{X1}, R_{X2} and R_{bo2} being selected, R_{bo1} can be derived from Equation 26 based on the desired $(V_{line,rms})_{boH}$ level as follows:

$$R_{bo1} = R_{bo2} \cdot \left(\frac{(V_{line,rms})_{boH}}{\sqrt{2} \cdot V_{boH}} - 1 \right) - \frac{R_x}{2} \quad \text{(eq. 28)}$$

In our application if $(V_{line,rms})_{boH}$ is 81 V, ($R_{x1} = R_{x2} = R_x$ = 1 MΩ) and (R_{bo2} = 120 kΩ) , we obtain:

$$R_{bo1} = \frac{120k \cdot 81}{\sqrt{2} \cdot 1.0\ V} - \frac{1000k}{2} - 120k = 6253\ k\Omega \quad \text{(eq. 29)}$$

In practice, 3 · 1800 kΩ resistors in series with a 560 kΩ one are used for a global 5960 kΩ R_{bo1} value which leads to ($(V_{line,rms})_{boH} \simeq 77.5$ V) and ($(V_{line,rms})_{boL} \simeq 69.8$ V).

Remark: A filtering capacitor C_{bo} is recommended between V_{SENSE} pin and ground to protect the pin from possible surrounding noise. It must be small however not to distort the voltage sensed by V_{SENSE} pin. Practically, the time constant it forms together with the sensing resistors must remain lower than the line period divided by 150 ($(T_{line}/150) = (1/(150 \cdot f_{line}))$) that is less than 150 μs in 50 Hz line conditions. If not, the voltage applied to V_{SENSE} pin, may not be proportional to the input voltage but a filtered, phase-shift portion of it, so this should be taken into account when dimensioning the brown-out circuitry and the frequency fold-back behavior.

In our case, the resistive impedance on V_{SENSE} pin can be approximated to R_{bo2}.

Hence,

$$R_{bo2} \cdot C_{bo} < \frac{1}{150 \cdot f_{line}} \Rightarrow C_{bo} < \frac{1}{150 \cdot R_{bo2} \cdot f_{line}}$$

$$= \frac{1}{150 \cdot 120k \cdot 60} \approx 1.0\ nF$$

Step 5: Current Sense Network

The current sense circuitry consists of:

- A Current Sensing Resistor R_{CS}
- A Resistor R_{FF} that Adjusts the Frequency Fold-back Characteristic

=> Computing R_{CS}

The circuit detects an over-current situation if the voltage across the current sense resistor exceeds 0.5 V. Hence:

$$R_{CS} = \frac{0.5}{(I_{L,pk})_{max}} \quad \text{(eq. 30)}$$

Combining this equation with Equation 3 leads to:

$$R_{CS} = \frac{(V_{line,rms})_{LL}}{4\sqrt{2} \cdot (P_{in,avg})_{max}} \quad \text{(eq. 31)}$$

In our practical case,

$$R_{CS} = \frac{90}{4\sqrt{2} \cdot 170} \cong 0.094\ \Omega \quad \text{(eq. 32)}$$

In order to have a bit of margin, a 80 mΩ resistor is selected.

R_{CS} losses can be computed using the equation giving the MOSFET conduction losses where R_{CS} replace $R_{DS(on)}$:

$$(\rho R_{CS})_{max} = \frac{4}{3} \cdot R_{CS} \cdot \left(\frac{(P_{in,avg})_{max}}{(V_{line,rms})_{LL}} \right)^2 \cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,nom}} \right) \quad \text{(eq. 33)}$$

Hence, our 80 mΩ current sense resistor will dissipate about 275 mW at full load, low line.

R_{SENSE} must be applied to the CS/ZCD pin through a resistor (R_{OCP} of Figure 1).

This resistor must be greater than 3.9 kΩ but not too high for noise immunity necessity. Generally, resistors in the range of 5 kΩ give good results.

=> Zero Current Circuitry

The CS/ZCD pin is also designed to receive a signal from an auxiliary winding for Zero Current Detection. As illustrated in Figure 1, this voltage is applied thought a diode to prevent this signal from distorting the current sense information during the on-time and through a resistor R_{ZCD}. This resistor must be high enough so that no more than 5 mA is injected to the CS/ZCD pin. The auxiliary winding being maximum near the line zero crossing and equal to ($(n_{aux}/n_p) \cdot V_{out,nom}$) where respectively, n_{aux} and n_p are the auxiliary and primary turns ratio of the magnetic component, this constraint leads to:

$$R_{ZCD} > \frac{\left(\frac{n_{aux}}{n_p} \cdot V_{out,nom} \right) - V_{CL(pos)}}{5\ mA + \frac{V_{CL(pos)}}{R_{OCP}}} \quad \text{(eq. 34)}$$

Where $V_{CL(pos)}$ is the 9 V minimum level of the CS/ZCD pin positive clamp.

The voltage applied to the CS/ZCD pin is:

$$V_{ZCD} = \frac{R_{OCP}}{R_{ZCD} + R_{OCP}} \cdot \frac{n_{aux}}{n_p} \cdot \left(V_{out,nom} - V_{line}\right) \quad \text{(eq. 35)}$$

This voltage is compared to the NCP1612 750 mV internal threshold for demagnetization detection. For a proper detection, a scale down factor $((R_{OCP}/(R_{ZCD} + R_{OCP})) \cdot (n_{aux}/n_p))$ in the range of 20, generally gives good results.

One way is to select $(R_{OCP} = R_{ZCD})$, (n_{aux}/n_p) in the range of 0.1 and re-arranging Equation 34, compute

$$R_{ZCD} = R_{OCP} > \frac{\left(\frac{n_{aux}}{n_p} \cdot V_{out,nom}\right) - \left(2 \cdot V_{CL(pos)}\right)}{5\ mA}$$

In our application, this leads to $(R_{OCP} = R_{ZCD} > 4.2\ k\Omega)$. We selected: $(R_{OCP} = R_{ZCD} = 4.7\ k\Omega)$. This selection also meets the $(R_{OCP} > 3.9\ k\Omega)$ requirement (see precedent paragraph).

The NCP1612 integrates a leading edge blanking on the CS/ZCD pin that prevents the need for a filtering capacitor. It is still possible to add one but it must be very small not to distort the ZCD signal. Otherwise, the circuit may not turn on at the very valley or worse, inappropriately skip valleys. In other words, check that the ZCD signal is correct and not too filtered. In our application this capacitor should not exceed 22 pF.

=> Computing R_{FF}

R_{FF} adjusts the current level below which the frequency starts to be reduced.

The FFcontrol pin sources a current that is proportional to:

$$I_{FF} = 140 \cdot 10^{-6} \cdot V_{SENSE} \cdot \frac{V_{control} - V_{control,min}}{V_{control,max} - V_{control,min}} \quad \text{(eq. 36)}$$

Since $(V_{SENSE} = 1\ V)$ when $(V_{line} = \sqrt{2} \cdot (V_{line,rms})_{boH})$, we can write:

$$\left(V_{SENSE} = \frac{1\ V}{\sqrt{2} \cdot \left(V_{line,rms}\right)_{BOH}} \cdot V_{line}\right)$$

Further noting that

$$\left(\frac{V_{control} - V_{control,min}}{V_{control,max} - V_{control,min}} = \frac{t_{on}}{t_{on,max}}\right)$$

where $t_{on,max}$ is the 25 μs internal maximum on-time and that

$$\left(I_{line} = \frac{V_{line} \cdot t_{on}}{2 \cdot L}\right)$$

Equation 36 changes into:

$$I_{FF} = \frac{56 \cdot L \cdot I_{line}}{5\sqrt{2} \cdot \left(V_{line,rms}\right)_{BOH}} \quad \text{(eq. 37)}$$

The FFcontrol pin voltage is then:

$$V_{FF} = \frac{56 \cdot R_{FF} \cdot L \cdot I_{line}}{5\sqrt{2} \cdot (V_{line,rms})_{BOH}} \quad \text{(eq. 38)}$$

The PFC stage operates in critical conduction mode (no frequency reduction) when V_{FF} exceeds 2.5 V, that is, as long as the instantaneous line current is higher than:

$$(I_{line})_{th} = \frac{25\sqrt{2} \cdot (V_{line,rms})_{boH}}{112 \cdot R_{FF} \cdot L} \quad \text{(eq. 39)}$$

If as specified, we want to start to reduce the frequency when the line current goes below 450 mA, resistor RFF must be:

$$R_{FF} \cong \frac{25\sqrt{2}}{112} \cdot \frac{(V_{line,rms})_{BOH}}{450 \cdot 10^{-3} \cdot L} = \quad \text{(eq. 40)}$$
$$= \frac{25\sqrt{2}}{112} \cdot \frac{77.5}{450 \cdot 10^{-3} \cdot 200 \cdot 10^{-6}} \cong 272\ k\Omega$$

It may be more convenient to express this threshold as a percentage of the maximal line current which is given by:

$$I_{line,max} = \sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{in,rms})_{LL}} \cong 2.67\ A \quad \text{(eq. 41)}$$

With a 270 kΩ resistor, the circuit starts to reduce the frequency when the line current is about 17% of its maximum value. The minimum 20 kHz operation will be obtained when the FFcontrol pin voltage is about 0.75 V nominal. At that point, the current is (17% · (0.75/2.5)) or 5% of its maximum value. Below this level, the circuit enters skip mode.

Remark: A filtering capacitor C_{FF} is recommended between FFcontrol pin and ground to protect the pin from possible surrounding noise. In atypical application, it must be small however not to distort the voltage sensed by FFcontrol pin. Practically, the time constant it forms together with the sensing resistors must remain lower than the line period divided by 150 $((T_{line}/150) = (1/(150 \cdot f_{line})))$ that is less than 150 μs in 50 Hz line conditions.

In our case, the resistive impedance on FFcontrol pin is R_{FF}.

Hence,

$$R_{FF} \cdot C_{FF} < \frac{1}{150 \cdot f_{line}} \Rightarrow C_{FF} < \frac{1}{150 \cdot R_{FF} \cdot f_{line}}$$
$$= \frac{1}{150 \cdot 270k \cdot 60} \approx 411\ pF$$

Remark: pfcOK Function

The NCP1612 is particularly interesting in applications where the downstream converter is of the forward or half-bridge type, i.e., a converter that takes advantage of a narrow input voltage range. As aforementioned, both the dynamic response enhancer and the soft OVP are of great help in this case by drastically minimizing the bulk voltage deviation under line/load changes. In addition, an optimum sequencing for this application type consists of having the PFC stage started first, the downstream converter entering operation afterwards when the bulk voltage is nominal. The pfcOK pin of the NCP1612 has been designed with the goal of controlling the downstream converter operation:

- The pfcOK pin is grounded until the PFC stage output voltage has reached its nominal level and whenever the NCP1612 detects improper conditions for operation (excessive die temperature, brown-out or bulk under-voltage situations, inappropriate V_{CC} level, latched-off state), i.e., in situations where the PFC stage cannot provide the nominal bulk voltage. In these conditions, the downstream converter should be disabled.
- The pfcOK pin is in high-impedance state otherwise.

The way the pfcOK pin is used, depends on the downstream converter. For instance, the pin can directly ground the feedback signal when the downstream converter must be disabled and release it otherwise[4]. This is generally possible with forward or flyback-type power supplies but generally not with resonant converters. In this second case, the pfcOK pin can instead drive the brown-out pin usually featured by resonant converter controllers. A portion of V_{CC} can then be applied to this pin to fix the high-state level as performed by resistors R_{32} and R_{33} of Figure 7. In this option, it is recommended to protect the pfcOK pin from surrounding noise. This is the goal of C_{18} of Figure 7.

Other possibilities to drive the pfcOK pin exist depending on the downstream converter characteristics.

The pfcOK pin can also serve to latch off of the PFC stage: if the pfcOK pin is pulled-up above 7.5 V, the NCP1612 latches off until a brown-out situation is detected or V_{CC} is dropped below its reset level (5 V typically). Practically, the PFC stage remains off until the PFC stage is unplugged to reset the system.

In the application of Figure 7, a portion of V_{CC} is applied to the pfcOK pin. The V_{CC} latched-off level is:

$$\frac{R_{33} + R_{32}}{R_{33}} \cdot 7.5\ V = \frac{39k + 120k}{39k} \cdot 7.5\ V \cong 30.6\ V \quad \text{(eq. 42)}$$

Please note that the pfcOK pin impedance (about 300 kΩ) is considered as negligible in the calculation.

Layout and Noise Immunity Considerations

The NCP1612 is not particularly sensitive to noise. However, usual layout rules for power supply apply. Among them, let us remind the following ones:

- The loop area of the power train must be minimized
- Star configuration for the power ground that provide the current return path
- Star configuration for the circuit ground
- The circuit ground and the power ground should be connected by one single path
- This path should preferably connect the circuit ground to the power ground at a place that is very near the grounded terminal of the current sense resistor (R_{sense}).
- A 100 or 220 nF ceramic capacitor should be placed between the circuit V_{CC} and GND pins, with minimized connection length
- The components (resistors or capacitors) that program the circuit operation must be placed as close as possible to the pin they drive.
- A filtering capacitor should be placed between the pfcOK pin and ground (e.g., 10 nF) with minimized connection length.

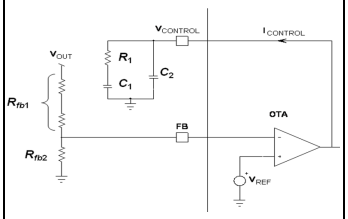
As aforementioned, it is furthermore recommended to place a filtering capacitor on four other relatively high-impedance pins of the circuit: feedback, FOVP/BUV, Input voltage sensing (V_{SENSE}) and FFcontrol to protect the pin from possible surrounding noise. It must be small however not to distort the voltage sensed by these pins. See the corresponding sections for more details.

[4]The pfcOK pin current capability is high but limited. The pfcOK pin can maintain its voltage below 250 mV while sinking 5 mA (see data sheet parametric table). If more current had to be absorbed or if 250 mV was too high to disable the downstream converter some intermediate circuitry would have to be inserted.

Table 1. SUMMARY OF THE MAIN EQUATIONS

Steps	Components	Formulae	Comments
Step1 − Key Specifications	• f_{line}: Line frequency. It is often specified in a range of 47−63 Hz for 50 Hz /60 Hz applications. • $(V_{line,rms})_{LL}$: Lowest Level of the line voltage, e.g., 90 V. • $(V_{line,rms})_{HL}$: Highest Level for the line voltage (e.g., 264 V in many countries). • $(V_{line,rms})_{boH}$: Brown−Output Line Upper Threshold. The circuit prevents operation until the line rms voltage exceeds this level. • $V_{out,nom}$: Nominal Output Voltage. • $t_{HOLD-UP}$: Nominal Output Voltage. • $(\delta V_{out})_{pk-pk}$: Peak−to peak output voltage low−frequency ripple. • $P_{out,max}$: Hold−up Time that is the amount of time the output will remain valid during line drop−out. • $(V_{out,min})$: Minimum output voltage allowing for operation of the downstream converter. • $P_{out,max}$: Maximum output power consumed by the PFC load, that is, 160 W in our application. • $(P_{in,avg})_{max}$: Maximum power absorbed from the mains in normal operation. Generally obtained at full load, low line, it depends on the efficiency that, as a rule of a thumb, can be set to 95%.		
Step2 − Power Components	Input Diodes Bridge Losses	$P_{bridge} = 2 \cdot V_f \cdot \frac{\frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta}}{V_{line,rms}} \approx$ $\approx \frac{1.8 \cdot V_f}{V_{line,rms}} \cdot \frac{P_{out}}{\eta}$	V_f is the forward voltage of any diode of the bridge. It is generally in the range of 1 V or less.
	Inductor	$L \leq \frac{(V_{line,rms})_{LL}^{\ 2}}{2 \cdot (P_{in,avg})_{max}} \cdot T_{on,max}$ $(I_{L,pk})_{max} = 2\sqrt{2} \cdot \frac{(P_{in,avg})_{max}}{(V_{line,rms})_{LL}}$ $(I_{L,rms})_{max} = \frac{(I_{L,pk})_{max}}{\sqrt{6}}$	In our application: $L \leq \frac{90^2}{2 \cdot 170} \cdot 20\mu = 476\ \mu H$ $(I_{L,pk})_{max} = 2\sqrt{2} \cdot \frac{170}{90} \cong 5.3\ A$ $(I_{L,rms})_{max} = \frac{5.3}{\sqrt{6}} \cong 2.2\ A$
	MOSFET Conduction Losses	$(\rho_{on})_{max} = \frac{4}{3} \cdot R_{DS(on)} \cdot \left(\frac{P_{out,max}}{\eta \cdot (V_{line,rms})_{LL}}\right)^2 \cdot$ $\cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,nom}}\right)^2$	$R_{DS(on)}$ is the drain−source on−state resistance of the MOSFET
	Bulk Capacitor Constraints	$C_{bulk} \leq \frac{P_{out,max}}{(\delta V_{out})_{pk-pk} \cdot \omega \cdot V_{out,nom}}$ $C_{bulk} \geq \frac{2 \cdot P_{out,max} \cdot t_{HOLD-UP}}{V_{out,nom}^{\ 2} - V_{out,min}^{\ 2}}$ $(I_{c,rms})_{max} \cong$ $\cong \sqrt{\left(\sqrt{\frac{32\sqrt{2}}{9\pi}} \cdot \frac{(P_{in,avg})_{max}}{\sqrt{(V_{in,rms})_{LL} \cdot V_{out,nom}}}\right)^2 - \left(\frac{P_{out,max}}{V_{out,nom}}\right)^2}$	These 3 equations quantify the constraints resulting from the low−frequency ripple ($(\delta V_{out})_{pk-pk}$ that must be kept below 8%), the hold−up time requirement and the rms current to be sustained.

Table 1. SUMMARY OF THE MAIN EQUATIONS (continued)

Steps	Components	Formulae	Comments
Step3 − Bulk Voltage Monitoring and Regulation Loop	Resistor Divider	$R_{fb2} = \frac{2.5}{I_{FB}}$ $R_{fb1} = R_{fb2} \cdot \left(\frac{V_{out,nom}}{V_{REF}} - 1\right)$ $C_{fb1} \leq \frac{1}{150 \cdot (R_{fb1} \parallel R_{rb2}) \cdot f_{line}}$	I_{FB} is the bias current that is targeted within the resistor divider. Values in the range of 50 μA to 100 μA generally give a good trade−off between losses and noise immunity. C_{FB} is the filtering capacitor that can be placed between the FB pin and ground to increase the noise immunity of this pin.
	Compensation	$G_0 = \frac{(V_{line,rms})_{LL}^{\ 2} \cdot R_{load,min}}{640000 \cdot L \cdot V_{out,nom}}$ $C_2 = \frac{G_0 \cdot \tan\left(\frac{\pi}{2} - \phi_m\right)}{2 \cdot \pi^2 \cdot f_c^{\ 2} \cdot R_{load,min} \cdot C_{bulk} \cdot R_0}$ $C_1 = \frac{G_0}{2 \cdot \pi \cdot f_c \cdot R_0} - C_2$ $R_1 = \frac{R_{load,min} \cdot C_{bulk}}{2 \cdot C_1}$	
	Fast OVP and BUV	$R_{buv2} = R_{fb2}$ $R_{buv1} = R_{fb1}$ $C_{buv} = C_{fb}$	A sensing network identical to the feedback one can be used in the absence of specific needs.
Step4 − Input Voltage Sensing	Input Voltage Sensing Resistors	$R_{bo1} = R_{bo2} \cdot \left(\frac{(V_{line,rms})_{boH}}{\sqrt{2} \cdot V_{boH}} - 1\right) - \frac{R_x}{2}$ $C_{bo} < \frac{1}{150 \cdot R_{bo2} \cdot f_{line}}$	R_X is the resistance of the R_{X1} and R_{X2} resistors for X2 capacitors discharge shown in Figure 5 ($R_X = R_{X1} = R_{X2}$). $(V_{line,rms})_{boH}$ is the line rms level above which the circuit starts operating. V_{boH} is the internal 1 V brown−out reference
Step5 − Current Sense Network	Current Sense Resistor	$R_{CS} = \frac{(V_{line,rms})_{LL}}{4\sqrt{2} \cdot (P_{in,avg})_{max}}$ $(\rho_{RCS})_{max} = \frac{4}{3} \cdot R_{CS} \cdot \left(\frac{(P_{in,avg})_{max}}{(V_{line,rms})_{LL}}\right) \cdot \left(1 - \frac{8\sqrt{2} \cdot (V_{line,rms})_{LL}}{3\pi \cdot V_{out,nom}}\right)$	$(V_{line,rms})_{LL}$ is the line rms voltage lowest level in normal condition (e.g., 90 V). $V_{out,nom}$ is the output nominal level (e.g., 390 V). $(P_{in,avg})_{max}$ is the maximum input power of your application.
	Zero Current Detection	$R_{ZCD} > \frac{\left(\frac{n_{aux}}{n_p} \cdot V_{out,nom}\right) - V_{CL(pos)}}{5\ mA + \frac{V_{CL(pos)}}{R_{OCP}}}$	Placed between R_{CS} and the CS/ZCD pin, resistor R_{OCP} must be greater than 3.9 kΩ but not too high for noise immunity. Generally, resistors in the range of 5 kΩ give good results.
	Current Controlled Frequency Fold−back	$R_{FF} = \frac{25\sqrt{2} \cdot (V_{line,rms})_{boH}}{112 \cdot L \cdot (I_{line})_{th}}$ $C_{FF} \leq \frac{1}{150 \cdot f_{line} \cdot R_{FF}}$	$(I_{line})_{th}$ is the line current level below which the NCP1612 starts to reduce the frequency.

Detailed Schematic For Our 160 W, Universal Mains Application

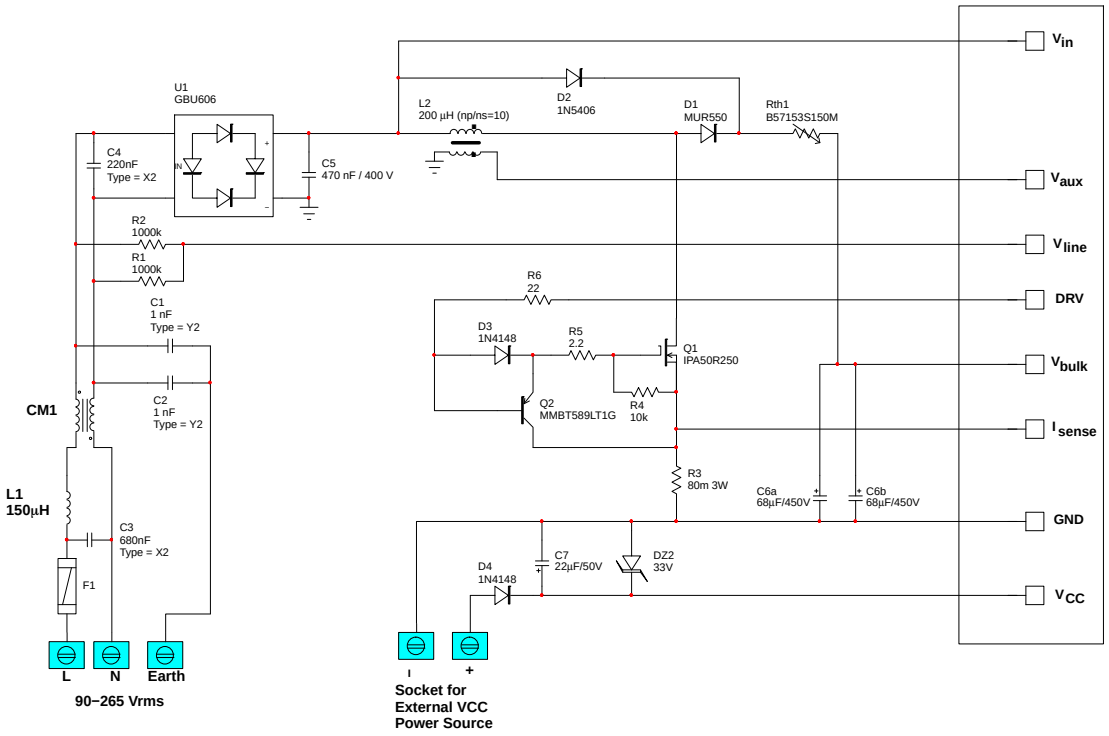


Figure 6. Application Schematic − Power Section

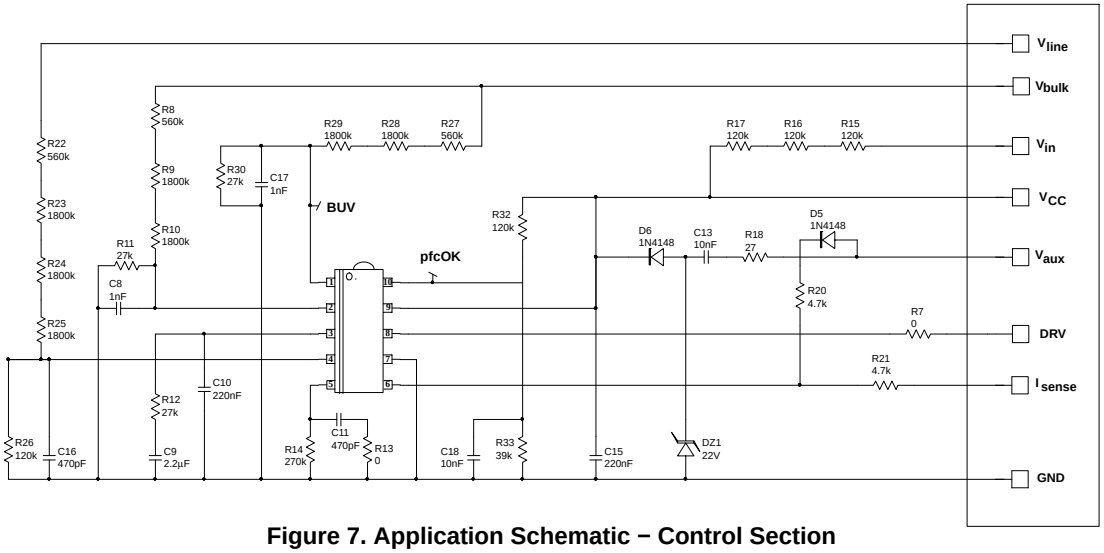


Figure 7. Application Schematic − Control Section

Conclusions

This paper summarizes the key steps when dimensioning a NCP1612-driven PFC stage. The proposed approach being systematic, it can be easily applied to other applications. In addition, an Excel Spreadsheet is available that further eases your design by computing the main components of your application according to the described method [5].

The process has been illustrated by the example of the 160 W, wide-mains evaluation board. You can find details and information on the performance of this board in the NCP1612 Evaluation Board Manual [4]. Implementation details (BOM, GERBER file…) can be found on our web site [6].

More details on the circuit operation can be found in its data sheet [7].

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[1] Joel Turchi, “Safety tests on a NCP1612-driven PFC stage”, Application note AND9046/D, http://www.onsemi.com/pub_link/Collateral/AND9046−D.PDF.

[2] Joel Turchi, “Compensation of a PFC stage driven by the NCP1654”, Application note AND8321/D, http://www.onsemi.com/pub_link/Collateral/AND8321−D.PDF.

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[7] NCP1612/D Data Sheet, http://www.onsemi.com/pub_link/Collateral/NCP1612−D.PDF

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