Electrostatic Discharge and IGBTs

AND9059/D

One of the major problems plaguing electronics components today is damage by electrostatic discharge (ESD). ESD can cause degradation or complete component failure. Shown in Table 1 are the susceptibility ranges of various technologies to ESD. As circuitry becomes more complex and dense, device geometries shrink, making ESD a major concern of the electronics industry.

Table 1. ESD SUSCEPTIBILITY OF VARIOUS TECHNOLOGIES

Device Type	Range of ESD Susceptibility (Volts HBM)
Power MOSFET	100–2,000
IGBT	4,000–8,000
Power Darlingtons	20,000–40,000
JFET	140–10,000
Zener Diodes	40,000
Schottky Diodes	300–2,500
Bipolar Transistors	380–7,000
CMOS	100–2,000
ECL (ICs)	500
TTL	300–2,500

GENERATION OF ESD

Electrostatic potential is a function of the relative position of non−conductors on the list of materials known as the Triboelectric Series, (see Figure 1 from DOD−HDBK−263). Additional factors in charge generation are the intimacy of contact, rate of separation and humidity, which makes the material surfaces partially conductive. Whenever two non−conductive materials are flowing or moving with respect to each other, an electrostatic potential is generated.

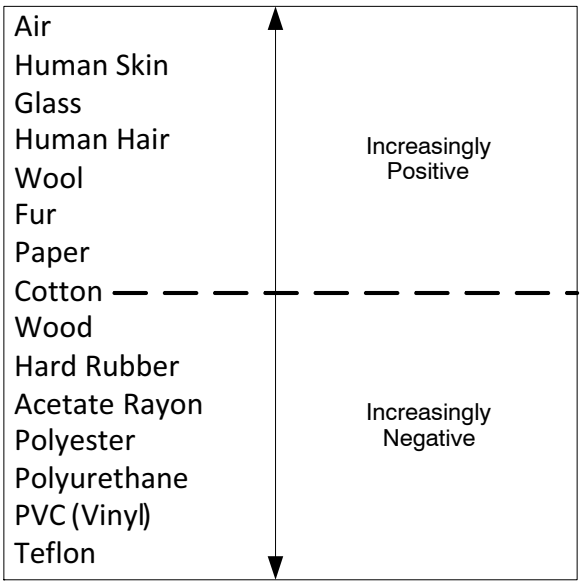

Figure 1. Triboelectric Series − A More Complete Table Appears in DOD−HDBK−263

From Figure 1, it can be seen that cotton is relatively neutral. The materials that tend to reject moisture are the most significant contributors to ESD. Table 2, also excerpted from DOD−HDBK−263, gives examples of the potentials that can be generated under various conditions. From these three Tables, it is apparent that sensitive electronic components can be damaged or destroyed if precautions are not taken, and that the necessary voltages can be easily generated.

Table 2. TYPICAL ELECTROSTATIC VOLTAGES

Means of Static Generation	Electrostatic Voltages	
	10 to 20% Relative Humidity	65 to 90% Relative Humidity
Walking across carpet	35,000	1,500
Walking over vinyl floor	12,000	250
Worker at bench	6,000	100
Vinyl envelopes for work instructions	7,000	600
Common poly bag picked up from bench	20,000	1,200
Work chair padded with polyurethane foam	18,000	1,500

ESD and IGBTs

Being MOS devices, insulated gate bipolar transistors can be damaged by ESD due to improper handling or installation. However, IGBT devices are not as susceptible as CMOS. Due to their large input capacitances, they are able to absorb more charge before being reaching the gate−breakdown voltage. Nevertheless, once breakdown begins, there is enough energy stored in the gate−source capacitance to cause complete perforation of the gate oxide. With a gate−to−emitter rating of VGE = ± 20 V maximum and electrostatic voltages typically being 100 − 25,000 V, it becomes very clear that these devices require special handling procedures. Figure 2 shows curve tracer drawings of a good device, and the same device degraded by ESD.

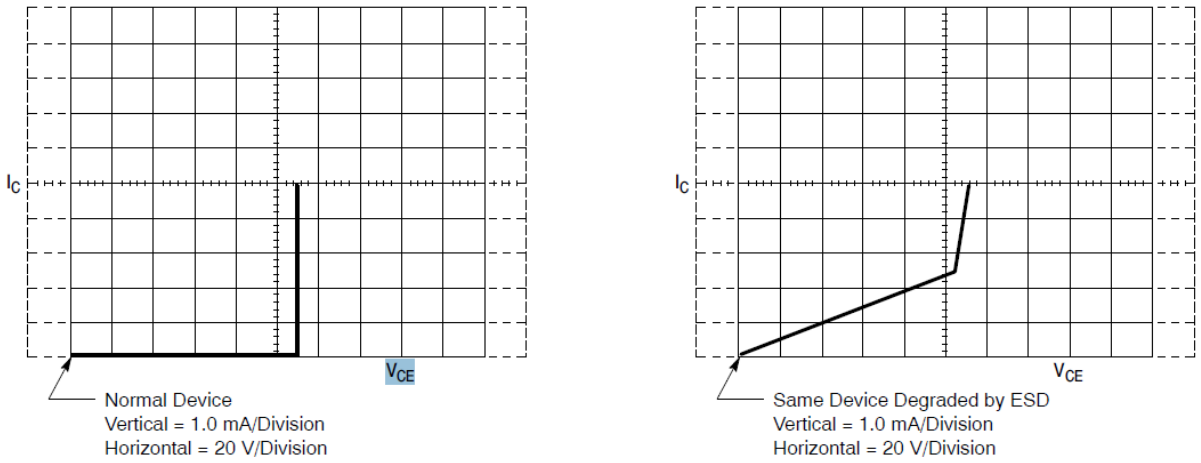

Figure 2. Curve Tracer Drawing of V_{CE} versus I_C of a Good Device (Left), and a Device in which the Gate was Damaged with ESD (Right). The Gate in this Device is Likely a Resistive Short.

Static Protection

The basic method for protecting electronic components combines the prevention of static build up with the removal of existing charges. The mechanism of charge removal from charged objects differs between insulators and conductors. Since charge cannot flow through an insulator, it cannot be removed by contact with a conductor. If the item to be discharged is an insulator (plastic box, person's clothing, etc.), ionized air is required.

If the object to be discharged is a conductor (metal tray, conductive bag, person's body, etc.), complete discharge can be accomplished by grounding it. Grounding of ESD sensitive product, such as IGBTs, must be done carefully, however. Grounding a charged IGBT with a low impedance ground will create an ESD event and could easily damage the device. Grounding of ESD sensitive devices needs to be with a high resistance path to ground, usually in the range of 1 MΩ.

A complete static−safe work station should include a grounded dissipative table top, floor mats, grounded operators (wrist straps), conductive containers, and an ionized air blower to remove static from non−conductors. Dissipative materials are those with properties between conductive and insulating and provide paths to ground in the range of a MΩ to several hundred MΩ. All soldering irons should be grounded. All non−conductive items such as Styrofoam coffee cups, cellophane wrappers, paper, plastic handbags, etc. should be removed from the work area. A periodic survey of the work area with a static meter is good practice and any problems detected should be corrected immediately. Above all, education of all personnel in the proper handling of static−sensitive devices is key to preventing ESD failures.

By following the above procedures, and using the proper equipment, ESD sensitive devices can be handled without being damaged. The key items to remember are:

1. Handle all static sensitive components at a static safeguarded work area.
2. Transport all static sensitive components in static shielding containers or packages.
3. Education of all personnel in proper handling of static sensitive components.

The maintenance of an ESD control program has been documented in the Electrostatic Discharge Association's (ESDA) ANSI/ESD S20.20−2007 and JEDEC's JESD625B.

Test Method:

ESD testing of semiconductors was first defined in military specifications such as MIL−STD−883B Method 3015.1, but today most testing of commercial product is performed using standards maintained by JEDEC or the Electrostatic Discharge Association (ESDA). These two organizations are now maintaining and developing ESD test methods jointly. The earliest and still most widely used ESD test method for semiconductors is the "human−body model" (HBM), ANSI/ESDA/JEDEC JS−001−2011. HBM consists of a network approximating the charge storage capability (100 pF) and the series resistance (1.5 kΩ) of a typical individual (Figure 3). For discrete and very low pin count

devices such as IGBTs, the stress is applied between all possible pin combinations. Test results for IGBTs show that gate−oxide breakdown is most likely, and that reverse−biased junctions are about an order of magnitude more sensitive than forward−biased ones. The damage mechanism, which can be identified through failure analysis of shorted or degraded samples, is usually oxide puncture or junction meltthrough.

More recently the “charged device model” (CDM) has been found to represent the type of stress which semiconductor components experience in automated factories. CDM emulates a semiconductor device becoming charged and then discharging to a grounded, low resistance, surface. The test is usually performed using a field induction method to bring the device being tested to a high potential. A simplified schematic of the tester is shown in . The device being tested is placed in the leads up position on top of a thin insulator which sits on a metal field plate whose potential can be adjusted. The device under test is brought to a high potential by changing the potential of the field plate. The device is then rapidly grounded by touching a device pin with a grounded pogo pin. This produces a very fast, ~ 1 ns, pulse whose peak current can be from 1 to 10 of amps, depending on the size of the unit being tested. Failures from CDM are typically oxide failures rather than junction damage. The CDM test is documented in two standards, JEDEC’s JESD22−C101E and ESDA’s ANSI/ESD S5.3.1−2009. These two standards are very similar, but differences in the test setup and calibration modules mean that test values from the two methods while similar in magnitude are not equivalent. Efforts are underway to merge these standards.

A third ESD test method which has been used widely is the “Machine Model”, (MM). The MM has a circuit diagram similar to HBM, but the capacitance is 200 pF and the 1.5 kΩ resistor is replaced by an implied inductance of about 0.8 μH. (The inductance is implied because that is what is needed to obtain the required waveform frequency with 200 pF of capacitance.) In recent years the MM has fallen out of favor because it gives very little more information than the HBM test and is not longer recommended for qualification. MM failure levels are typically about an order of magnitude lower than HBM failure levels but can range from a factor of 3 to a factor of 30.

Significance of Sensitivity Data

The Industry Council on ESD Target Levels (a collection of ESD experts from a wide ranging group of electronics companies) has done extensive studies of what ESD levels are needed to manufacture electronic systems with high yield. (White Paper 1: A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements and White Paper 2: A Case for Lowering Component Level CDM ESD Specifications and Requirements) They found that if integrated circuits had HBM levels of 500 V or higher and CDM levels of 250 V and higher they can be handled in manufacturing lines with basic ESD control without yield loss. Without basic ESD control in the factory even HBM levels of 8000 V can have yield loss. Today, **onsemi**’s IGBTs have HBM levels of 8000 V or more and CDM levels of 2000 V. With these ESD levels **onsemi**’s IGBTs can be handled very safely in any manufacturing facility with the basic ESD controls in place required for manufacturing products containing modern integrated circuit products.

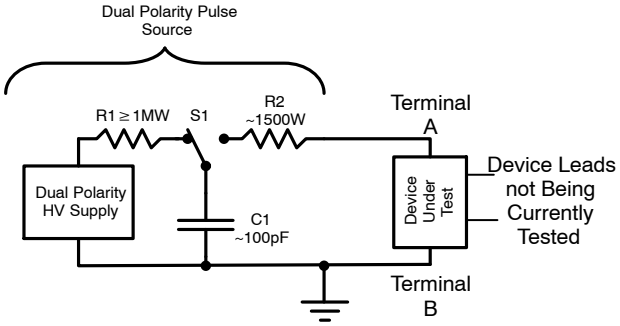

Figure 3. Simplified HBM test schematic

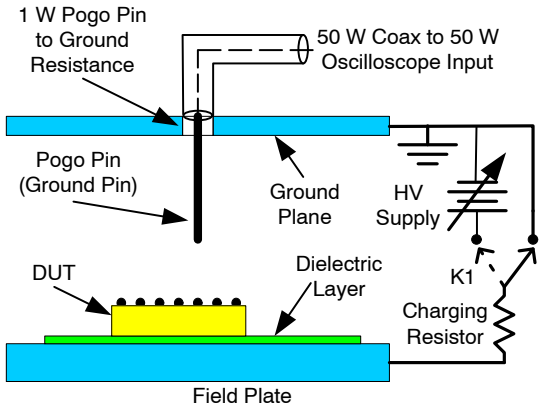

Figure 4. Simplified CDM tester schematic

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