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Designing High-Efficiency LED Driver Circuits Using the NCL30051

APPLICATION NOTE

Introduction

Lighting represents about 1/6th of global electricity consumption. In advanced economies, this ratio may be significantly higher due to high commercial usage. For example, in the US it is estimated that only 28% of the energy consumed for lighting is for residential usage. The bulk of energy consumption for lighting is in commercial applications such as offices, restaurants and retail. In this context, new lighting sources that provide similar illumination to traditional ones, but at much lower energy consumption, are critical to eco-friendly practices that seek to reduce energy consumption.

Solid state lighting using High Brightness LEDs (HB-LEDs) has been gaining popularity since it provides high efficacy (lumens/W) and offers the promise of long lifetime while reducing maintenance cost. Both are critical for commercial lighting where there are long operating hours and in many cases, lighting that might not be easily accessible for maintenance. Moreover LEDs turn on rapidly unlike some light sources and are easily dimmed allowing better control of the amount of light needed. Ease of control is another way of saving energy since the light source can be controlled to take advantage of daylight harvesting as well as occupancy factors.

Unlike incandescent lamps, LEDs do pose some specific challenges. They require a regulated DC current for optimal operation so cannot be directly powered from the ac line. Other light sources such as fluorescent lamps and low voltage halogen bulbs also cannot be powered directly from the ac line and require a magnetic or electronic ballast to transform the ac line into an appropriate signal for the lamp. LEDs require a new class of power electronics systems, viz., LED drivers and LED power supplies. These come in many forms and flavors. This is especially true for commercial lighting as there are a broad range of different lighting applications such as cove, low bay, task, accent, spot, down lighting, architectural, and high bay to name a few and each application has different considerations. Many of these applications require significant light output so a large number of LEDs may be needed. A high bay light for a warehouse may require more than 100 LEDs to generate the lumen output requirement.

A large portion of LED drivers are designed to operate from an ac voltage input – this allows the LED light source to be easily retrofitted into the existing building infrastructure. The majority of these ac input drivers require galvanic isolation between primary and secondary and many also require conformance to harmonic reduction or power factor standards. This conformance is achieved through power factor correction (PFC) circuits.

We can classify these drivers into three basic categories:

- Single output AC line powered constant current (CC) drivers intended to drive an array of LEDs. The array may be a single string of LEDs or a series-parallel combination of LEDs. The driver has a constant voltage (CV) mode that is there to limit the maximum output voltage of the driver in the event that the LEDs are inadvertently disconnected. This will be referred to as Type 1 driver and is illustrated in Figure 1.
- The second type of configuration utilizes a front end LED power supply which is connected to the ac line and provides a regulated interim bus voltage. This bus voltage is then provided to one or more DC-DC converters which accurately control the current in a string of LEDs. This approach provides greater control and flexibility at the expense of additional circuitry and cost. A common example of this is cove lighting system where a safe low voltage bus (such as 24 Vdc) is provided to each fixture. This configuration is referred to as Type 2 for the rest of the document. The front-end AC-DC converter of this configuration will be referred to as LED power supply in this document.
- A third variation, though less frequently employed, comprises multiple Type 1 drivers in a single housing, with each driver driving one string each. This configuration eliminates the current sharing issue amongst parallel strings of LEDs since each string is independently regulated. These are most often seen in applications that have to drive more than 100 W of LEDs.

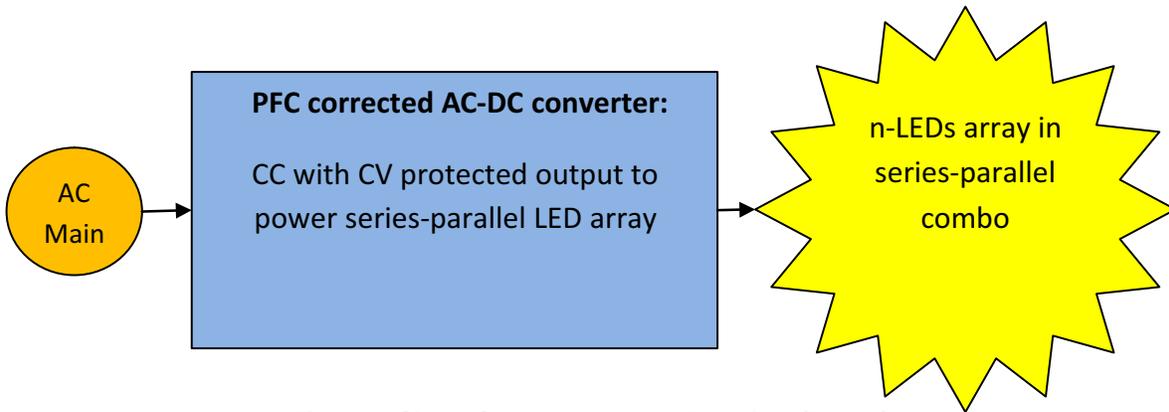


Figure 1. Single Stage Integrated LED Driver (Type 1)

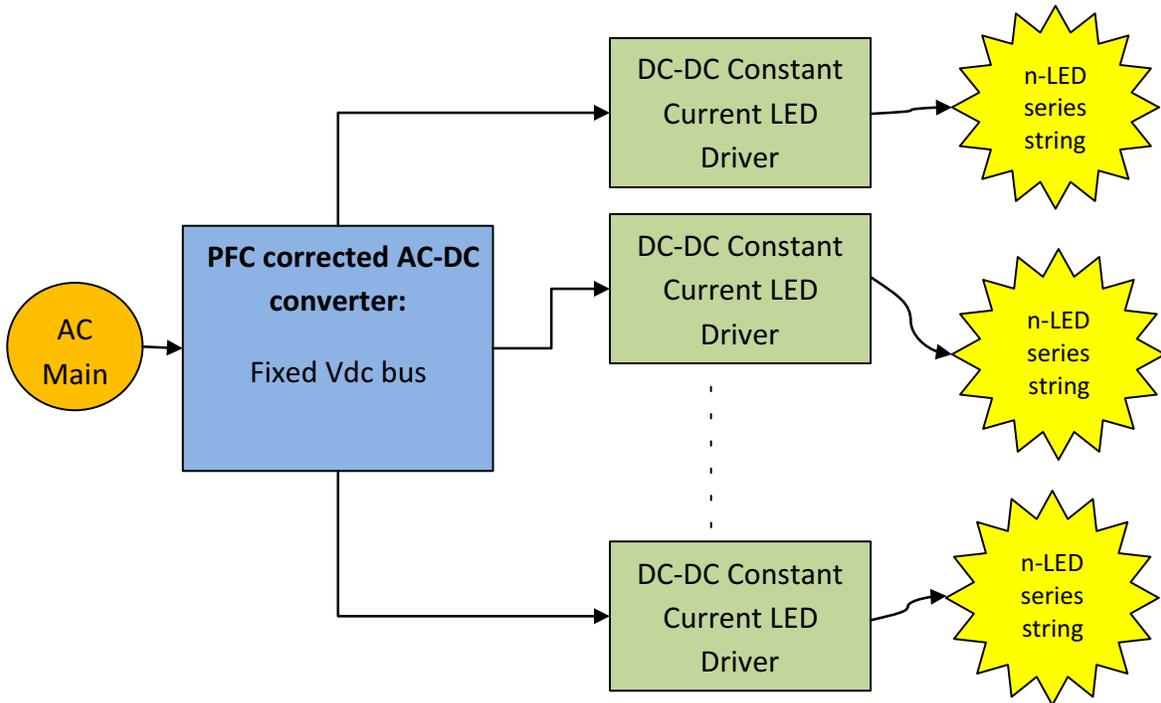


Figure 2. Two-Stage LED Driver with Single Front-End Converter (LED Power Supply) – Type 2

LED Driver Requirements

The LED driver needs to provide a well-regulated DC current to the LEDs in any given configuration in order to ensure the required lumen output, color and long operating life of the LEDs. A typical ac voltage input LED driver must meet following requirements:

- Provide accurate drive current for the LEDs in the chosen configuration.
- Provide galvanic isolation between primary and secondary.
- Regulate against any LED voltage variations and potential shorting of one or more LEDs in a string
- Regulate the LED current for any input voltage level within the specified operating range.
- Provide protection against overvoltage, short circuit, overload, and other abnormal operating conditions.
- Provide harmonic reduction and power factor correction (if required) to meet regulatory requirements.
- Operate at high conversion efficiency and limit the heat generation and temperature rise.

For drivers intended for commercial lighting applications, additional requirements include operation over a wide temperature range and long lifetime. These may also have specialized dimming control protocols to interface with building control systems.

Dimming Considerations

There are two principle methods of dimming LEDs (analog and digital) and each method has its advantages and disadvantages as well as an impact on the overall driver design. LEDs are diodes and their forward voltage varies non-linearly with current. The light output is proportional to current and over certain regions of current it can be approximated in a linear relationship. This relationship varies depending on the LED manufacturer as well as the design of a specific LED type. It also varies with temperature and from part-to-part and lot-to-lot.

In analog dimming, the output current of the LED driver is reduced in order to achieve reduced light output. As the current is reduced, the forward voltage of the LEDs as well as the junction temperature of the LED is reduced. As a result, a 50% reduction in LED current may not result in a 50% reduction in light output so the dimming curve is not linear. Moreover, reducing the current by 50% will also reduce the forward voltage of the LED so the power will be reduced by more than 50%. Thus we see that one of the key advantages of analog dimming is that the efficacy of the LEDs (lm/W) improves as the LEDs are dimmed. Additionally, analog dimming results in a variation of the LED forward voltage that can be about 20–25% as the current is varied from 100% to 10%. For example a typical white LED may have a forward voltage of 3.4V at 700 mA. This drops to 2.95 V at 70 mA. One additional limitation of analog dimming is that the color of the LED can experience color point shift when the current is changed over a wide range so is not typically used in applications where the color temperature must be tightly controlled.

The second option is digital dimming where the LED current is pulsed between a regulated current and zero at a high frequency with a controllable duty cycle. The frequency of the pulse train is high enough for the human eye to not perceive the changing amplitude as flicker, yet low enough not to interfere with the stability of the LED driver circuit (typically in the range of 200 Hz to a few kHz). The dimming is achieved by controlling the duty cycle of the pulse (lower the duty cycle for more dimming). With PWM dimming, the color temperature of LED is maintained as the drive current (when present) is always constant and at a regulated level. There are other digital modulation schemes that can also be used to implement dimming but the principle is similar. In digital dimming, the LED forward voltage is fairly constant and only varies by the change in RMS junction temperature.

While digital dimming adds increased complexity to the circuit implementation (in terms of a series switch and its control), it offers significant benefit in better linearity, more

predictable lumen output and a well defined color point for the LEDs.

NCL30051 LED Driver IC

The NCL30051 is designed for LED lighting applications that work from an ac input and require power factor correction and high conversion efficiency. The NCL30051 provides an innovative control mechanism compared to traditional two stage power conversion architectures. This unique regulation scheme offers extreme simplicity for certain applications.

Traditional 2-stage converters have independent control loops for the PFC stage and the step-down stage, allowing each converter output to be regulated on its own. The half-bridge resonant (HBR) converter topology offers significant efficiency and EMI advantages for the second stage conversion over a more conventional flyback topology. However, conventional HBR topologies such as LLC involve varying the switching frequency to regulate the output and hence add further complexity to PFC–PWM combination controllers.

In contrast, the NCL30051 simplifies the overall approach significantly by implementing the HBR approach for the second stage converter at a fixed frequency. This simply means that the second-stage converter now operates in a non-regulating fixed-ratio voltage conversion mode. The implication of this approach is that any output regulation required has to be provided by adjusting the output of the PFC front-end converter. The benefits of this approach can be summarized as follows:

- Low pin-count of controller combines strong feature set
- Low external component count
- ZVS of the second stage FETs without any tuning requirements
- High efficiency facilitates improved thermal performance
- Low EMI and easy filtering due to fixed frequency
- Facilitation of synchronous rectification control design
- Easier design of magnetic components (esp. Resonant transformer and inductor)

Further details on theory of operation of the NCL30051 are provided in the data sheet.

Figures 3 and 4 provide the block diagram view of the differences between traditional control schemes and the control scheme offered by the NCL30051. As these figures indicate, the NCL30051 approach is applicable to both type 1 and type 2 LED driver configurations identified in Figures 1 and 2.

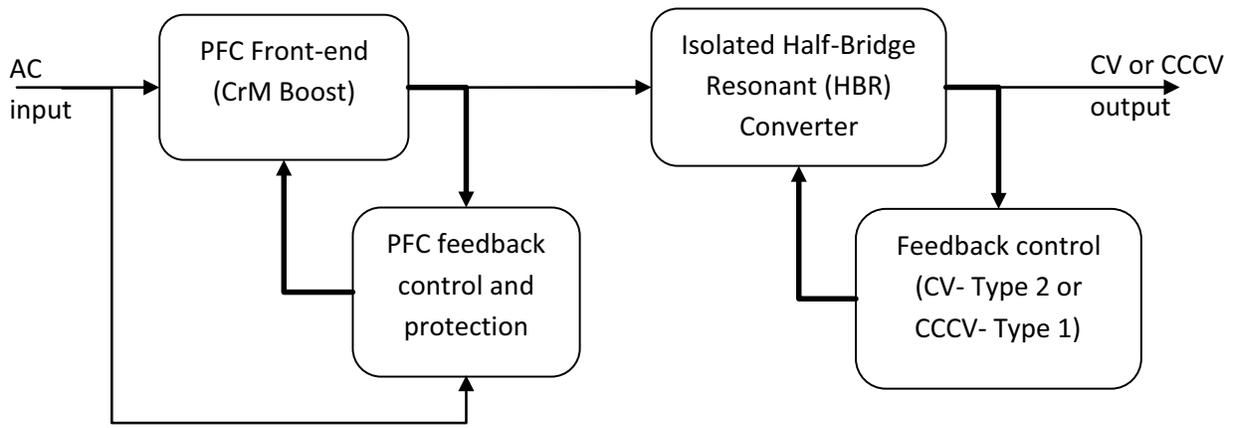


Figure 3. Traditional Two Stage Approach for High-Efficiency LED Driver

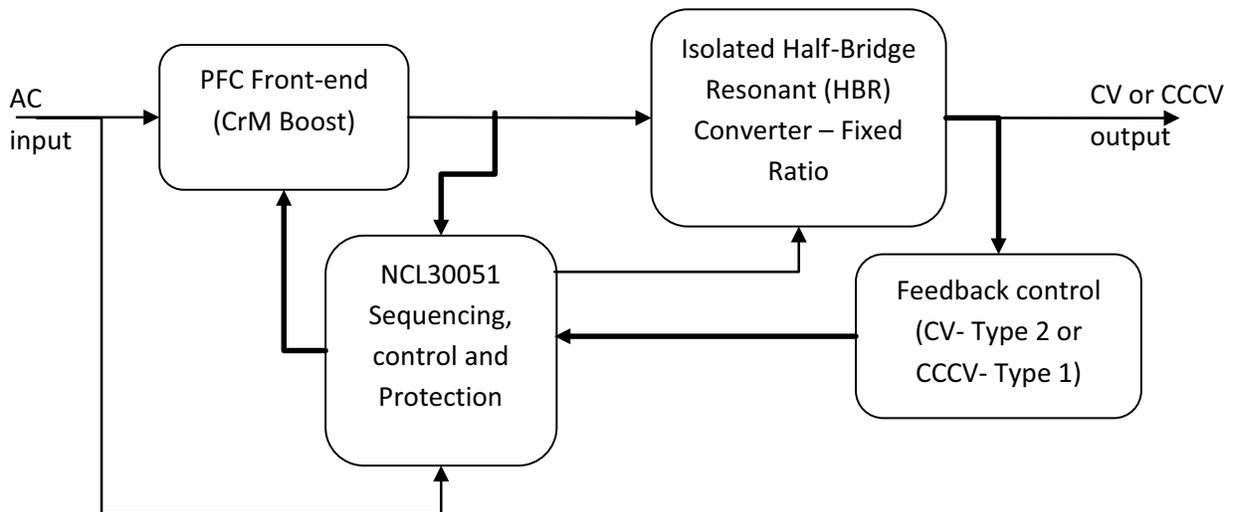


Figure 4. Simplified Control Scheme Offered by NCL30051

The novelty of the NCL30051 architecture means that the design procedure is different from traditional 2-stage designs. The complexity of this design is higher for type 1, so the step-by-step design procedures are provided first for the simpler option (type 2) and then for the more complex one (type 1). However, all the required details are independently maintained in each design procedure to keep them self-contained. For readers less familiar with power electronics, it may make sense to go through the type 2 procedure first; others may go to the relevant design procedure directly.

Design Procedure for Type 2 LED Driver Front-end using NCL30051

The step-by-step design procedure for the NCL30051-based LED power supply is provided in this section. In case the LED driver (Type 1 circuit) is being designed, the same design procedure and principles apply, albeit with an added complexity related to the CCCV circuit

and variations in the voltage, which is covered in the latter part of this document.

[Note: Steps 1–3 can be skipped if specifications for the LED power supply are readily available]

Step 1: Identify the load requirements

The first step is to understand the load characteristics. This includes:

- Identifying the LEDs to be used
- What current to drive each LED with
- What type of series-parallel array of LEDs will be employed to get required light output

Based on the above information, the load voltage and current characteristics will be more accurately characterized and will be used to develop the driver design.

An example is given below (and used throughout this design procedure to illustrate the design steps).

- LEDs used: OSRAM Golden DRAGON Plus LW W5AM (White LEDs)
- Drive current per LED: 350 mA [Note: these LEDs are capable of being driven at anywhere between 100 mA and 1 A of current, but specified operating point is 350 mA.]
- LED strings: Array of (m=) 3 LED strings in parallel with each string containing (n=) 12 LEDs in series is chosen for this application. The resultant total LED driver output current (I_{out}) is 1.05 A (3×0.35 A). [In this approach (type-2), current in individual strings is controlled using a DC-DC stage for each string.]

$$I_{out} = m \cdot I_{LED} \quad (eq. 1)$$

Step 2: Driver output voltage range and selection of LED power supply output voltage

Once the LEDs, their drive current and string arrangement are chosen, the next step is to calculate the output voltage range of the driver. Based on the LED specifications, determine the [VF_{min}, VF_{nom} and VF_{max}] values for the chosen LEDs at the selected drive current. In the present case, these values are [2.7, 3.2 and 3.7] V at 350 mA drive current. Thus, the V_{string} [min, nominal and max] values become [n*VF_{min}, n*VF_{nom} and n*VF_{max}] or [32.4, 38.4 and 44.4] V. The driver max and min voltage are thus, 44.4 V and 32.4 V, respectively. These values are based on the static LED drive current of 350 mA. If analog dimming is used, a wider range of VF values is applicable, thus widening the driver output range. There is a VF reduction of about 10–15% as the LED current is reduced from 350 mA to 50 mA (less than 10:1 range). In addition, there is also a temperature dependence of the VF where the value of VF drops by about 0.25 V when the temperature rises from 25°C to 100°C. All these factors require a slight widening of the V_{out} range compared to the calculated values above. In this case, the V_{out} range is changed to (V_{o-min}=) 31.4 to (V_{o-max}=) 44.4 V. The V_{o-ratio} is calculated to be (44.4/31.4 = 1.41).

$$V_{string-max} = n \times VF_{max} \quad (eq. 2)$$

$$V_{string-min} = n \times VF_{min} \quad (eq. 3)$$

$$V_{o-max} = V_{string-max} \quad (eq. 4)$$

$$V_{o-min} = V_{string-max} - V_{margin} \quad (eq. 5)$$

$$V_{o-ratio} = \frac{V_{o-max}}{V_{o-min}} \quad (eq. 6)$$

The LED power supply output voltage has to be chosen so that the DC-DC driver can support the V_{out} range. The most suitable and commonly implemented topology for the DC-DC driver is the buck converter (though boost/buck-boost/SEPIC variations are also feasible). For the buck converter implementation, the output of the LED power supply (V_{dc-bus}) has to be always higher than V_{out} with enough margin for the maximum duty ratio of the DC-DC

buck regulator selected. In the present case, the value of V_{dc-bus} is 50 V assuming the maximum duty ratio is 0.9.

$$V_{dc-bus} \geq \frac{V_{o-max}}{D_{max}} \quad (eq. 7)$$

Step 3: LED power supply power rating

The next step is to calculate the power rating of the front-end based on the calculated values of V_{dc-bus} and I_{out}. Since the front-end is expected to deliver rated current (I_{out}) at V_{dc-bus} and a high duty cycle, the total power rating is given by the following equation where η represents the efficiency of the DC-DC converter stage at maximum load.

$$P_o = I_{out} \times V_{dc-bus} \times D_{max} \div \eta \quad (eq. 8)$$

In this case, the power rating is (1.05 × 50 × 0.9)/0.95 = 55.3 W. Taking the power losses and design margin into account, the front-end (Input bridge and PFC circuit) should be designed for slightly higher power – 60 W in this case.

Step 4: Input Voltage Range and PFC output voltage (minimum) selection

The next step is to identify the input voltage range and plan the PFC output voltage based on that information. Typically, the LED drivers are designed to operate for one of the following four input voltage conditions:

1. Single (Low) voltage range (85–135 Vac) – This would be applicable to drivers for single geographic markets such as North America and Japan
2. Single (High) voltage range (170–265 Vac) – This would be applicable to Europe, China and other regions which use 220/240 Vac lines.
3. Universal input range (85–265 Vac) – This range is used to standardize designs for application anywhere in the world.
4. Dual voltage range (115 Vac residential and 277 Vac commercial/industrial lighting applications – resultant range for a single driver without range switch is 90–305 Vac factoring in the tolerances). This covers the higher commercial voltage range used in the United States.

The single voltage range (1 or 2 above) makes the driver implementation easier. The low range reduces the voltages required for all stages of the driver and the high range reduces the level of currents being processed. However, currently many designs are specified for universal or dual voltage ranges and the resulting complexity is not too difficult to handle with ICs such as NCL30051. Focusing on conditions 3 and 4, it can be summarized that the maximum input ac voltage for LED driver can be 265 Vac (for residential applications) or 305 Vac (for industrial/commercial lighting).

The maximum input ac voltage helps determine the minimum value of the PFC output voltage (V_{bulk}) for this application. In normal PFC applications, this voltage is set to a fixed value anywhere between 380 V to 400 V and there

are no significant component stress effects of the range of this choice. However, with the NCL30051 application, the V_{bulk} range can be wide based on the output variations, so it makes sense to start with the lowest possible V_{bulk} as the minimum voltage. The minimum possible V_{bulk} is given by:

$$V_{bulk-min} = V_{in-max}(rms) \times \sqrt{2} \quad (eq. 9)$$

Applying this equation to V_{in-max} of [265, 305] Vac results in $V_{bulk-min}$ of [375, 431] Vdc. With some margin added, the chosen values are 380 and 435 V respectively. It

is pertinent to observe that the ripple present on the PFC output does not have any impact on the minimum bulk voltage choice given by Equation 9. This is because the instantaneous ripple value at the peak of the rectified line voltage is always zero as illustrated in . The instantaneous ripple valley occurs at 45° angle after the zero crossing of the line voltage and hence the boost relationship between input and output is always maintained for the choice of V_{bulk} provided by Equation 9.

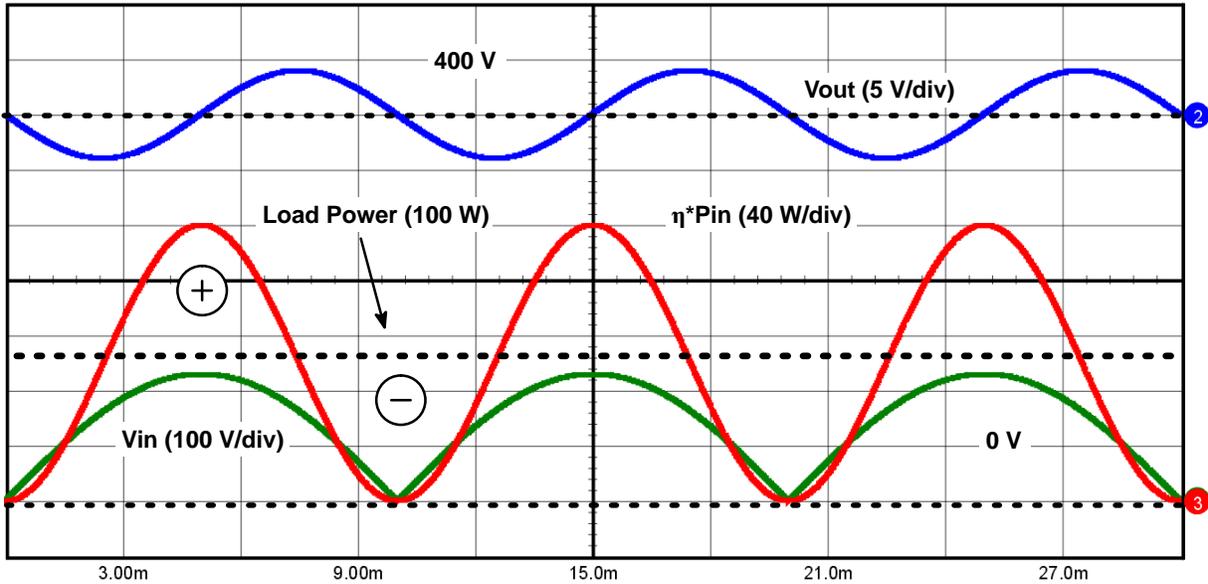


Figure 5. Relationship Between PFC Output Ripple and Input Voltage

Step 5: Determine the range of PFC output voltage required

The next step is to check the range of the required PFC output voltage in order to meet the output voltage range requirements. In the LED power supply (Type-2 application), the front-end does not see much variation in the PFC output voltage since the regulation is handled by the DC-DC stage at the back-end. In this case, the PFC output voltage remains relatively constant at the selected value from Equation 9. Based on the losses of the HBR stage and the load variation, there will be some variation in V_{bulk} that has to be designed for. As a result, the $V_{bulk-max}$ value has to be chosen higher than the $V_{bulk-min}$ by about 15% to include design margin.

$$V_{bulk-max} = V_{bulk-min} \times 1.15 \quad (eq. 10)$$

The calculated values for $V_{bulk-max}$ are [437, 500] Vdc for the two voltage ranges discussed in the previous step.

The value of $V_{bulk-max}$ determines the stress level of all major components in the PFC section of the circuit. At 500 V (corresponding to V_{in-max} of 305 Vac), the 600 V rated devices (FET and boost diode) are usable with more than 15% margin and that level of derating is usually acceptable for such applications. However, the bulk capacitor rating has to be considered and the most effective solution is to use series combination of lower (300/400 V)

rated capacitors for these applications. For the 265 V max application, the use of single 450 V rated capacitors is marginally acceptable. The NCL30051 is designed to handle this voltage level.

Step 6: Design of bulk capacitor

The bulk capacitor design follows the choice of $V_{bulk-max}$. Naturally, the voltage rating of the bulk capacitor has to be higher than the sum of $V_{bulk-max}$ and half the peak-to-peak ripple voltage, which is given by:

$$V_{ripp(p-p)} = \frac{P_o}{(2 \cdot \pi \cdot f) \times V_{bulk-max} \times C_{bulk}} \quad (eq. 11)$$

Normal rule of thumb is to use about 1 μ F output capacitance for 1 W of output power. Applying this rule and choosing a 47 μ F capacitor for this application, results in a peak-to-peak ripple of [7.8, 8.8] V for $V_{bulk-max}$ of [437, 500] V. This ripple is attenuated by the HBR converter and results in a corresponding ripple at the output of the front-end LED power supply. The choice of bulk capacitor has to be revisited after the HBR design to ensure the required ripple specification at the output is met. The rms current in the bulk capacitor is provided in [1] and needs to be calculated to ensure the chosen capacitor can handle this current without heating up. As mentioned in previous step,

for the higher $V_{\text{bulk-max}}$ value, it is preferable to go with two lower voltage rated series capacitors (100 μF , 300 V) which give an equivalent value of 47 μF .

Step 7: Design of PFC Diode

The PFC diode design is not very constrained in this approach since the diode turns off at zero current and does not face significant reverse recovery phenomenon. With the present design, a 600 V ultrafast diode can be chosen with sufficient design margin. The required current rating is given by:

$$I_{d(\text{avg})} = P_o / V_{\text{bulk-min}} \quad (\text{eq. 12})$$

In order to improve the efficiency, low V_f is needed and can be achieved by selecting a slightly higher current rated device (e.g. 3 A device – MURS360 – for the present application)

Step 8: Design of PFC FET

The PFC FET design also follows the standard procedure used in CrM PFC design. Again, the voltage ratings for the present example facilitate the choice of 600/650 V FET with sufficient derating.

Step 9: Design of PFC Inductor

Design of the PFC inductor follows the design procedure provided in the application literature for CrM PFCs [2]. Note that additional winding is needed on the PFC inductor for Zero Crossing Detection (ZCD).

Step 10: Design of other PFC circuit elements

Like the previous three design steps, this step also follows the traditional CrM controller design. Since the PFC section of the NCL30051 is similar to the NCP1608, the choice of components for current sense, feedback, ZCD, On-time control, etc. follow the design procedure in the NCP1608 application note [2]. The design tool for NCP1608 [3] is an excellent place to start for selecting appropriate component values for this application.

Step 11: Step-down ratio calculation for HBR converter

The HBR converter step-down ratio is decided by the following equation:

$$\text{Ratio}_{\text{HBR}} = \frac{V_{\text{bulk-min}} \times \text{Eff}_{\text{conv}}}{V_{\text{dc-bus}}} \quad (\text{eq. 13})$$

Where Eff_{conv} is the conversion efficiency of the HBR converter, typically >0.95 , which accounts for duty cycle loss in switching transitions and other parasitics. For the present cases, the HBR ratio comes out to [7.22, 8.26] for $V_{\text{bulk-min}}$ of [380, 435]. The regulation loop ensures that the V_{bulk} is adjusted up or down in order to maintain the $V_{\text{dc-bus}}$ in case either the actual ratio or the assumed conversion efficiency is non-optimal.

The output ripple at $V_{\text{dc-bus}}$ is equivalent to the bulk voltage ripple (given by Equation 10) divided by the HBR ratio. In the type-2 LED power supply application, this ripple is not critical as long as the minimum voltage is sufficient to provide required headroom for the secondary DC-DC LED driver.

Step 12: HBR transformer design

The transformer design for the half-bridge resonant converter follows based on the step-down ratio calculated in the previous step. The transformer turns ratio is derived by dividing the HBR ratio by two (since the half-bridge converter steps down half the input voltage every half-cycle). Thus, for the two cases, the transformer turns ratio would be [3.61, 4.13]. The actual transformer design is usually an iterative process, where the required number of primary and secondary turns is selected for a specific core to prevent core saturation. After that, the required wire size based on the current levels is determined and the fit of these wires into the available winding window is confirmed.

For the HBR transformer, the magnetizing inductance (L_m) and the leakage inductance (L_{lk}) are critical parameters that play a significant role in circuit operation (achieving resonance and zero voltage switching). However, the convenient approach is to take whatever leakage inductance that can be achieved through normal winding techniques and design the rest of the resonant tank (viz. resonant capacitors) to achieve the desired performance. For reducing magnetizing inductance, there is an option to gap the core that can be exercised. This approach keeps the transformer complexity low and works very well in the NCL30051 application, since there is no frequency modulation of the HBR stage.

Step 13: HBR Resonant Circuit operation

The LLC resonant converter operating at the resonant frequency provides the significant benefits of lowest EMI and highest efficiency [4]. In order to operate in this mode, the switching frequency has to be fixed to match the resonant frequency of the series resonant tank. This frequency is given by:

$$f_s = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{lk} \cdot C_r}} \quad (\text{eq. 14})$$

This equation assumes that the leakage inductance value is sufficient not to require an external resonant inductor.

The resonant tank has to operate at a frequency that is set by the NCL30051 clock to achieve true resonant operation. The specified clock frequency range of the NCL30051 is from about 30 kHz to 150 kHz (corresponding half-bridge clock frequency range is 15 kHz to 75 kHz) and is settable using a single capacitor. As an example, a half-bridge frequency of 35 kHz is chosen. This represents a good compromise between requiring resonant elements (L or C) which are too large (when frequency is too low) and possibly high switching and core losses (when frequency is too high).

The value of C_r can be calculated from the above equation, once f_{sw} and L_{lk} are known. In this example, with an L_{lk} of 100 μH , the calculated value of C_r is 0.2 μF , which is an acceptable practical value.

Step 14: HBR FET selection

The FET selection for the HBR stage is straightforward. The voltage rating of the FETs equals $V_{\text{bulk-max}}$ and

adequate derating can be achieved by choosing commonly available 600/650 V FETs. The R_{ds} /current rating of these FETs is the next consideration. In the HBR topology, there are no turn-on switching losses, so the output capacitance of the FETs (C_{oss}) does not hinder the FET choice – so in this respect, low R_{ds-on} devices are preferred. However, the topology does require fast turn-off to limit turn-off losses. The FET should be chosen while keeping in mind the drive capability of the NCL30051 half-bridge driver (which is 100 mA peak). As discussed in the data sheet, if the drive capability needs to be increased, a simple discrete gate driver circuit can be incorporated into the design.

Step 15: HBR rectifier selection

The output rectifiers in the HBR topology operate in a center-tapped half-wave rectification mode and with no output inductor, each device sees twice the output voltage as its peak rating. In this case, 150 V rated Schottky rectifiers provide the best option as they offer low V_f and no reverse recovery phenomenon. The current rating of these devices has to exceed I_{out} by sufficient margin given the resonant nature of the topology. A 5 or 10 A rated device would be well suited for this application.

Step 16: HBR output capacitor selection

The output capacitor in the HBR circuit experiences significant peak and ripple currents (roughly an order of magnitude higher than an equivalent forward converter) as it has to filter the resonant current in the transformer without the benefit of an intervening inductor. As a result, it is important to choose a very low ESR and high ripple current rated capacitor with appropriate voltage rating. Even though the actual voltage ripple on the capacitor is not of much consequence, the high ripple current can lead to losses, self heating and reduced life if the capacitor choice is not appropriate.

Step 17: Feedback loop design for CV

The feedback loop of the LED power supply is based on voltage feedback only. This can be implemented easily with simple components which include feedback divider resistors, TL431 and RC-compensation network. The compensated signal (error signal) is typically transferred to the primary side using an optocoupler.

Step 18: Merging of secondary-side control signal with PFC feedback signal

The unique control methodology of the NCL30051 allows the control of the output voltage by feeding the error signal into the PFC loop so that the bulk voltage is adjusted accordingly. On the primary side, this error signal is fed to the Pcontrol pin of NCL30051 through a reverse ORing diode. The Pcontrol pin also has a default error signal generated by the PFC error amplifier. The lower of these two signals dominates and helps set the fixed ON time for the PFC block as described in earlier sections. In the intended implementation, the NCL30051's PFC error amplifier should be configured to set the maximum value of the output

voltage and the secondary side feedback should be allowed to control it lower based on the output conditions.

Application of the above steps in a systematic manner will enable a designer to easily come up with a design for a front-end power supply for a type-2 LED driver using the NCL30051. The high level of integration and novelty of topology make it one of the most compact and efficient solutions for this application. However, the success and optimization of the design still depend on the application specific trade-offs made for a particular design. In that sense, the above steps only provide a guideline or framework for the design.

The trade-offs and design choices take a more definitive role when it comes to using the NCL30051 in a type-1 LED driver application.

Design Procedure for Type-1 LED Driver using NCL30051

The type-1 LED driver poses two additional challenges to be addressed by the NCL30051 design approach:

1. The output voltage variations caused by LED forward voltage variation are not buffered by the second stage DC-DC converter and are seen directly by the AC-DC LED driver. As a result, a wider voltage range has to be accommodated and the V_o -ratio becomes higher.
2. The output control is not a voltage control as in type-2 front-end, but is a combined constant current/constant voltage (CCCV) control as required by the LED load.

The following design procedure applies to type-1 drivers. [For the sake of simplicity, all the steps from type-2 approach are repeated and commonality between the two approaches is identified].

Step 1: Identify the load requirements – [Identical to Type-2]

The first step is to understand the load characteristics. This includes:

- Identifying the LEDs to be used
- What current to drive the LEDs
- What type of series-parallel array of LEDs will be employed to get required lumen output

Based on the above information, the load voltage and current characteristics will be more accurately characterized and will be used to develop the driver design.

An example is given below (and used throughout this design procedure to illustrate the design steps).

- LEDs used: OSRAM Golden DRAGON Plus LW W5AM (White LEDs)
- Drive current per LED: 350 mA [Note: these LEDs are capable of being driven at anywhere between 100 mA and 1 A of current, but specified operating point is 350 mA.]

- LED strings: Array of (m=) 3 LED strings in parallel with each string containing (n=) 12 LEDs in series is chosen for this application. The resultant total LED driver output current (I_{out}) is 1.05 A (3×0.35 A).

$$I_{out} = m \times I_{LED} \quad (eq. 15)$$

Step 2: Driver output voltage range [Reduced compared to type-2]

Once the LEDs, their drive current and string arrangement are chosen, the next step is to calculate the output voltage range of the driver. Based on the LED specifications, determine the $[VF_{min}, VF_{nom}$ and $VF_{max}]$ values for the chosen LEDs at the selected drive current. In the present case, these values are [2.7, 3.2 and 3.7] V at 350 mA drive current. Thus, the V_{string} [min, nominal and max] values become $[n \times VF_{min}, n \times VF_{nom}$ and $n \times VF_{max}]$ or [32.4, 38.4 and 44.4] V. The driver max and min voltage are thus, 44.4 V and 32.4 V, respectively. These values are based on the static LED drive current of 350 mA. If analog dimming is used, a wider range of VF values is applicable, thus widening the driver output range. There is a VF reduction of about 10–15% as the LED current is reduced from 350 mA to 50 mA (less than 10:1 range). In addition, there is also a temperature dependence of the VF where the value of VF drops by approximately 0.25 V when the temperature rises from 25°C to 100°C. All these factors require a slight widening of the V_{out} range compared to the calculated values above. In this case, the V_{out} range is changed to (V_{o-min}) 31.4 to (V_{o-max}) 44.4 V. The $V_{o-ratio}$ is calculated to be ($44.4/31.4 = 1.41$).

$$V_{string-max} = n \times VF_{max} \quad (eq. 16)$$

$$V_{string-min} = n \times VF_{min} \quad (eq. 17)$$

$$V_{o-max} = V_{string-max} \quad (eq. 18)$$

$$V_{o-min} = V_{string-min} - V_{margin} \quad (eq. 19)$$

$$V_{o-ratio} = \frac{V_{o-max}}{V_{o-min}} \quad (eq. 20)$$

Step 3: LED driver power rating [Similar to type-2]

The next step is to calculate the power rating of the driver based on the calculated values of V_{o-max} and I_{out} .

$$P_o = I_{out} \times V_{o-max} \quad (eq. 21)$$

In this case, the power rating is $44.4 \times 1.05 = 46.6$ W, which is lower than the one calculated for the type-2 circuit. Taking the power losses and design margin into account, the front-end (Input bridge and PFC circuit) should be designed for slightly higher power – 50–55 W in this case.

Step 4: Input Voltage Range and PFC output voltage (minimum) selection [Identical to type-2]

The next step is to identify the input voltage range and plan the PFC output voltage based on that information. Typically, the LED drivers are designed to operate for one of the following four input voltage conditions:

1. Single (Low) voltage range (85–135 Vac) – This would be applicable to drivers for single geographic markets such as North America and Japan
2. Single (High) voltage range (170–265 Vac) – This would be applicable to Europe, China and other regions which use 220/230 Vac lines.
3. Universal input range (85–265 Vac) – This range is used to standardize designs for application anywhere in the world.
4. Dual voltage range (115 Vac residential and 277 Vac commercial/industrial lighting applications – resultant range for a single driver without range switch is 90–305 Vac factoring in the tolerances). This covers the higher commercial voltage range used in the United States.

The single voltage range (1 or 2 above) makes the driver implementation easier. The low range reduces the voltages required for all stages of the driver and the high range reduces the level of currents being processed. For this case, the single range low mains example will be used (85–135 Vac) to illustrate the design procedure.

The maximum input ac voltage helps determine the minimum value of the PFC output voltage (V_{bulk}) for this application. However, with the NCL30051 application, the V_{bulk} range can be wide based on the output variations, so it makes sense to start with the lowest possible V_{bulk} as the minimum voltage. The minimum possible V_{bulk} is given by:

$$V_{bulk-min} = V_{in-max(rms)} \times \sqrt{2} \quad (eq. 22)$$

Applying this equation to V_{in-max} of 135 Vac results in $V_{bulk-min}$ of 154 Vdc. With some margin added, the chosen value is 160 V.

Step 5: Determine the range of PFC output voltage required [More challenging compared to type-2]

The next step is to check the range of the required PFC output voltage in order to meet the output voltage range requirements. Since the half-bridge resonant converter operates as a fixed voltage ratio converter, the maximum PFC voltage is simply determined by multiplying the minimum voltage and the output voltage ratio.

$$V_{bulk-max} = V_{bulk-min} \times V_{o-ratio} \times 1.10 \quad (eq. 23)$$

The calculated values for $V_{bulk-max}$ is 248 V so for simplicity this will be rounded to 250 V.

The value of $V_{bulk-max}$ determines the stress level of all major components in the PFC section of the circuit. At 250 V (corresponding to V_{in-max} of 135 Vac), the 300 V or higher rated devices (FET and boost diode) are usable with about 16.7% margin. A higher voltage FET may be selected for availability and sourcing flexibility as well. The most common capacitor rating above 250 V that provides adequate derating are 350 V. It should be noted that the above calculations is for LED VF rated currents only. If

analog dimming is used, the range becomes wider and results in even higher value of $V_{\text{bulk-max}}$.

Step 6: Design of bulk capacitor [Similar to type-2]

The bulk capacitor design follows the choice of $V_{\text{bulk-max}}$. Naturally, the voltage rating of the bulk capacitor has to be higher than the sum of $V_{\text{bulk-max}}$ and half the peak-to-peak ripple voltage, which is given by:

$$V_{\text{ripp}(p-p)} = \frac{P_o}{(2 \cdot \pi \cdot f) \times V_{\text{bulk-max}} \times C_{\text{bulk}}} \quad (\text{eq. 24})$$

Normal rule of thumb is to use about 1 μF output capacitance for 1 W of output power. Applying this rule and choosing a 47 μF capacitor for this application, results in a peak-to-peak ripple of 12.4 V for $V_{\text{bulk-max}}$ of 257 V. This ripple is attenuated by the HBR converter and results in a corresponding ripple at the output of the LED driver. The choice of bulk capacitor has to be revisited after the HBR design to ensure the required ripple specification at the output is met. The rms current in the bulk capacitor is provided in [1] and needs to be calculated to ensure the chosen capacitor can handle this current without heating up.

Step 7: Design of PFC Diode [Similar to type-2]

The PFC diode design is not very constrained in this approach since the diode turns off at zero current and does not face significant reverse recovery phenomenon. With the present design, a 300 V or higher ultrafast diode can be chosen with about 15% design margin. The required current rating is given by:

$$I_{d(\text{avg})} = P_o / V_{\text{bulk-min}} \quad (\text{eq. 25})$$

In order to improve the efficiency, low V_f is needed and can be achieved by selecting a slightly higher current rated device (e.g. 3 A device – MURS340 – for the present application).

Step 8: Design of PFC FET [Similar to type-2]

The PFC FET design also follows the standard procedure used in CrM PFC design. Again, the voltage rating for the present example facilitates the choice of a 300 V or higher FET with sufficient derating.

Step 9: Design of PFC Inductor [Similar to type-2]

Design of the PFC inductor follows the design procedure provided in the application literature for CrM PFCs [2]. Note that additional winding is needed on the PFC inductor for Zero Crossing Detection (ZCD). Note that the higher V_{bulk} value results in a marginally higher (about 10%) required inductance value for the same minimum switching frequency.

Step 10: Design of other PFC circuit elements [Similar to type-2]

Like the previous 3 design steps, this step also follows the traditional CrM controller design. Since the PFC section of the NCL30051 is similar to the NCP1608, the choice of components for current sense, feedback, ZCD, On-time control, etc. follow the design procedure in the NCP1608 application note [2]. The design tool for NCP1608 [3] is an

excellent place to start for selecting appropriate component values for this application.

Step 11: Step-down ratio calculation for HBR converter [Different from type-2]

The HBR converter step-down ratio is decided by the following equation:

$$\text{Ratio}_{\text{HBR}} = \frac{V_{\text{bulk-min}} \times \text{Eff}_{\text{conv}}}{V_{o-\text{min}}} \quad (\text{eq. 26})$$

Where Eff_{conv} is the conversion efficiency of the HBR converter, typically >0.95 , which accounts for duty cycle loss in switching transitions and other parasitics. For the present case, the HBR ratio comes out to 4.8 for $V_{\text{bulk-min}}$ of 160 V. The regulation loop ensures that the V_{bulk} is adjusted up or down in order to maintain the V_o or I_o in case either the actual ratio or the assumed conversion efficiency is non-optimal.

The output ripple at V_o is equivalent to the bulk voltage ripple (given by equation 10) divided by the HBR ratio. In LED applications, this ripple may not be that critical.

Step 12: HBR transformer design [Similar to type-2]

The transformer design for the half-bridge resonant converter follows based on the step-down ratio calculated in the previous step. The transformer turns ratio is derived by dividing the HBR ratio by two (since the half-bridge converter steps down half the input voltage every half-cycle). Thus, the calculated transformer turns ratio in this example is 2.4. The actual transformer design is usually an iterative process, where the required number of primary and secondary turns is selected for a specific core to prevent core saturation. After that, the required wire size based on the current levels is determined and the fit of these wires into the available winding window is confirmed.

For the HBR transformer, the magnetizing inductance (L_m) and the leakage inductance (L_{lk}) are critical parameters that play a significant role in circuit operation (achieving resonance and zero voltage switching). However, the convenient approach is to take whatever leakage inductance that can be achieved through normal winding techniques and design the rest of the resonant tank (viz. resonant capacitors) to achieve the desired performance. For reducing magnetizing inductance, there is an option to gap the core that can be exercised. This approach keeps the transformer complexity low and works very well in the NCL30051 application, since there is no frequency modulation of the HBR stage.

Step 13: HBR Resonant Circuit operation [Similar to type-2]

The LLC resonant converter operating at the resonant frequency provides the significant benefits of lowest EMI and highest efficiency [4]. In order to operate in this mode, the switching frequency has to be fixed to match the resonant frequency of the series resonant tank. This frequency is given by:

$$f_s = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{lk} \cdot C_r}} \quad (\text{eq. 27})$$

This equation assumes that the leakage inductance value is sufficient not to require an external resonant inductor.

The resonant tank has to operate at a frequency that is set by the NCL30051 clock to achieve true resonant operation. The specified clock frequency range of the NCL30051 is from about 30 kHz to 150 kHz (corresponding half-bridge clock frequency range is 15 kHz to 75 kHz) and is settable using a single capacitor. As an example, a half-bridge frequency of 35 kHz is chosen. This represents a good compromise between requiring resonant elements (L or C) which are too large (when frequency is too low) and possibly high switching and core losses (when frequency is too high).

The value of C_r can be calculated from the above equation, once f_{sw} and L_{lk} are known. In this example, with a L_{lk} of 100 μH , the calculated value of C_r is 0.2 μF , which is an acceptable practical value.

Step 14: HBR FET selection [Similar to type–2]

The FET selection for the HBR stage is straightforward. The voltage rating of the FETs equals $V_{\text{bulk-max}}$ and adequate derating can be achieved by choosing commonly available 300 V or higher FETs. The R_{ds} /current rating of these FETs is the next consideration. In the HBR topology, there are no turn-on switching losses, so the output capacitance of the FETs (C_{oss}) does not hinder the FET choice – so in this respect, low R_{ds-on} devices are preferred. However, the topology does require fast turn-off to limit turn-off losses. The FET should be chosen while keeping in mind the drive capability of the NCL30051 half-bridge driver (which is 100 mA peak).

Step 15: HBR rectifier selection [Similar to type–2]

The output rectifiers in the HBR topology operate in a center-tapped half-wave rectification mode and with no output inductor; each device sees twice the output voltage as its peak rating. In this case, 150 V rated Schottky rectifiers provide the best option as they offer low V_f and no reverse recovery phenomenon. If the V_{o-max} is contained further through a different choice of LEDs, there is a possibility to even go to 100 V rating for the rectifier in type–1 designs. The current rating of these devices has to exceed I_{out} by sufficient margin given the resonant nature of the topology. A 5 or 10 A rated device would be well suited for this application.

Step 16: HBR output capacitor selection [Similar to type–2]

The output capacitor in the HBR circuit experiences significant peak and ripple currents (roughly an order of magnitude higher than an equivalent forward converter) as it has to filter the resonant current in the transformer without the benefit of an intervening inductor. As a result, it is important to choose a very low ESR and high ripple current rated capacitor with appropriate voltage rating. Even though the actual voltage ripple on the capacitor is not of much consequence, the high ripple current can lead to losses, self

heating and reduced life if the capacitor choice is not appropriate.

Step 17: Feedback loop design for CCCV [More complex compared to type–2]

The feedback circuit for the LED control consists of two parallel loops (implemented using operational amplifiers or dedicated ICs on the secondary). One loop is the current control loop which regulates the LED current to a specified value. This is the dominant loop under normal circumstances as the LED is a current controlled load. However, the additional voltage loop helps contain the output voltage in conditions where there is a LED open fault or where PWM dimming is applied. The two parallel loops are configured so that the lower of the two outputs takes over and hence there is a smooth transition between CC and CV operation. The compensated signal (error signal) is typically transferred to the primary side using an optocoupler.

Step 18: Merging of secondary-side control signal with PFC feedback signal [Similar to type–2]

The unique control methodology of the NCL30051 allows the control of the output voltage/current by feeding the error signal into the PFC loop so that the bulk voltage is adjusted accordingly. On the primary side, this error signal is fed to the Pcontrol pin of NCL30051 through a reverse ORing diode. The Pcontrol pin also has a default error signal generated by the PFC error amplifier. The lower of these two signals dominates and helps set the fixed ON time for the PFC block as described in earlier sections. In the intended implementation, the NCL30051's PFC error amplifier should be configured to set the maximum value of the output voltage and the secondary side feedback should be allowed to control it lower based on the output conditions.

Step 19: PWM dimming [New for type–1 only]

In the situation where PWM dimming is to be applied, additional circuit required. Typically, the PWM dimming signal is provided externally to the secondary side CCCV control block. The PWM signal is buffered and is used to turn on and off the half bridge on the primary side. In case of PWM dimming, the current sensing circuit requires additional averaging circuit (sample and hold) to avoid feeding the wrong feedback signal to the primary. This circuitry is described in the demo board manual.

One additional consideration for PWM dimming is the status of the HBR converter during the PWM off time. Since the HBR converter is designed as a fixed ratio converter with no frequency modulation, during the PWM off time, it continues to circulate significant energy in the resonant tank and hence, carry significant no load losses that impact the average efficiency. NCL30051 addresses this issue by offering a means to shut down the resonant controller during the PWM off time. The (inverted) PWM signal is applied to the OSC pin of the NCL30051 through an opto-isolator and a polarity inverter to shut the oscillator down during PWM off time. As long as the PWM off time is not too long,

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the LLC resonance restarts right away when PWM signal enters the on mode. This mode allows low circulating losses and helps improve the efficiency.

Summary

The preceding sections have provided detailed step-by-step design procedures for using the NCL30051 in ac-input LED driver applications. The two major architectures (type-1 and type-2) are both covered in required detail. The type-2 architecture is relatively simpler, and hence is covered first. However, the type-1 is a more integrated and attractive approach. As shown in the design procedure and examples, the NCL30051 provides a very compact, viable solution in majority of the cases of type-1 applications. The architecture of the NCL30051 does have

some constraints for type-1 approach under extreme conditions as highlighted in the design procedure. Understanding these constraints and applying the right design trade-offs can lead to the optimum LED driver design using the NCL30051 – resulting in high power factor, high reliability, high efficiency, low THD and low cost.

References

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