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650 V SUPERFET®-III MOSFET-based Power Module Applications for XEV OBC System Design

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APPLICATION NOTE

AND90084/D

SUMMARY

The on−board charger (OBC) market is growing rapidly as the demand for battery powered electric vehicles is increasing worldwide. An OBC system is composed of AC−DC converter with power factor correction (PFC) cascaded with a DC−DC converter to control power delivery to the battery. Typically, a two−phase interleaved PFC is coupled with an LLC DC−DC for the 3.3 kW charger. ON Semiconductor has developed a series of power modules with excellent electrical and thermal performance to enable high efficiency chargers with high power density. In this Application Note, we introduce 650 V SF3 SJ MOSFET−based power module family specialized for OBC system design and the basic information on OBC design and analysis using ON Semiconductor's power modules, FAM65CR51XXZ1/2 PFC module and FAM65HRXXDS1/2 H−Bridge module. Also, we demonstrate the performance of these modules through the dedicated system level OBC circuit simulation.

INTRODUCTION TO ON SEMICONDUCTOR 650 V POWER MODULE

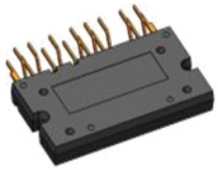
Figure 1 shows the shape of ON Semiconductor's 650 V/51 mΩ SF3 Si MOSFET−based power module. The module has two design variation, PFC module and DC/DC converter module. PFC module is composed of two MOSFETs and two diodes to form a two−phase interleaved boost converter as shown in Figure 2. Customers can choose between 600 V, 15 A Si stealth diode version, FAM65CR51DZ1/2 (Y−form/L−form) and 650 V 30 A SiC diode version, FAM65CR51ADZ1/2. DC/DC converter module (FAM65HR51/82DS1/2) has two−phase, four MOSFET H−Bridge circuit as seen in Figure 2. Customers can select either 51 mΩ MOSFET−based module, FAM65HR51DS1/2 or 82 mΩ MOSFET−based module, NXV65HR82DS1/2. The guideline for choosing optimal module design is provided in chapter Introduction to ON Semiconductor 650 V Power Module and chapter Performance Evaluation of PFC Module and H−bridge Module Using System Level Simulation. ♣ Also, the bridge rectifier module for AC input circuit block and the secondary side of DC/DC converter block is available per request. Single combination of PFC module and DC/DC converter module (Al2O3 DBC substrate) can take 3.6 kW of output power and single H−bridge module with AlN DBC substrate works up to 7 kW. Table 2 introduces the family of 650 V power modules.

PFC Function Module Introduction

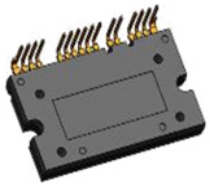
PFC Converter Operation

Figure 2 represents the block diagram of a conventional high voltage OBC system. The PFC block is composed of AC power source (85 − 265 Vac), input filter, bridge rectifier and two−phase interleaved boost converter.

(a) Bottom View



(b) Top View (Y−Form)



(c) Top View (L−Form)

Figure 1. 650 V Power Module for OBC and DC/DC Converter Application

The PFC block generates AC input current that is in phase with the AC input voltage to maximize the power factor (PF) and minimize the grid harmonic distortion. With typical control, the PFC stage can hold 0.97 < PF < 1.0.

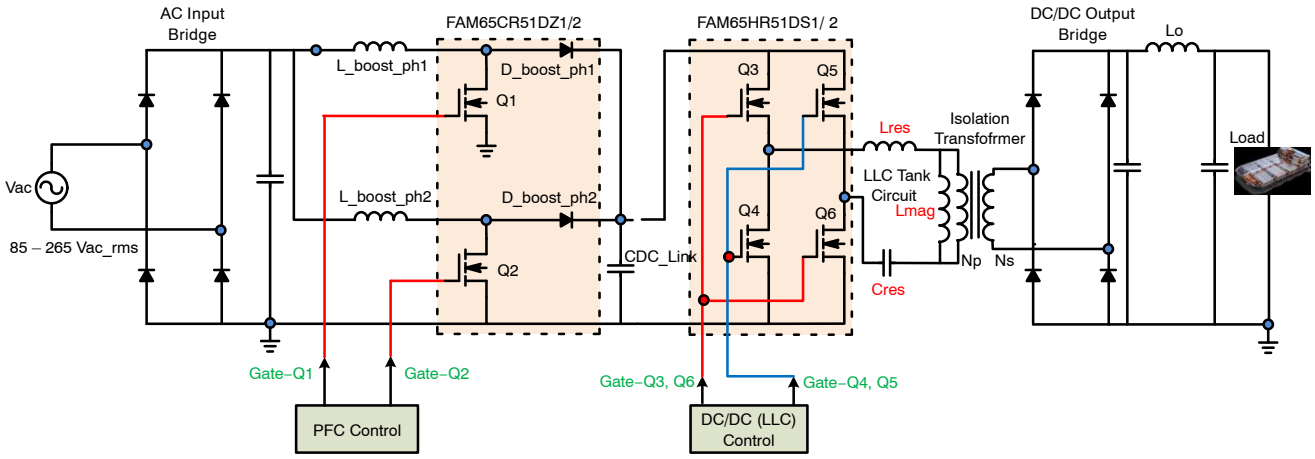


Figure 2. Block Diagram of Conventional OBC System Including Two−phase Interleaved PFC and LLC Converter

The PFC circuit can be designed to operate in continuous current mode (CCM) or critical current mode (CRM) based on the nature of the inductor current waveform in a boost converter circuit. In high power application such as the OBC for EVs, the CCM topology is commonly used to minimize the current ripple and maximize the system efficiency. In the CCM PFC, the switch (MOSFET) in the boost converter has a fixed switching frequency with variable duty cycle (on−time), whereas the CRM PFC has variable switching frequency with fixed on−time. This characteristic of CRM makes the design of the PFC components more complicated, requiring a dedicated input EMI filter circuit due to the high current ripple. Although the CRM PFC has an advantage in reduced switching losses owing to its zero current switching, this advantage is canceled by higher conduction losses than that of the CCM PFC. Since the CCM PFC has a fixed switching frequency, power factor is higher than CRM PFC, typically by 0.2% to 0.3% and this leads to higher PFC efficiency. Figure 3 shows the phase matching between input voltage and current (PF ≈ 98%), and waveform of the inductor current in the boost converter operating in CCM PFC mode. By contrast, Figure 4 shows the inductor current in CRM PFC where the current changes the slope at its zero−crossing point. In this application note, CCM operation was applied using ON Semiconductor's FAM65CR51 family. Figure 5 represents the circuit diagram of two phase interleaved boost converter circuit and Figure 9 shows the internal circuit diagram of FAM65CR51(A)DZ1/2* module that is ideal to implement a two−phase interleaved boost PFC converter. Figure 6 illustrates the effect of interleaving in CCM PFC circuit. In a two phase interleaved boost converter, the two inductor currents are out of phase by 180° and the ripple in each inductor current is cancelled partially at the summing node.

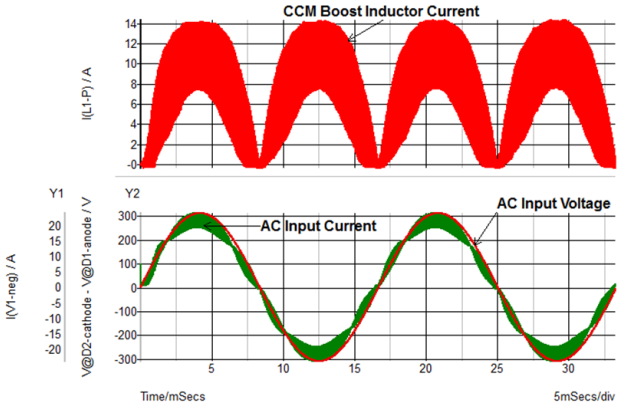


Figure 3. Phase Matching between Input Voltage and Current in a CCM PFC

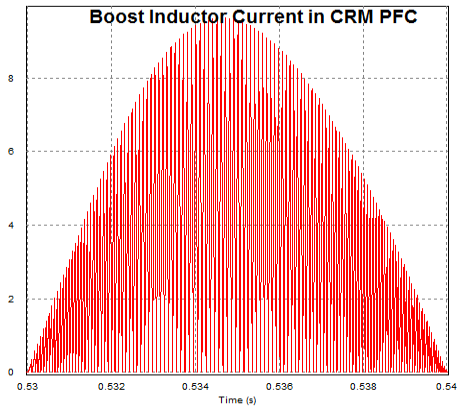


Figure 4. Boost inductor current in CRM PFC

*: A is for designation of 650 V 30 A SiC diode version

In CCM PFC, duty cycle is continuously changing and maximum ripple reduction occurs when the duty cycle, D is 0.5 as seen in Figure 7. Equation 1 below represents the current ripple reduction ratio *K* in a two−phase interleaved boost converter.

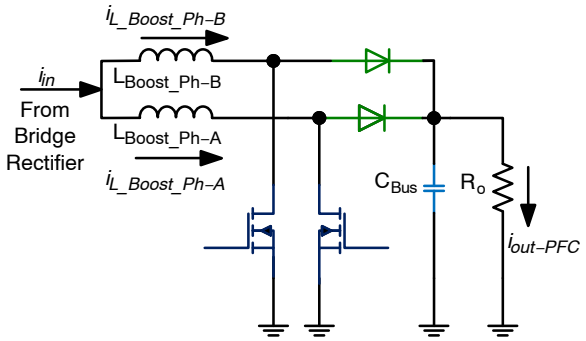


Figure 5. Interleaving of Two−phase Current

$$K(D) = \frac{\Delta I_{interleaved}}{\Delta I_{L\_boost}} = \frac{1 - 2 \times D}{1 - D},\ D < 0.5$$

$$= \frac{1 \times 2 - D}{D},\ D \geq 0.5 \qquad \text{(eq. 1)}$$

where

$\Delta_{IL-boost}$: Amplitude of the phase current ripple

$\Delta_{Iinterlived}$: Amplitude of interleaved current ripple

Also, interleaving can reduce the total boost inductor energy consumption. In a single phase boost converter,

$$E_{L\_boost} = \frac{1}{2}Li^2 \qquad \text{(eq. 2)}$$

In a two phase interleaved Boost converter, total inductor energy,

$$E_{L\_interleaved} = 2 \times \left[\frac{1}{2} \times L\left(\frac{i}{2}\right)^2\right] = \frac{1}{4}Li^2 \qquad \text{(eq. 3)}$$

Therefore, interleaving brings reduction in the size of the inductor and consequently reduced current ripple in output capacitor.

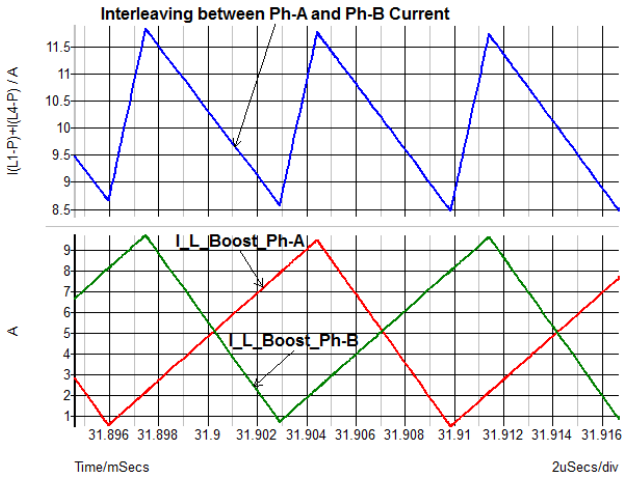


Figure 6. Current Ripple Reduction in Two−phase Interleaved Boost PFC Circuit

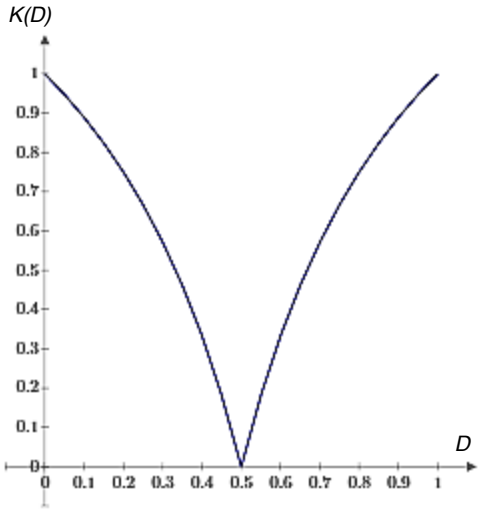


Figure 7. Ripple Reduction in PFC Boost Inductor Current by Interleaving (Ripple is Minimized at D = 0.5)

Design Specification on PFC Function Block

Table 1 below shows the design specification of 3.3 kW and 6.6 kW PFC circuit block and Figure 8 illustrates the PFC circuit block diagram including AC power grid, input rectifier bridge and control circuit used in the PFC system simulation. Pre−charging circuit was not considered in the simulation.

Table 1. TYPICAL DESIGN SPECIFICATION OF PFC BLOCK

AC Input Voltage	85 – 265 V_{rms}, 50 – 60 Hz
PFC Output Voltage	390 – 400 V_{DC}
Rated Output Power	3.3 kW~11 kW
Inductor Current Ripple	<25% @ Rated Power
Output Voltage Ripple	2% of Output at 120 Hz
Switching Frequency	50 kHz~250 kHz

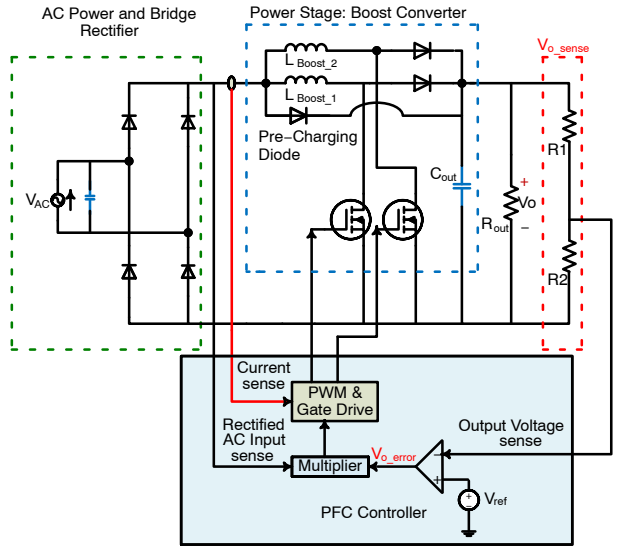


Figure 8. Closed−loop PFC Function Block

Major Components in PFC Function Block

PFC Boost Inductor

The inductance of the boost inductor can be determined by the amount of current ripple and the switching frequency as below:

$$L_{boost} = \frac{1}{\%ripple} \times \frac{v_{ac\_min}^{2}}{P_{out}} \left(1 - \frac{\sqrt{2} \times v_{ac\_min}}{V_{out}}\right) \times \frac{1}{f_{fw}} \quad \text{(eq. 4)}$$

By putting the design specifications (Table 1) into the Equation 4 above,

$$L_{boost} = \frac{1}{0.25} \times \frac{(85\ v_{rms})^2}{3300\ W} \times \left(1 - \frac{\sqrt{2} \times 85\ v_{rms}}{400\ V}\right) \times$$

$$\times \frac{1}{65 \times 10^3\ Hz} = 130.3\ \mu H$$

Considering the design margin, 150 μH inductor would be enough for 3.3 kW PFC.

Output Capacitor

The value of Output capacitor is determined by PFC output voltage, the rated power of PFC and capacitor hold−up time. Suppose PFC output voltage should not fall below 300 V during single AC line cycle period (1/60 Hz = 16.7 ms), the hold−up time, $t_{\_hold}$ = 16.7 ms and V_{out_min} = 300 V. Assuming Vout = 400 V, output capacitor size can be determined as below [1]:

$$C_{out} \geq \frac{2 \times P_{out\_max} \times t_{hold}}{V_{out}^{2} - V_{out\_min}^{2}} = 1.575\ mF$$

Typically, 1.8 mF~2.0 mF capacitor is used for 3.3 kW OBC system.

Input Rectifier Diode

The bridge rectifier must be able to handle the AC input current peak defined below:

$$i_{in\_ac\_max} = \sqrt{2} \times \frac{P_{out\_max}}{\eta \times v_{ac\_min} \times PF} =$$

$$= \sqrt{2} \times \frac{3300\ W}{0.98 \times 85\ v_{rms} \times 0.98} = 40.4\ A$$

where

η = Target PFC efficiency

ON Semiconductor has 1000 V, 80 A ultrafast diode, RURG80100 for the AC input rectifier application.

FAM65CR51 PFC Module Family

FAM65CR51 family was developed specially for two−phase interleaved PFC boost converter operation or two−phase bridgeless PFC operation and the module is composed of a pair of MOSFET and series−connected diode branch to form a two−phase boost converter circuit as shown in the Figure 9 below.

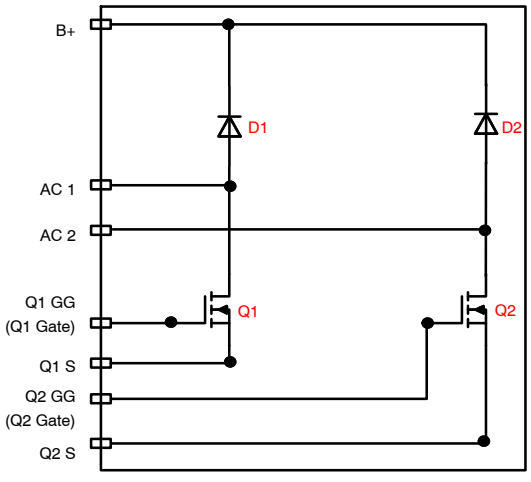


Figure 9. Internal Circuit Diagram of FAM65CR51DZ1 PFC Module

In the module, ON Semiconductor's 3rd generation (SF3) Super Junction MOSFET die is used for the main boost converter switch. Table 2 below shows the electrical characteristics of the MOSFET die in FAM65CR51DZ1/2 module. Since PFC Boost converter experiences hard switching, the MOSFET parameters should be optimized to have low switching loss along with low thermal impedance. As seen from Table 2, 650 V SF3 SJ MOSFET die has: 1) low Qg that enables the fast turn−on/turn−off, 2) small Coss resulting in low switching loss and 3) low thermal resistance comparing to the major competitors' parts. Table 3 shows the boost converter diode characteristics. As the base line−up, 600 V 15 A stealth diode is applied in the module and currently, 650 V 30 A SiC diode version, FAM65CR51ADZ1/2 is also available to enhance the converter efficiency. In PFC boost converter, the reverse recovery current from the high side diode is directly added to the drain current of the low side MOSFET during the turn−on transient and this causes the increased turn−on switching loss in the low side MOSFET. Since SiC diode has nearly zero reverse recovery current, applying SiC diode brings the reduced MOSFET switching loss, increased system efficiency and reduced EMI. Figure 10 shows the reverse recovery characteristics of 600 V 15 A stealth diode (ISL9R1560−F085) and 650 V 30 A SiC diode (FFSP3065−F085) in a 5.5 kW PFC boost converter. As seen from Figure 26, by applying SiC diode, PFC efficiency increases owing to the reduced power loss from both the diode and MOSFET. The standard module with Al_2O_3 DBC substrate has the thermal resistance of 0.66°C/W. For higher thermal performance, the module with AlN DBC substrate, FAM65CR51AXZ1/2 is available. FAM65CR51AXZ1/2 module has less than 1/3 thermal resistance of Al_2O_3 DBC version and by using this AlN DBC module, customers can reduce the design complexity and also save the cost and space in a 6 kW PFC converter design. Table 4 shows all the electrical and thermal features of FAM65CR51 PFC module family.

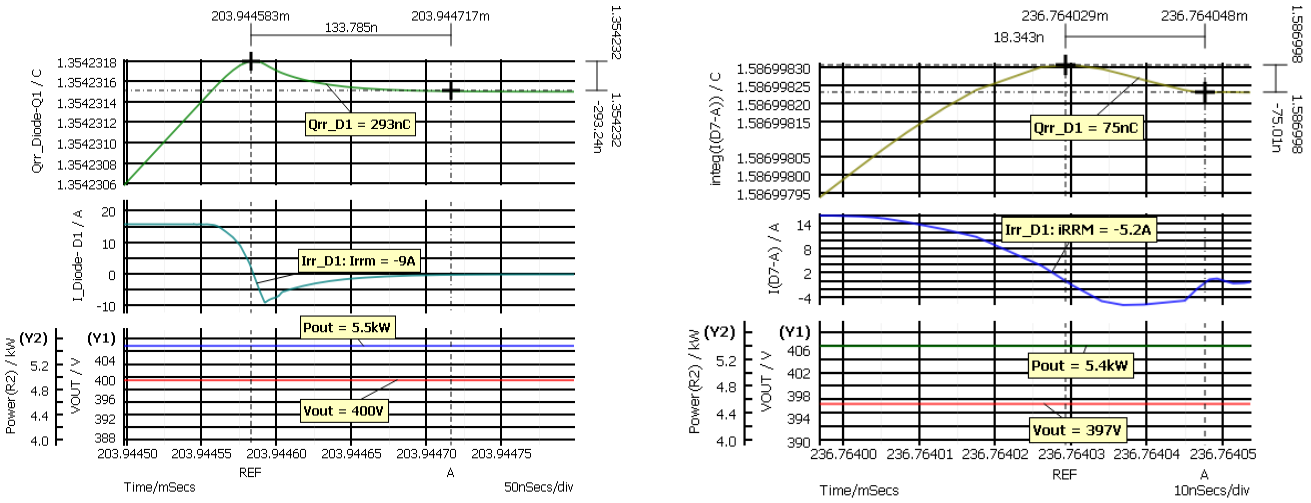


Figure 10. Reverse Recovery in ISL9R1560−F085 Stealth Diode and FFSP3065−F085 SiC Diode

Table 2. ELECTRICAL CHARACTERISTICS OF MOSFET DIE IN PFC MODULE AND DC/DC CONVERTER MODULE

Symbol	Parameter	Typical Value		Units
		51 mΩ Die	82 mΩ Die*	
V_{GS} (Q1−Q2)	Gate to Source Voltage	±20 Max		V
I_D (Q1−Q2)	Drain Current Continuous (T_C = 25°C, V_{GS} = 10 V)	33 Max	23.5 Max	A
	Drain Current Continuous (T_C = 100°C, V_{GS} = 10 V)	21 Max	14.8 Max	A
BVDSS (Q1−Q2)	Drain to Source Breakdown Voltage	650 Min	650 Min	V
Coss	Output Capacitance (V_{DS} = 400 V, V_{GS} = 0 V and fsw = 1 MHz)	109	72.3	pF
Qg	Total Gate Charge	123	79.7	nC
$R_{DS(ON)}$	ON−Resistance of the MOSFET Die	44	73	mΩ
$R_{\theta JC}$	Junction to Case Thermal Resistance (Note 1)	0.66	0.93	°C/W
$R_{\theta JS}$	Junction to Heatsink Thermal Resistance (Note 2)	1.2	1.47	°C/W
T_J	Maximum Junction Temperature	−55 to 150		°C
T_C	Maximum Case Temperature	−40 to 125		°C
T_{STG}	Storage Temperature	−40 to 125		°C

1. $R_{\theta JC}$: Test method compliant with MIL STD 883−1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and discoloration on the DBC surface allowed.
2. $R_{\theta JS}$: Defined by thermal simulation assuming the module is mounted on a 5 mm Al−360 die casting material with 30 μm of 1.8 W/mK thermal interface material.

Table 3. BOOST CONVERTER DIODE CHARACTERISTICS

Symbol	Parameter	Typical Value		Units
		600 V 15 A Si Diode	650 V 30 A SiC Diode	
V_{RRM}	Peak Repetitive Reverse Voltage	600 Min	650 Min	V
V_{RWM}	Working Peak Reverse Voltage	600 Min	650 Min	V
V_R	DC Blocking Voltage	600 Min	650 Min	V
$I_{F(AV)}$	Average Rectified Forward Current Tc = 25°C	15	30	A
I_{FSM}	Non−Repetitive Forward Surge Current (Half Wave 1 Phase 60 Hz)	45	110	A
I_{RR}	Reverse Recovery Current (I_F = 15 A, dI_F/dt = 200 A/μs, VR = 390 V)	5.0	–	A
T_J	Maximum Junction Temperature	−55 to 175	−55 to 175	°C
T_{STG}	Storage Temperature	−40 to 125	−40 to 125	°C
E_{AVL}	Avalanche Energy (1 A, 40 mH)	20	144	mJ
Q_{RR}	Reverse Recovery Charge (I_F = 15 A, dI_F/dt = 800 A/μs, V_R = 390 V)	390	–	nC
T_{RR}	Reverse Recovery Time (I_F = 15 A, dI_F/dt = 800 A/μs, V_R = 390 V)	52	–	nsec
S	Softness Factor t_b/t_a (I_F = 15 A, dI_F/dt = 800 A/μs, V_R = 390 V)	1.36	–	–
R_{θ_JC}	Junction to Case Thermal Resistance (Note 3)	1.98	1.4	°C/W
R_{θ_JS}	Junction to Heatsink Thermal Resistance (Note 4)	2.97	3.03	°C/W

3. $R_{\theta JC}$: Test method compliant with MIL STD 883−1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and discoloration on the DBC surface allowed.
4. $R_{\theta JS}$: Defined by thermal simulation assuming the module is mounted on a 5 mm Al−360 die casting material with 30 μm of 1.8 W/mK thermal interface material.

Table 4. FAM65CR51 PFC MODULE FAMILY AND FAM65HR51 H−BRIDGE MODULE FAMILY

Function	Part Name	Distinguishing Technical Feature	Rth_jc [°C/W] Typ	
			MOSFET	Diode
Two−Phase Interleaved PFC Module	FAM65CR51DZ1/2	51 mΩ Die, Al_2O_3 DBC 15 A Stealth Diode	0.66	1.98
	FAM65CR51XZ1/2	51 mΩ Die, ALN DBC 15 A Stealth Diode	0.19	0.74
	FAM65CR51ADZ1/2	51 mΩ Die, Al_2O_3 DBC 30 A SiC Diode	0.54	1.4
	FAM65CR51AXZ1/2	51 mΩ Die, AlN DBC 30 A SiC Diode	0.19	0.72
H−Bridge Module	FAM65HR51DS1/2	51 mΩ Die, Al_2O_3 DBC Snubber Cap.	0.66	–
	FAM65HR51XS1/2	51 mΩ Die, AlN DBC Snubber Cap.	0.19	–
	NXV65HR51DZ1/2	51 mΩ Die, Al_2O_3 DBC, No snubber Cap	0.66	–
	NXV65HR82DS1/2	82 mΩ Die, Snubber Cap.	0.93	–
	NXV65HR82DZ1/2	82 mΩ Die, No Cap.	0.93	–

FAM65HR51DS1 DC/DC Converter Module

Introduction

FAM65HR51DS1/2 and NXV65HR82DS1/2 H−Bridge modules were developed for various DC/DC converter applications including LLC converter and conventional (Phase−shifted) full bridge converter. FAM65HR51DS1/2 module has four 650 V 51 mΩ SF3 MOSFET dies to form a two−phase full bridge circuit and NXV65HR82DS1/2 module is built with four of 650 V 82 mΩ SF3 MOSFET dies. ON Semiconductor's 650 V SF3 Super Junction MOSFET family has fast switching speed and fast reverse recovery of the body diode to optimize the switching behavior. The features of the modules will be explained in detail in chapter FAM65HRXXDS1/2 H−Bridge Module.

DC/DC (LLC) Converter Operation

Figure 11 represents a DC/DC converter block in a vehicle OBC system. PFC output voltage is fed into DC/DC converter input. This input waveform is not a pure DC signal and includes 120 Hz AC ripple from PFC block. DC/DC converter switches on and off the input voltage waveform and generates the square pulse waveform controlled by PWM control. Typically, DC/DC converter forms a Half bridge or Full bridge circuit and LLC resonant topology or Phase−shifted full bridge topology is applied to minimize the switching loss by zero voltage switching (ZVS). LLC tank circuit follows the DC switching block. LLC is named since the resonant tank circuit is composed of resonant inductor, resonant capacitor and magnetizing inductance of the isolation transformer. The square waveform from DC switching block changes to "almost−sinusoidal" signal through LLC tank circuit and transferred to the isolation transformer. The transformer isolates the primary switching block from secondary load side to protect the propagation of conductive EMI noise and short circuit from the load side.

In most cases, the turn ratio of the transformer, N_{sec}/N_{pri} is higher than unity to operate in wide range of output (battery) voltage. In the secondary side, transformer output signal is rectified by the bridge rectifier circuit and finally becomes the DC signal to charge the HV battery.

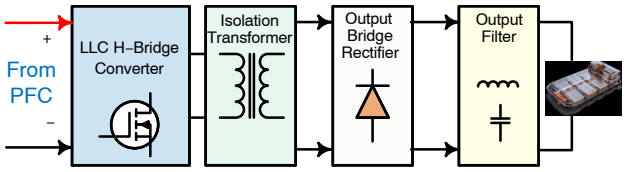


Figure 11. OBC DC/DC Converter Block Diagram

Figure 12 shows the full−bridge LLC converter circuit with current mode control. Input voltage is supplied from PFC block and ranges 390 V~400 V. The output voltage is determined by HV battery voltage, 250 V~450 V. In an LLC DC/DC converter stage, MOSFET power loss is one of the major factor that determines OBC system efficiency and reduction of the turn−off switching loss and conduction loss of the MOSFET is critical in a converter design. MOSFET power loss is related to the size of the die. As the size of the die increases, MOSFET conduction loss decreases with lower Rds_on value and at the same time, the switching loss increases due to the increased loop parasitic inductance and resistance. In a 3.6 kW or lower power OBC system, using smaller die (60 mΩ~82 mΩ) can bring reduced switching loss accommodating some increase in conduction loss. But as the power level of OBC increases above 3.6 kW, the conduction loss becomes dominant and the smaller die size inevitably brings higher total power loss and higher junction temperature due to the higher thermal resistance. For those reasons, applying larger MOSFET die in LLC topology is

justified in a high power OBC system owing to the lower conduction loss and ZVS effect during the turn−on switching transient. Currently, LLC converter topology would be the most viable choice to use the ZVS characteristics. In a conventional full−bridge converter, the two MOSFETs in diagonal direction forms a switching pair sharing the same gate drive signal with duty cycle of 50%. Each switching pair has 180° of phase difference. As an alternative, Phase−shifted full bridge topology can be implemented without LC resonant tank circuit enabling natural ZVS through free−wheeling of the body diode and control is also simpler than that of LLC topology. But in HV OBC application, the system efficiency is critical and excessive power loss from body diode free−wheeling operation becomes a big burden to achieve the target efficiency. Therefore, Phase−shifted full bridge topology is in general not used for HV OBC system and mainly used in HV to LV DC/DC converter where efficiency is not the highest priority. In terms of control, either the peak current mode control or average current mode control method is used to set the charging current in accordance with the HV battery charging state (SOC). Here, the DC/DC converter control method will not be discussed further. In this application note, LLC full bridge converter circuit with average current mode control was implemented to evaluate the performance of FAM65HR51DS1/2 H−bridge module including switching behavior, power loss and efficiency.

LLC Resonant Tank Circuit Analysis

Figure 13 shows the simplified LLC resonant converter circuit (a) and equivalent secondary side signal processing block diagram (b). LLC resonant tank circuit is composed of resonant inductor, Lr, resonant capacitor, Cr and the transformer magnetizing inductance, Lmag. As seen from Figure 13 (a), the input voltage of the LLC resonant circuit is a square waveform alternating between the positive and negative value of DC input voltage of the full−bridge converter block. Assuming only the fundamental frequency component of the input voltage is used to transfer energy from the primary side to the secondary side of the isolation transformer, the First Harmonic Approximation (FHA) method [4] can be applied to perform the analysis of an LLC resonant circuit avoiding complex analytical method.

In Figure 13 (b), the primary side was replaced by AC current source model. Since the average value of $|i_{\_ac}(t)|$ is equals to the DC output current, Io, $i_{ac}(t)$ can be represented as the Equation 5.

$$i_{ac}(t) = \frac{\pi \times I_o}{2} \sin(2\pi f_{sw} t) \quad \text{(eq. 5)}$$

Using FHA method, $v_{ac}(t)$ can be approximated by the fundamental component of the square waveform VP (t) as the Equation 6.

$$V_p(t) = V_0 : \text{if } \sin(2\pi f_{sw} t) \geq 0$$
$$V_p(t) = -V_0 : \text{if } \sin(2\pi f_{sw} t) < 0 \quad \text{(eq. 6)}$$

Therefore,

$$v_{ac}(t) = V_{p\_f0}(t) = \frac{4\,V_o}{\pi} \sin(2\pi f_{sw} t) \quad \text{(eq. 7)}$$

where

$V_{p\_f0}(t)$ = Fundamental frequency component of V_p (t)

The ac equivalent resistance, r_{ac}, can be obtained using iac (t) and vac (t).

$$r_{ac} = \frac{v_{ac}(t)}{i_{ac}(t)} \times \frac{8}{\pi^2} \times \frac{V_o}{I_o} = \frac{8}{\pi^2} R_o \quad \text{(eq. 8)}$$

Considering the transformer turns ratio n = Npri / Nsec, the actual AC equivalent road resistance seen from the primary side is given by Equation 9.

$$r_{ac} = \frac{8 \times n^2}{\pi^2} R_o \quad \text{(eq. 9)}$$

Using this AC equivalent resistance in Equation 9, AC equivalent circuit for the entire LLC converter can be obtained as illustrated in Figure 14.

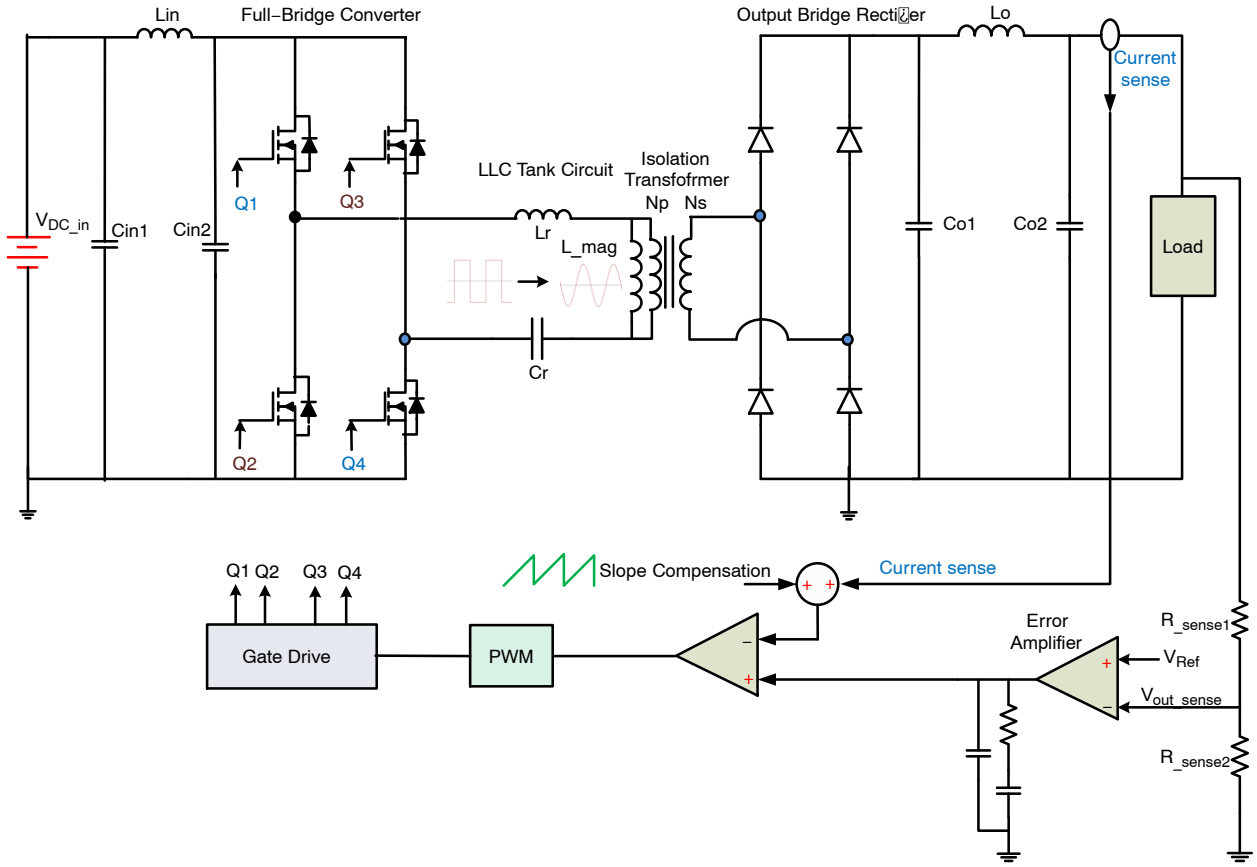


Figure 12. Full−Bridge LLC Converter Circuit with Current Mode Control

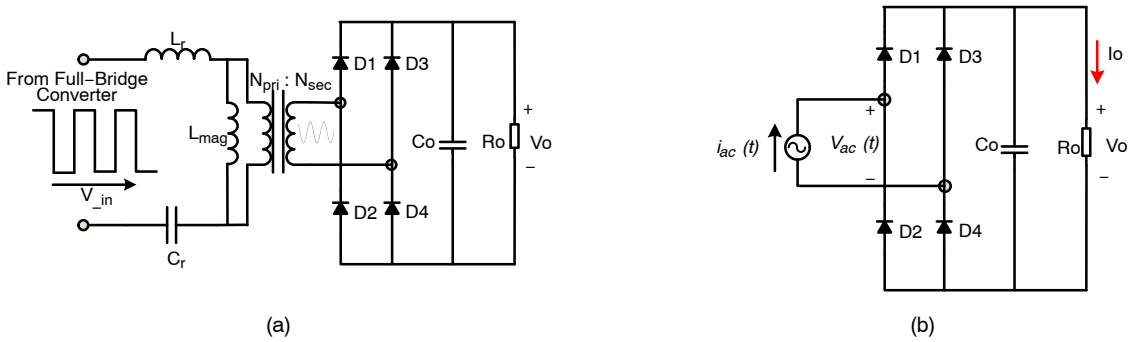


Figure 13. (a) Simplified LLC Circuit and (b) Equivalent Model Replacing Primary Side with AC Current Source

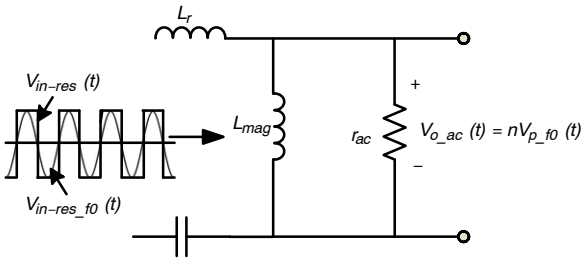


Figure 14. AC Equivalent Circuit for LLC Resonant Converter

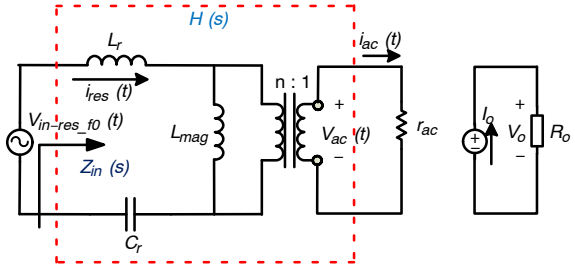


Figure 15. Two Port Network Model of FHA Resonant Circuit

The quality factor, Q of the resonant tank circuit in Figure 13 is defined as the Equation 10.

$$Q = \frac{\sqrt{L_r / C_r}}{r_{ac}} \quad \text{(eq. 10)}$$

where

$$n = \frac{N_{pri}}{N_{sec}}$$

$$r_{ac} = \frac{8}{\pi^2} \times \frac{N_{pri}^2}{N_{sec}^2} \times R_o$$

$$R_o = \frac{V_o}{I_o}$$

The resonant tank gain is the magnitude of the transfer function of the AC equivalent circuit and defined as in Equation 11.

$$M = \frac{v_{o\_ac}(t)}{V_{in-res\_f0}(t)} = \frac{nV_{p\_f0}(t)}{V_{in-res\_f0}(t)} = \frac{\frac{4}{\pi} V_o \times \sin(2\pi f_{sw} t)}{\frac{2}{\pi} V_{in} \times \sin(2\pi f_{sw} t)} =$$

$$= \frac{2\pi \times V_o}{V_{in}} \quad \text{(eq. 11)}$$

Alternatively, LLC resonant tank circuit can be defined by its transfer function *H(s)* and input impedance $Z_{in}(s)$ using two port network model as Figure 15.

$$H(s) = \frac{V_{ac}(s)}{V_{in-res\_f0}(s)} = \frac{1}{n} \times \frac{n^2 \times r_{ac} \parallel sL_{mag}}{Z_{in}(s)} \quad \text{(eq. 12)}$$

where

$$Z_{in}(s) = \frac{V_{in-res\_f0}(s)}{I_{res}(s)} = \frac{1}{sC_r} + sL_r + n^2 r_{ac} \parallel sL_{mag}$$

In Equation 12, the term, $n^2 \cdot r_{ac}$ is the effective resistive load reflected to the primary side of the transformer.

The term “Normalized Voltage Conversion Ratio” or “Voltage Gain” $M(f_{sw})$ is defined as:

$$M(f_{sw}) = n \times \| H(j2\pi f_{sw}) \| = n \times \frac{v_{ac}(t) \mid rms}{V_{in-res\_f0}(t) \mid rms} =$$

$$= n \times \frac{\frac{2\sqrt{2}}{\pi} V_o}{\frac{\sqrt{2}}{\pi} \times V_{in}} = \frac{2n \times V_0}{V_{in}} \quad \text{(eq. 13)}$$

From Equation 13, input to output DC/DC voltage conversion ratio becomes:

$$\frac{V_o}{V_{in}} = \frac{1}{2n} M(f_{sw}) \quad \text{(eq. 14)}$$

After some comprehensive work using the Equations 10, 11, 12, 13 and 14, the voltage gain can be described as a function of the quality factor Q, inductance ratio ($m = L_r / L_{mag}$) and normalized frequency, f1 as shown in Equation 15. ([2], [4])

$$M(Q, m, f_1) = \frac{f_1^2 \times (m-1)}{\sqrt{(m \times f_1^2 - 1) + f_1^2 \times (f_1^2 - 1)^2 \times (m-1)^2 \times Q^2}} \quad \text{(eq. 15)}$$

Table 5 shows an example of the design parameters in an LLC converter. These parameters are applied also in 3.3 kW LLC converter evaluation board and the OBC simulation.

Table 5. DESIGN PARAMETERS FOR UP TO 3.6 kW LLC FULL−BRIDGE CONVERTER

Component	Designation	Value
Converter DC Input Voltage	V_{in_DC}	390 – 400 V
Converter DC Output Voltage	V_{out_DC}	250 – 450 V
Switching Frequency	f_{sw}	100 – 150 kHz
Resonant Frequency	f_{res}	100 kHz
Resonant Inductor	L_r	25 μH
Resonant Capacitor	C_r	100 nF
Magnetizing Inductance	L_{mag}	125 μH
Transformer Turns Ratio	$n = N_{pri} / N_{sec}$	0.8
Inductance Ratio	$m = L_{mag} / L_r$	5
Normalized Frequency	$f1 = f_{sw} / f_{res}$	1 – 1.55

In the designed LLC converter circuit using Table 5, Q varies from 2.217 to 0.267 as the output load varies. Figure 16 shows the LLC converter gain variation with the change in the output load. As the output load gets heavier, the peak gain point shifts closer to to the resonant point and the peak gain gets closer to unity. Figure 17 illustrates the LLC gain characteristics in 3.3 kW loading. In the figure, the power transfer operation is divided into the two regions, ZVS Region 1 and ZVS Region 2. During the power transfer operation (I_Lr > I_Lmag), the magnetizing inductor is being charged and it does not participate in the resonance operation. In this power transfer mode, the resonant frequency, fres is defined as:

$$f_{res\_0} = \frac{1}{2\pi \sqrt{L_r \times C_r}} \quad \text{(eq. 16)}$$

ZVS is accomplished in both the region 1 and region 2. In region 2, the switching frequency is lower than the resonant frequency and the converter gain is higher than unity. Therefore, the converter is operated in boost mode. In region 1, the LLC converter is working in Buck operation mode. The switching frequency is higher than resonant frequency and the LLC gain is lower than the unity.

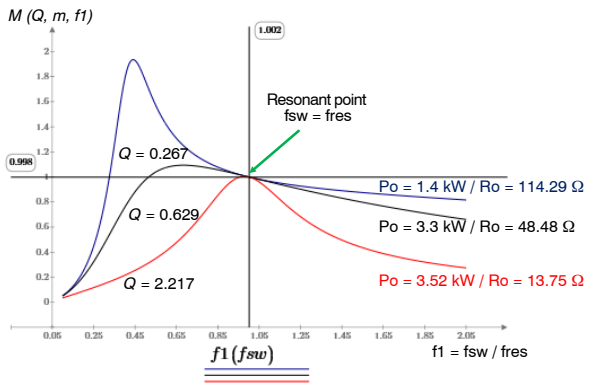


Figure 16. LLC Converter Gain Variation in Accordance with the Load Shift

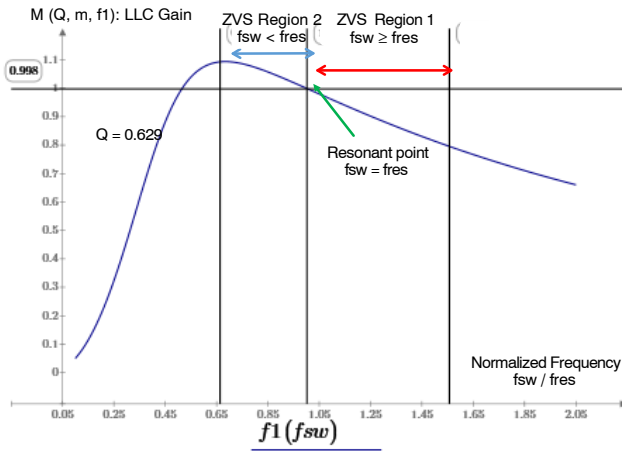


Figure 17. LLC Converter Gain Graph at 3.3 kW Load Condition

The two ZVS operating regions are explained in detail as below.

ZVS Region 1

Figure 18 shows the typical waveforms in LLC converter operating in the ZVS region 1. In this region, the switching frequency f_{sw} is set higher than the resonant frequency, f_{res}, and power is transferred from primary side to the secondary side of the transformer until the end of each switching period. The magnetizing inductor current, I_Lmag is a part of the resonant inductor current, $I_{\_Lr}$ and just charges the magnetizing inductor, Lmag. Therefore, Lmag is not involved in the resonant operation. The primary side transformer current, $I_{\_TXR\_Pri} = I_{\_Lr} - I_{\_Lmag}$ is delivered to the secondary side. At the end of power delivery operation, $I_{\_Lr}$ changes its direction (di/dt becomes negative) and returns back to the body diode of the MOSFET in the other phase leg to achieve ZVS turn−on. Gate drive signal is applied at some point in this period as seen from Figure 19. One thing is that as the switching period $Ts = 1 / f_{sw}$ ends before the resonant current completes its own period, $T_r = 1 / f_{res}$, MOSFET has a hard turn−off switching and the secondary side rectifier diodes experience hard commutation as seen Figure 20. By design optimization of an LLC tank circuit, turn−off transient current of the MOSFET can be minimized resulting in near zero current switching condition (ZCS).

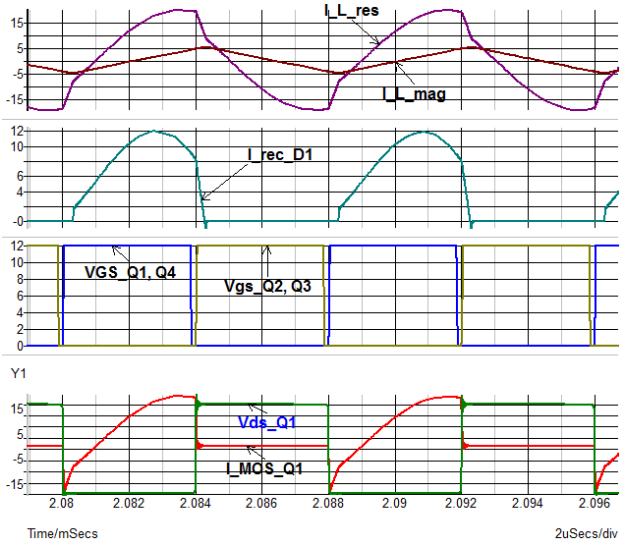


Figure 18. Typical Waveforms in LLC Full−bridge Converter (f_{sw} = 125 kHz, f_{res} = 100 kHz)

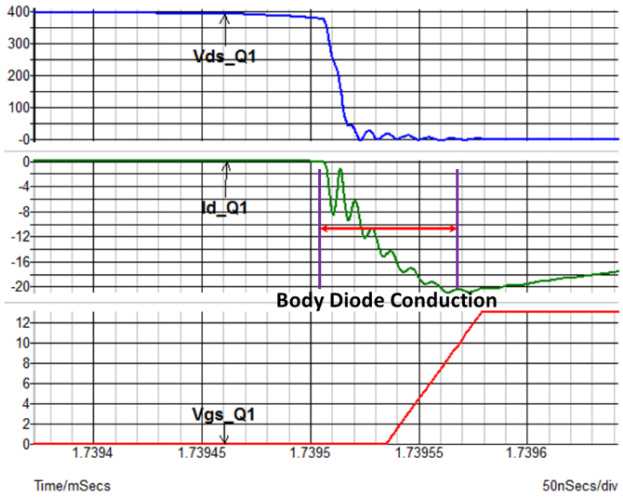


Figure 19. ZVS Operation: Gate Drive Signal is Engaged During the Body Diode Conduction (V_{ds} ≈ 0 V)

ZVS Region 2

Figure 21 shows the LLC converter waveforms in ZVS region 2. In this region, the switching frequency fsw is lower than the resonant frequency, fres and each switching period includes the freewheeling period T_{fw} and in this region, $I_{\_Lmag} \approx I_{\_Lr}$. In this period, resonant operation includes discharging of magnetizing inductor and this resonant current returns back to the converter since the MOSFET channel is still open. During the freewheeling operation, the power in primary side of the transformer is not transferred to the secondary side and generates the additional conduction loss in the MOSFET. In this period, second

resonant frequency, fres_1 is defined as given in Equation 17.

$$f_{res\_1} = \frac{1}{2\pi\sqrt{(L_r + L_{mag}) \times C_r}} \quad \text{(eq. 17)}$$

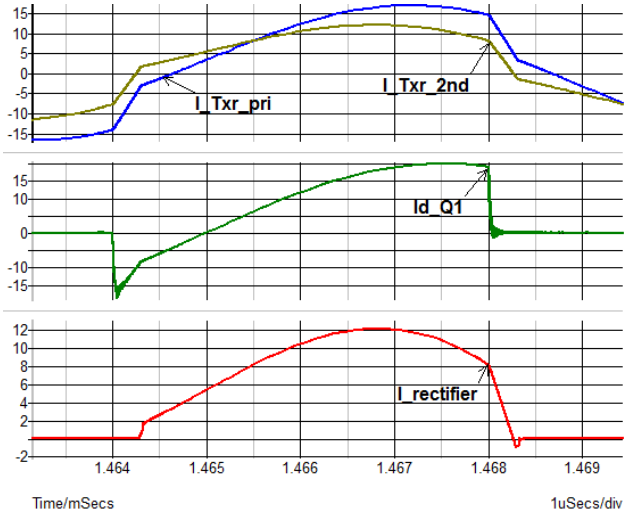


Figure 20. Secondary Side Rectifier Diode Hard Commutation During the MOSFET Turn−off Transient

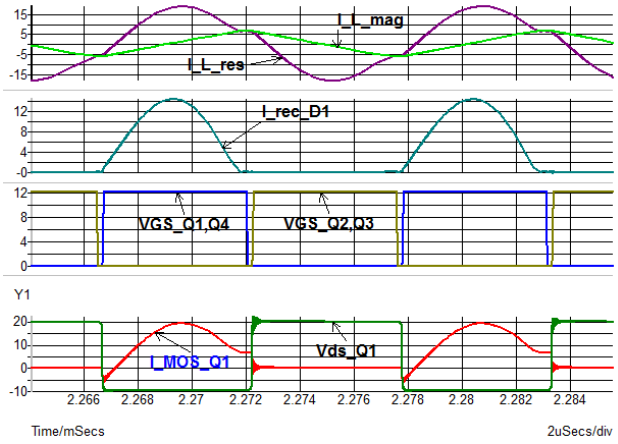


Figure 21. Waveforms in LLC Full−bridge Converter in ZVS Region 2 (f_{sw} = 90 kHz, $f_{resonant}$ = 100 kHz)

FAM65HRXXDS1/2 H−Bridge Module

Figure 22 shows the circuit diagram and pin−out configuration of FAM65HR51DS1 H−bridge module. The module was designed for a two−phase full bridge (LLC) DC/DC Converter application in an automotive On−board Charger (OBC). Each phase leg is composed of series connected two MOSFET dies (totem pole). 650 V 51 mΩ MOSFET die in this H−bridge module is identical with the one used in FAM65CR51DZ1 PFC module and 650 V 82 mΩ MOSFET die is also available. Since the size of 82 mΩ MOSFET die is smaller than that of 51 mΩ MOSFET, customers can expect some reduction in switching loss and increase in conduction loss as well as increase in thermal resistance. Figure 23 illustrates the power loss comparison between 51 mΩ die and 82 mΩ die in 3.6 kW LLC converter. The data shows that 82 mΩ die has higher total power loss due to higher conduction loss. In 3.6 kW OBC system, customers can select between the two different die sizes based on the comparison of efficiency and cost. Figure 24 shows the junction temperature of 51 mΩ and 82 mΩ die in 3.6 kW LLC converter when V_{out} = 400 V and P_{out} = 3.6 kW. From the figure, both 51 mΩ and 82 mΩ die has enough thermal (T_j) margin up to 3.6 kW. Above 3.6 kW of power level, the conduction loss becomes predominant and 51 mΩ MOSFET die is required to guarantee higher efficiency (Figure 31) and thermal performance. Also, the module has an optional 150 nF high voltage snubber capacitor across the DC link for noise suppression. Figure 25 and Figure 26 illustrate the effect of the snubber capacitor. As seen from the Figure 26, oscillation in the gate loop and power switching loop reduced by around 3 dB. ♣ Along with existing Al_2O_3 DBC substrate, the module with AlN DBC substrate (FAM65HR51XS1/2) is available to maximize the thermal performance. AlN DBC version has only 1/3 of the thermal resistance of Al_2O_3 DBC version as seen from Table 4. The family of H−Bridge module is qualified for AEC Q101 and conforms to AQG324 guidelines. Table 2 in page 6 represents the electrical and thermal characteristics of all the H−Bridge DC/DC converter module.

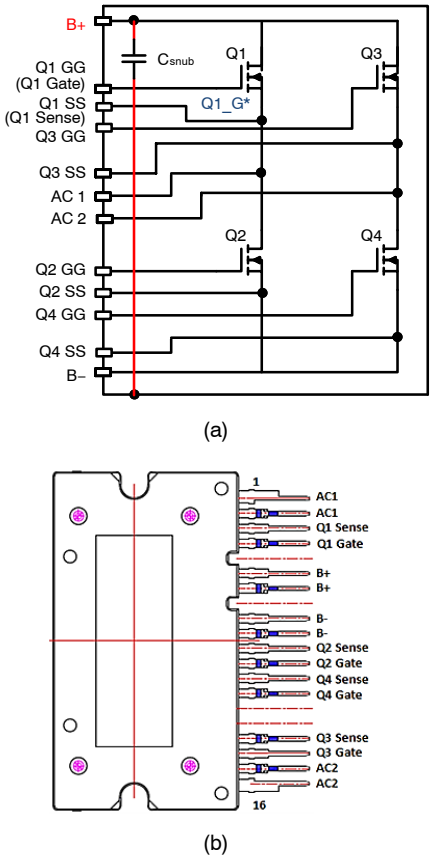


Figure 22. FAM65HR51DS1 H−bridge Module (a) Circuit Diagram and (b) Pin−out Configuration

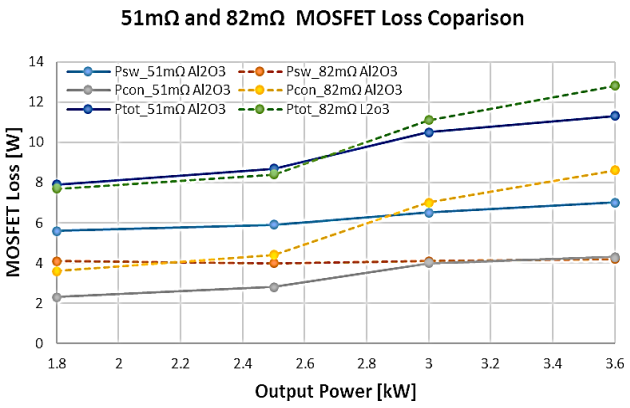


Figure 23. Power Loss Comparison between 51m and 82m Die in H−bridge Module (T_{case} = 100°C Fixed)

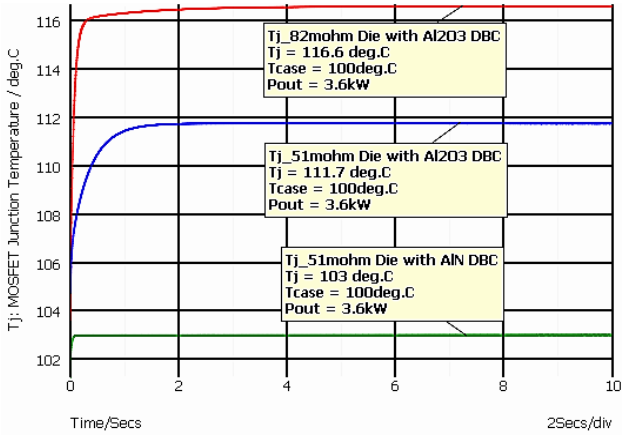


Figure 24. Junction Temperature Comparison between 51m and 82m Die in 3.6 kW LLC Converter (T_{case} = 100°C Fixed)

♣ In thermal simulation, module case temperature was set to 100°C. Then, 6th order Foster junction−case thermal impedance network, Z_{th_jc} of 51 mΩ and 82 mΩ die were applied to calculate Tj of each die.

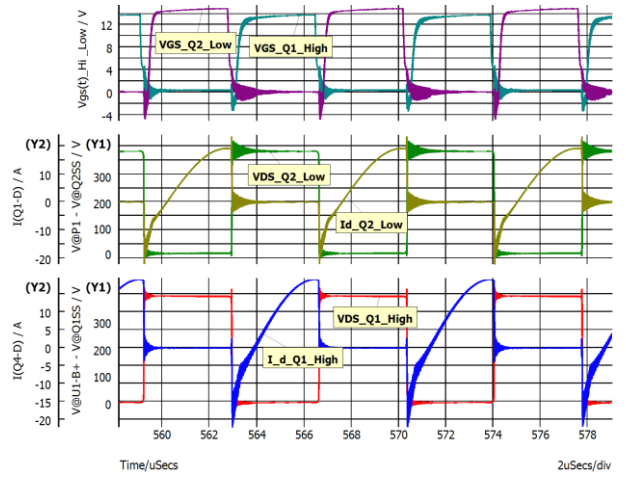


Figure 25. MOSFET Switching Waveforms in LLC Converter without Snubber Capacitor

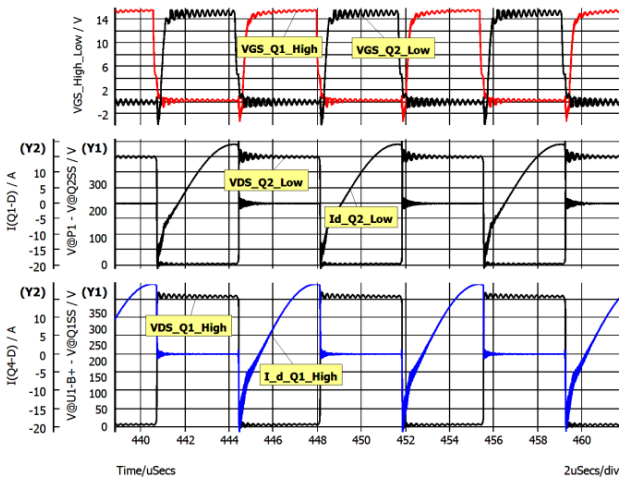


Figure 26. MOSFET Switching Waveforms in LLC Converter with 150 nF Snubber Capacitor

PERFORMANCE EVALUATION OF PFC MODULE AND H−BRIDGE MODULE USING SYSTEM LEVEL SIMULATION

As mentioned in the previous Application Note AND9813/D, the module solution has higher electrical and thermal performance comparing to the discrete device solution owing to the lower parasitic inductance in the conduction path and lower thermal resistance between the junction and heatsink. In this Application Note, the performance of the PFC and DC/DC converter module were analyzed. ♣ In the simulation, typical R_{ds_on} (25°C) = 44 mΩ was applied.

PFC Module Performance Evaluation

The simulation was carried using ANSYS Q3D package model of PFC module and SPice simulation model of the MOSFET and Diode die. Since Q3D package model of the module includes all the circuit parasitic components, MOSFET and diode simulation models work in bare die condition. The PFC function block simulations were carried in 1.8 kW~5.5 kW range. As observed from Figure 27, FAM65CR51DZ1 module (650 V/15 A Si stealth diode version) showed 98.1%~97.8% of efficiency and FAM65CR51ADZ1 module (SiC diode version) showed 98.3%~98% efficiency. This result reveals that the PFC block efficiency increases by around 0.3% with FAM65CR51ADZ1 module due to near zero reverse recovery of the high side SiC diode. The reverse recovery current from the Si diode causes the increased turn−on switching loss in the low side MOSFET. Since the MOSFET experiences hard switching in PFC boost converter, reduction of the switching loss is critical and for this reason, SiC diode is favored over Si diode and the advantage of using SiC diode becomes more evident as the power level gets higher. Also, the simulation was carried on the module with Si Stealth diode and AlN DBC, FAM65CR51XZ1 and the module shows the efficiency in between FAM65CR51DZ1 and FAM65CR51ADZ1 owing to the

superior thermal performance (lower conduction loss from lower T_j). ♣ In thermal analysis, switching loss was obtained from SPice circuit simulation. SIMETRIX v.8.3 was used as SPice simulation platform. 5−pin thermal simulation model (Figure 28) was applied as MOSFET die model and the case temperature of the simulation model was set to 100°C. And as seen in Figure 29, the conduction loss of MOSFET dies were obtained by calculating T_j and R_{ds_on} (T_j) value using closed loop control composed of MOSFET current input, R_{ds_on} vs. T_j curve fitting function and 6th order junction−case Foster thermal impedance network of each module.

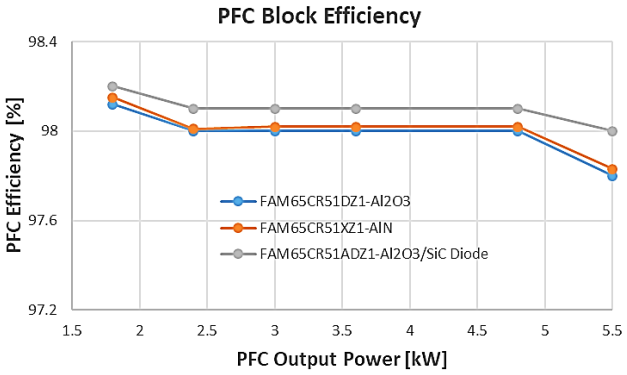


Figure 27. PFC Function Block Efficiency (T_{case} = 100°C)

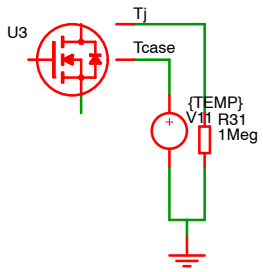


Figure 28. Five−Pin Thermal Simulation Model for MOSFET Die

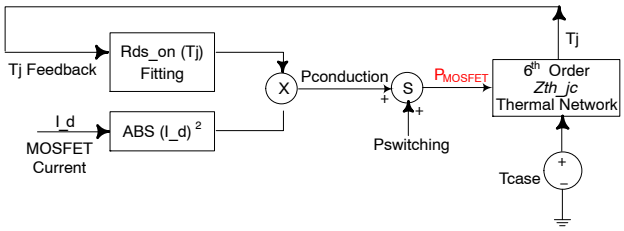


Figure 29. Thermal Analysis Block Diagram

DC/DC Converter Module Performance Evaluation

The same analysis method was applied to evaluate 51 mΩ die−based FAM65HR51DS1 module and 82 mΩ die−based NXV65HR82DS1 module in 1.8 kW~5.5 kW LLC DC/DC converter circuits. As expected, 82 mΩ die−based FAM65HR82DS1 module shows the lowest efficiency in the entire power range due to the highest conduction loss. Since LLC converter operates in ZVS condition, the benefit of the lower switching loss in 82 mΩ die is masked by high conduction loss. But the simulation result shows that 82 mΩ die works in safe operating condition and fits into 3.6 kW OBC system. Figure 30 shows the power loss comparison between 51 mΩ and 82 mΩ MOSFET die and Figure 31 illustrates the efficiency trend extended up to 5.5 kW. As the power grows over 3 kW, the conduction loss of 82 mΩ MOSFET die gets higher (Figure 29) and this high conduction loss causes low converter efficiency as seen in Figure 31. ♣ Additional simulation was carried on the AlN DBC−based module, FAM65HR51DX1 for the performance comparison. As observed from Figure 31, AlN DBC shows the highest efficiency among the three modules owing to the lowest conduction loss. But the most significant benefit of AlN DBC application is its superior thermal performance as observed in Figure 24 and Figure 32.

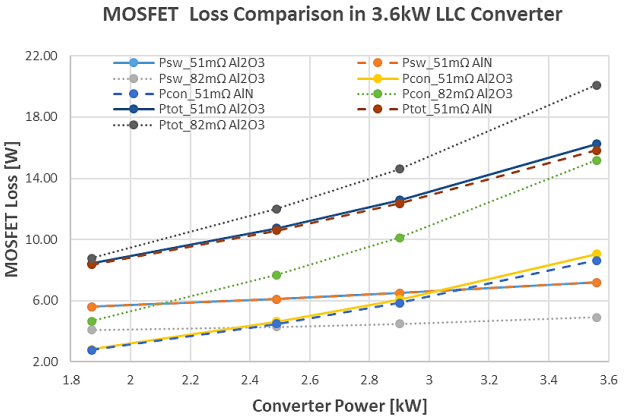


Figure 30. Power loss Comparison between 51 mΩ Die and 82 mΩ Die in H−bridge Module (T_{case} = 100°C)

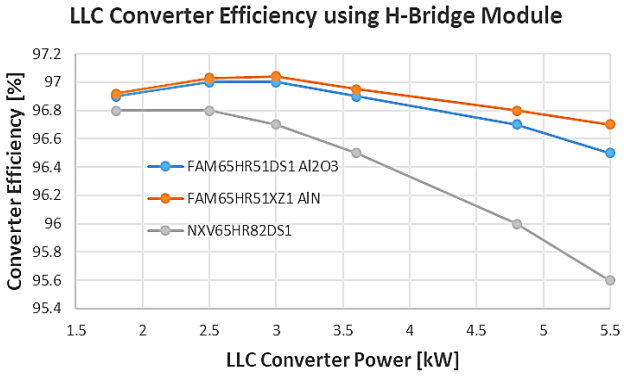


Figure 31. LLC Converter Efficiency Using H−bridge Module (T_{case} = 100°C)

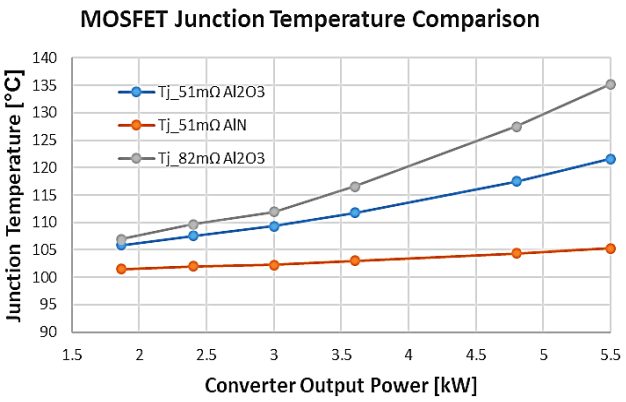


Figure 32. MOSFET Junction Temperature Comparison in H−bridge Module (LLC Converter: T_{case} = 100°C)

CONCLUSION

In this application note, ON Semiconductor's 650 V SF3 Si MOSFET−based power module family is introduced. These modules are optimized to work in On Board Charger and DC/DC converter applications. PFC modules are designed to fit into the two−phase interleaved boost PFC topology and two−channel bridgeless PFC topology. Single PFC module works best in 3.6 kW range with 98% of efficiency and parallel−connected two modules can take over 7 kW of output power. 650 V, 30 A SiC diode option and AlN DBC option are available to enhance the electrical and thermal performance of the module solution. H−Bridge modules is used typically for DC/DC converter applications including LLC converter, Phase−shifted full bridge (PSFB) and hard−switched full bridge converter. Single H−bridge module with Al_2O_3 DBC and 51 mΩ MOSFET die works optimally in 3.6 kW range with near 97% of efficiency and the module with AlN DBC provides outstanding thermal performance with only 1/3 thermal resistance of Al_2O_3 DBC and works up to 6 kW range. For cost−saving solution, ON Semiconductors also provides 82 mΩ MOSFET−based module. When 51 mΩ MOSFET−based PFC module and H−Bridge module are combined together to form a 3.6 kW OBC system, customers can expect around 95% of efficiency within 3.6 kW of output power ranges as seen in Figure 33. ♣ In terms of mechanical information including thermal interface and mounting guideline of the module, please refer to Application Note, AND9814/D.

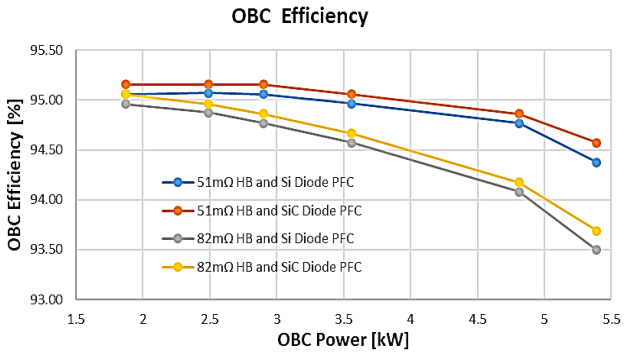


Figure 33. OBC System efficiency by combining PFC module and H−bridge module (T_{case} = 100°C)

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