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AND90025/D

A 12 W Adaptor with NCP1362 Quasi Resonant Controller

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APPLICATION NOTE

The NCP1362 offers a new Primary Side Regulation (PSR) solution targeting output power levels up to 12 W continuously in a universal−mains flyback application.

Thanks to a Novel Method, this new controller saves the secondary feedback circuitry for Constant Voltage and Constant Current regulation, achieving excellent line and load regulation without traditional opto coupler and TL431 voltage reference.

The NCP1362 operates in valley lockout quasi−resonant peak current mode control mode at high load to provide high efficiency. When the power on the secondary side starts to diminish, the controller automatically adjusts the duty−cycle then at lower load the controller enters in pulse frequency modulation at fixed peak current with a valley switching detection. This technique allows keeping the output regulation with tiny dummy load. Valley lockout at the first 4 valleys prevent valley jumping operation and then a valley switching at lower load provides high efficiency.

This application note focuses on the experimental results of a 12−W adaptor driven by the NCP1362 and on the general behavior of this controller.

Table 1. EVALUATION BOARD SPECIFICATION

Parameter	Value
Minimum input voltage	85 V rms
Maximum input voltage	265 V rms
Output voltage	12 V
Nominal output power	12 W

Figure 1. EVB Picture (Top View)

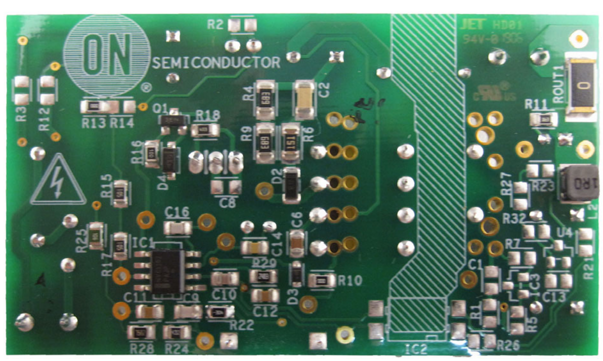

Figure 2. EVB Picture (Bottom View)

BOARD SCHEMATIC

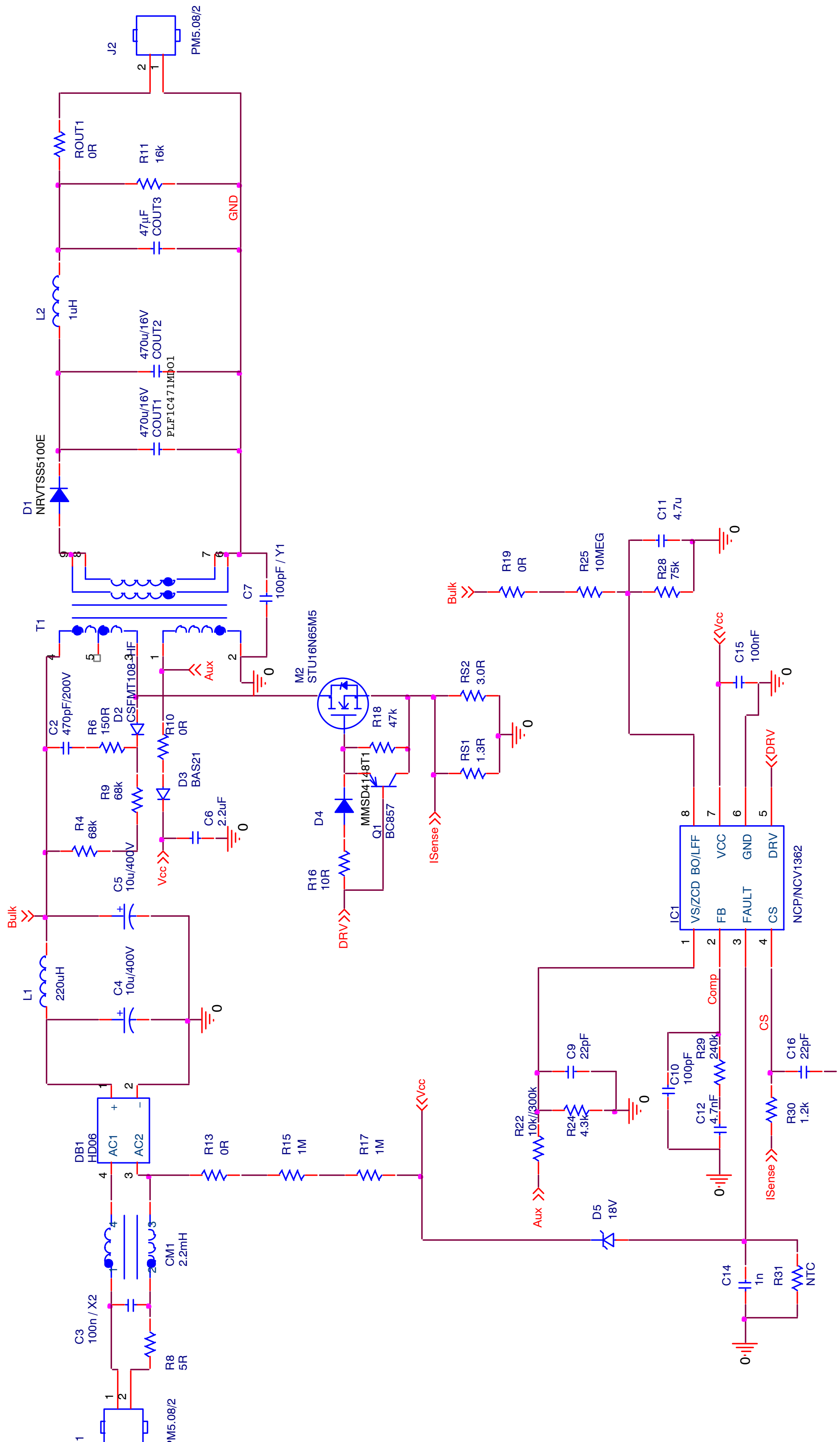

Figure 3. Evaluation Board Schematic

TYPICAL WAVEFORMS

Start−up

The start−up sequence is performed with resistors connected to the bulk capacitor or directly to the mains input voltage to reduce the power dissipation. To further reduce the standby power, the start−up current of the controller is extremely low, below 6.3 μA maximum. The start-up time is directly linked to the V_{cc} capacitor value. Also, this capacitor has to be large enough to maintain the V_{cc} voltage above $V_{cc(off)}$ level in no load condition. Indeed, in light load or no load condition, the controller operates at the minimum frequency clamp and the dead time between two cycles will be 1 ms. The V_{cc} voltage has to be kept above $V_{cc(off)}$. Finally, the last constraints regarding the V_{cc} capacitor is the start−up time. Generally, the power supply has to start in less than 3 s regardless the input voltage. Taking in account these parameters, in our application board, we have successfully tested (Figure 4) a 2.2−μF value for C_6.

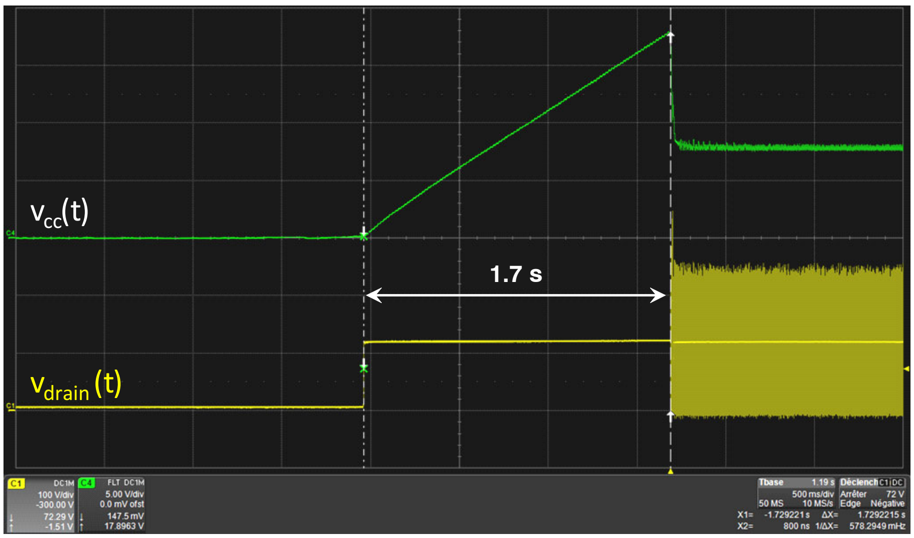

Figure 4. The Start−up Sequence is below 2 s at 85 V rms − Room Temperature

Valley Lockout

The valley lockout technique makes controller changes valley (from the 1st to the 4th valley) as the load decreases without any valley jumping. This allows extending the quasi−resonance (QR) operation range.

The following scope shoots show the operating valley as the load decreases for an input voltage of 115 V rms.

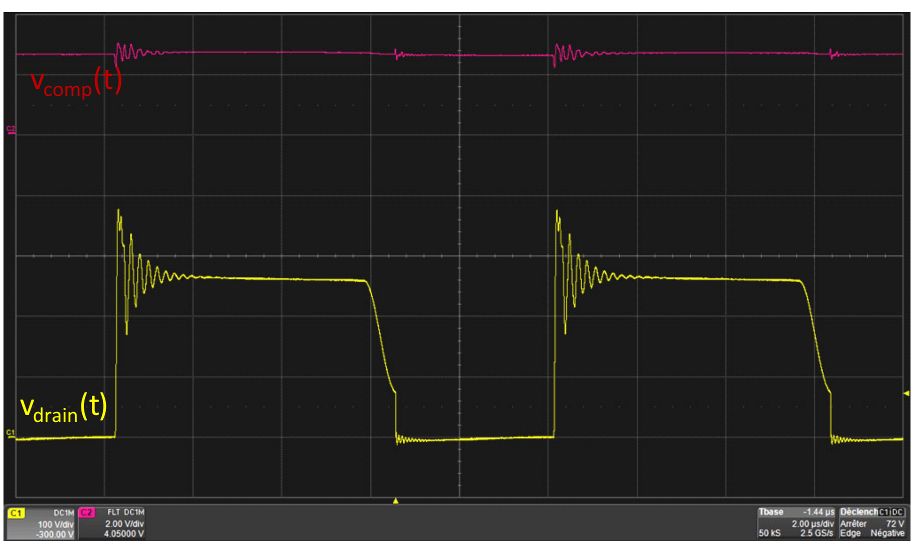

Figure 5. QR (1st valley) Operation @ 1 A / 115 V rms

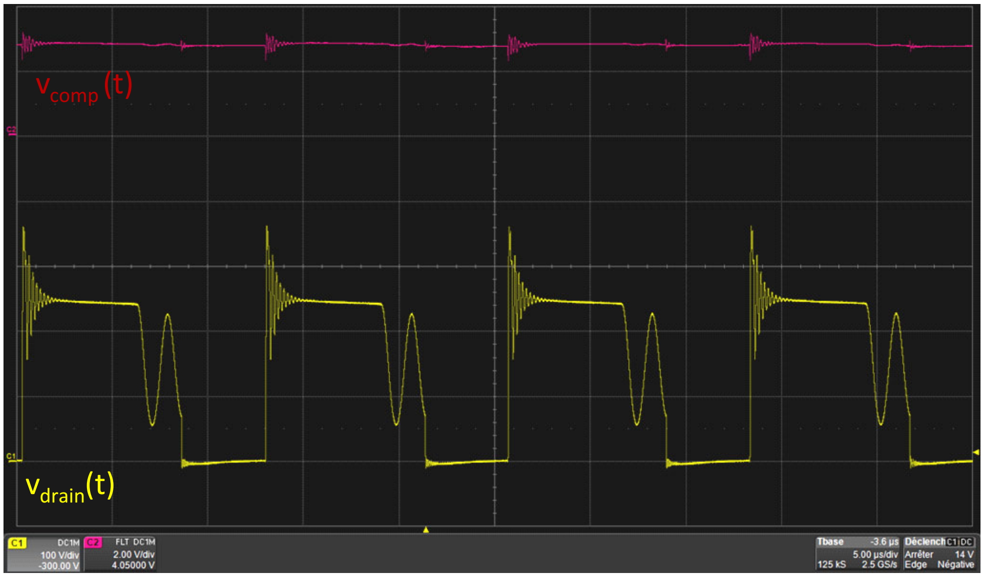

Figure 6. 2nd Valley Operation @ 0.9 A / 115 V rms

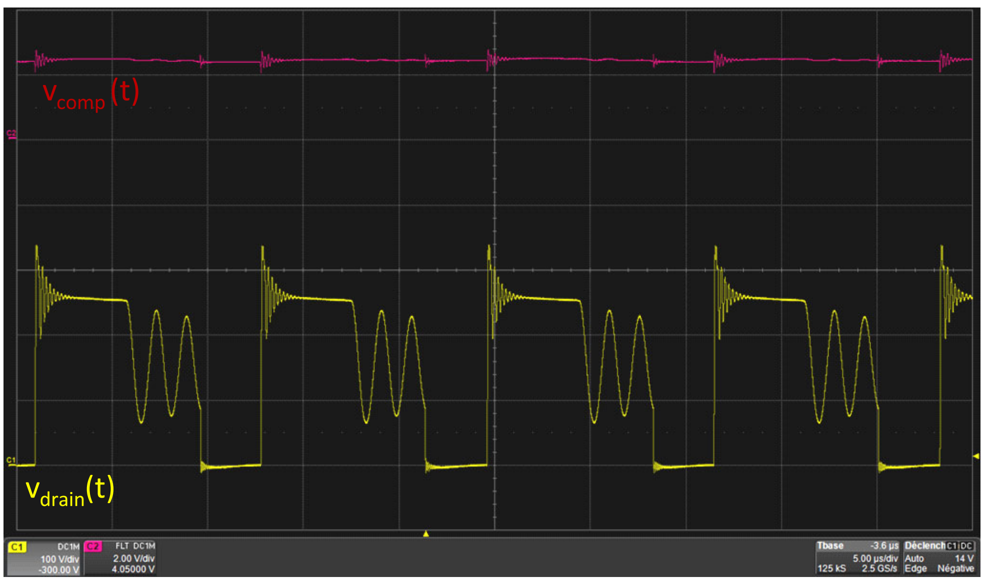

Figure 7. 3rd Valley Operation @ 0.6 A / 115 V rms

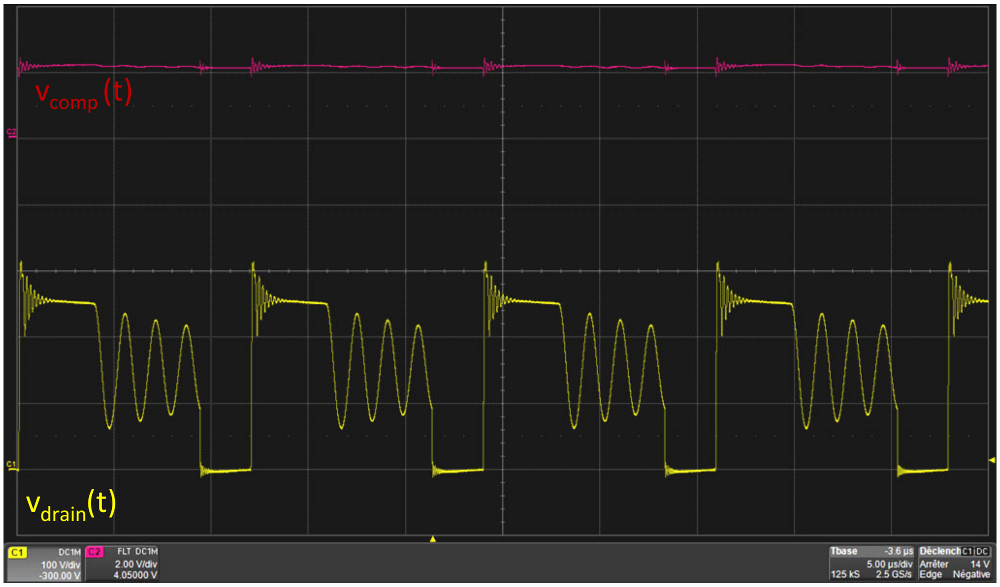

Figure 8. 4th Valley Operation @ 0.4 A / 115 V rms

Frequency Foldback Mode

If while operating at valley 4, the load further decreases, the NCP1362 will operate in Frequency Foldback (FF) mode. Practically, the circuit enters in FF mode when comp voltage drops below 2.1 V. The current is frozen to $V_{CS(VCO)}$ and regulation is made by varying the switching frequency (f_{SW} reduces if the power demand diminishes). The system reduces the switching frequency by adding some dead−time after the 4th valley is detected. Moreover, in order to keep the high efficiency benefit inherent to the QR operation, the controller turns on again with the next valley after the dead time has ended. As a result, the controller will still run in valley switching mode even when the FF is enabled.

In this 12−W evaluation boards, at 115 V rms, the switching frequency is around 73 kHz @ 0.37 A at the beginning of the frequency foldback mode. The primary peak current is frozen to $V_{CS(VCO)}$.

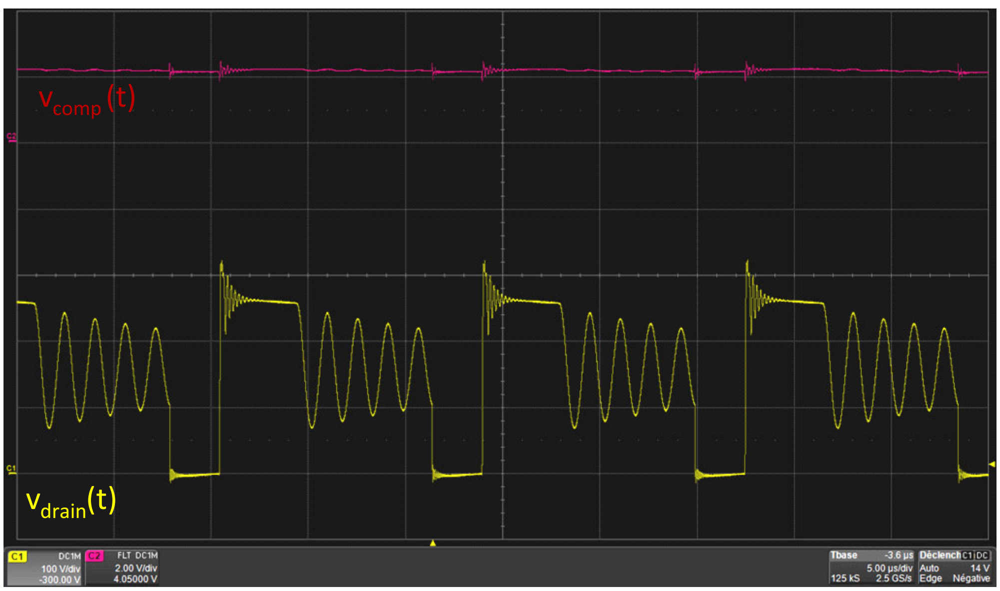

Figure 9. FF Mode & $V_{CS(VCO)}$ @ 0.37 W / 115 V rms

1−kHz Minimum Frequency Clamp

Due to the primary side regulation, the only way to have an information of the output voltage is to generate a new cycle and read the voltage on the auxiliary winding. This voltage is an image of the output voltage affected by the transformer turns ratio. For this reason, the system has to impose a minimum switching frequency to refresh the sampling on the primary side and have a good transient response. The default minimum frequency clamp is set to 1 kHz.

So the frequency clamp impose to transfer energy from primary to secondary side each ms. Because there is no load on the output, the 12−V voltage cannot be maintained to the nominal level and will increase until the OVP protection is trigged. To avoid this fault, a dummy load is generally connected on the output to dissipate this energy in no load condition but the stand−by performance will be affected. For this reason, a second frozen peak current called $V_{CS(STB)}$ is implemented in this controller to reduce to the minimum the energy transfer each cycle and so limit the power dissipated in the dummy load.

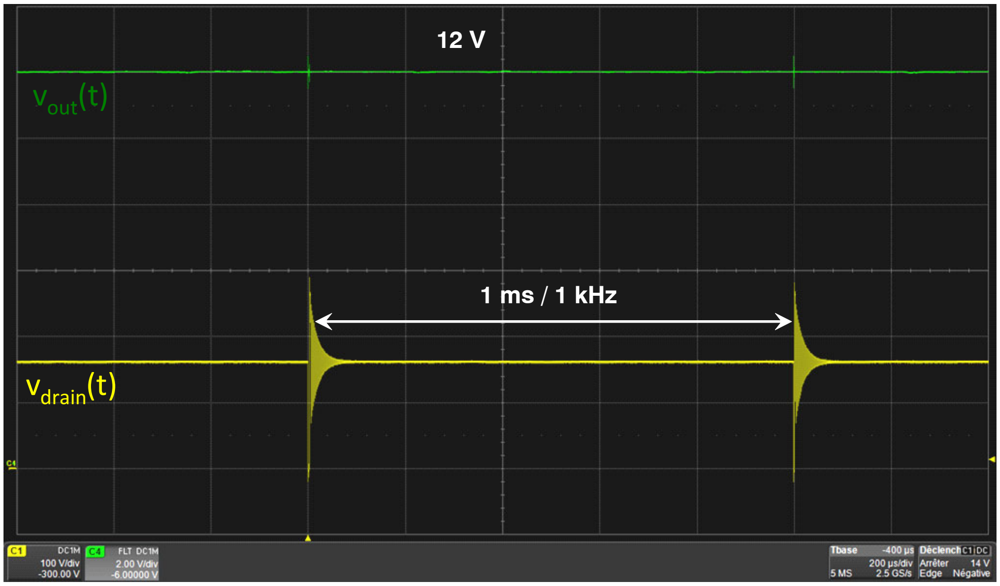

Figure 10. 1 kHz Minimum Frequency Clamp & $V_{CS(STB)}$ @ No Load / 115 V rms

Transient Load

Figure 11 and Figure 12 show an output transient load step from 0% to 50% of the maximum output power at low line and high line.

The step load response is 950 mV or 7.9% of the output voltage in the worth case.

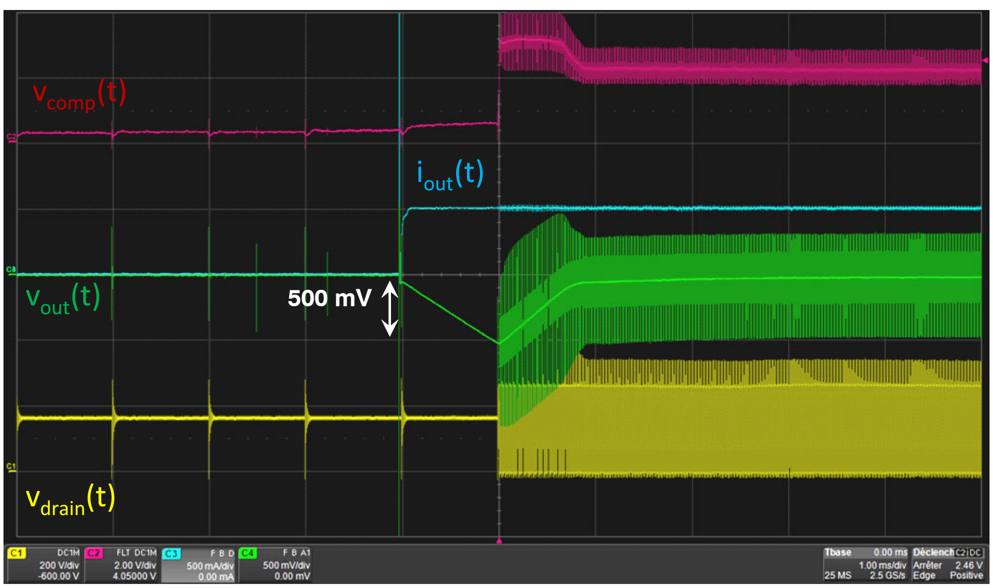

Figure 11. Step Load Response between 0% to 50% @ 115 V rms

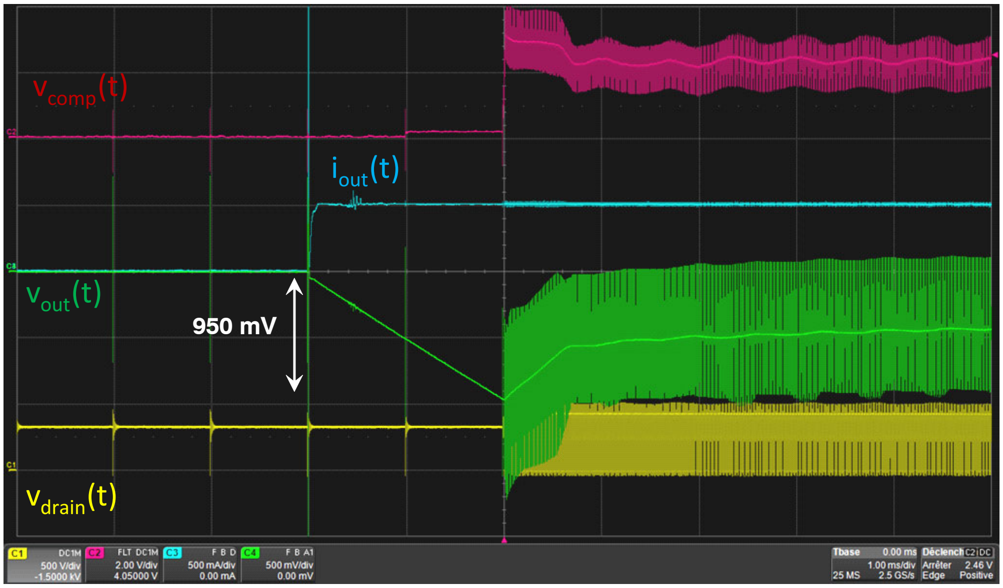

Figure 12. Step Load Response between 0% to 50% @ 230 V rms

Figure 13 and Figure 14 show an output transient load step from 50% to 100% of the maximum output power at low line and high line. The slew rate is 1 A/µs and the frequency is 25 Hz.

The step load response is ±75 mV.

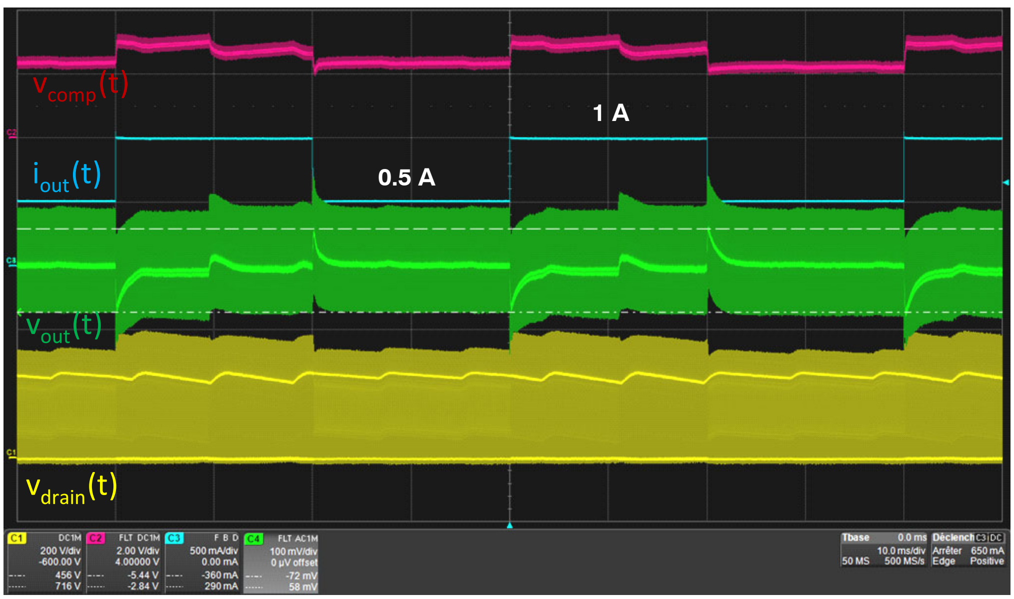

Figure 13. Step Load Response between 50% to 100% @ 115 V rms

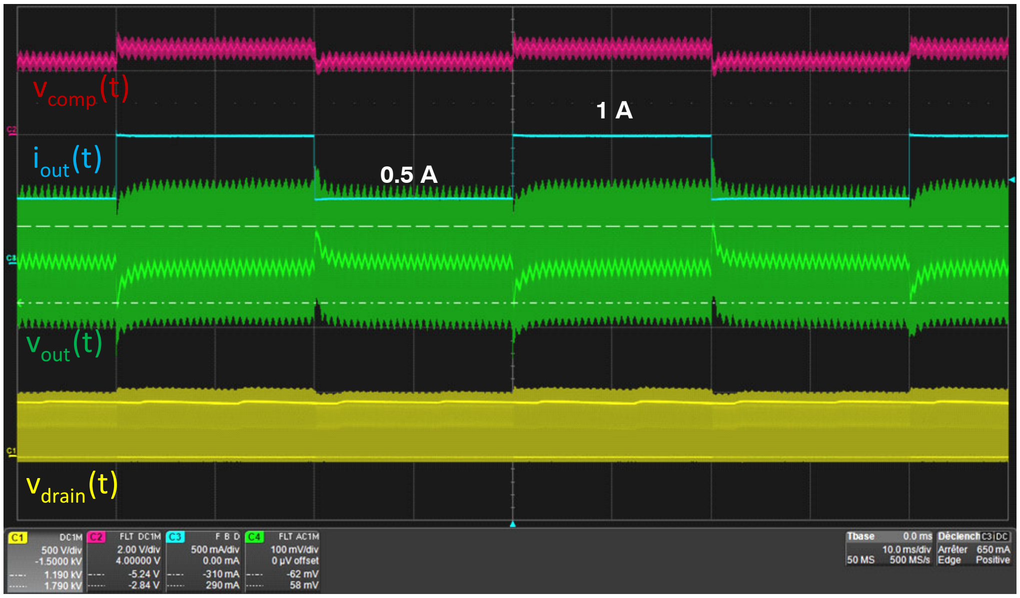

Figure 14. Step Load Response between 50% to 100% @ 230 V rms

Efficiency Results and Stand−by Performance

All measurements have been done after a 30 min warm−up phase at full load and an additional 5 min at the load under consideration.

The input power was measured with the power meter 66202 from Chroma.

The output voltage and output current were measured using digital multimeter embedded on dc electronic load 63103 from Chroma.

Table 2. EFFICIENCY @ 115 V RMS AND 230 V RMS

Input voltage	Pout (%)	Pout (W)	Pin (W)	Efficiency (%)
115 V rms	100	11.99	13.98	85.74
	75	9.09	10.55	86.16
	50	5.99	6.96	86.07
	25	2.43	2.82	86.20
	Average*	–	–	86.04
	10	1.15	1.37	83.69
	No load	–	24 m	–
230 V rms	100	12.00	13.73	87.40
	75	9.08	10.45	86.89
	50	6.01	6.99	86.02
	25	2.41	2.87	83.80
	Average*	–	–	86.03
	10	1.15	1.41	81.56
	No load	–	44 m	–

*The average efficiency was calculated from the efficiency measurements at 25%, 50%, 75% and 100% of the nominal output power.

The stand−by consumption is a key parameter for this kind of application. Thanks to the double frozen peak current, both light load and no load condition are optimized. The standby consumption is below 60 mW regardless the input voltage (55 mW at 265 V rms) like shown in the Table 2.

Please note that, if the BO pin voltage is grounded to disable this function, the power dissipation in the BO resistances will be saved. In this configuration, the no load consumption drops below 40 mW at 265 V rms. Also, by using capacitive startup, 17 mW at 265 V rms could be saved (or 13 mV @ 230 Vrms) so the standby power consumption is dropping below 30 mW.

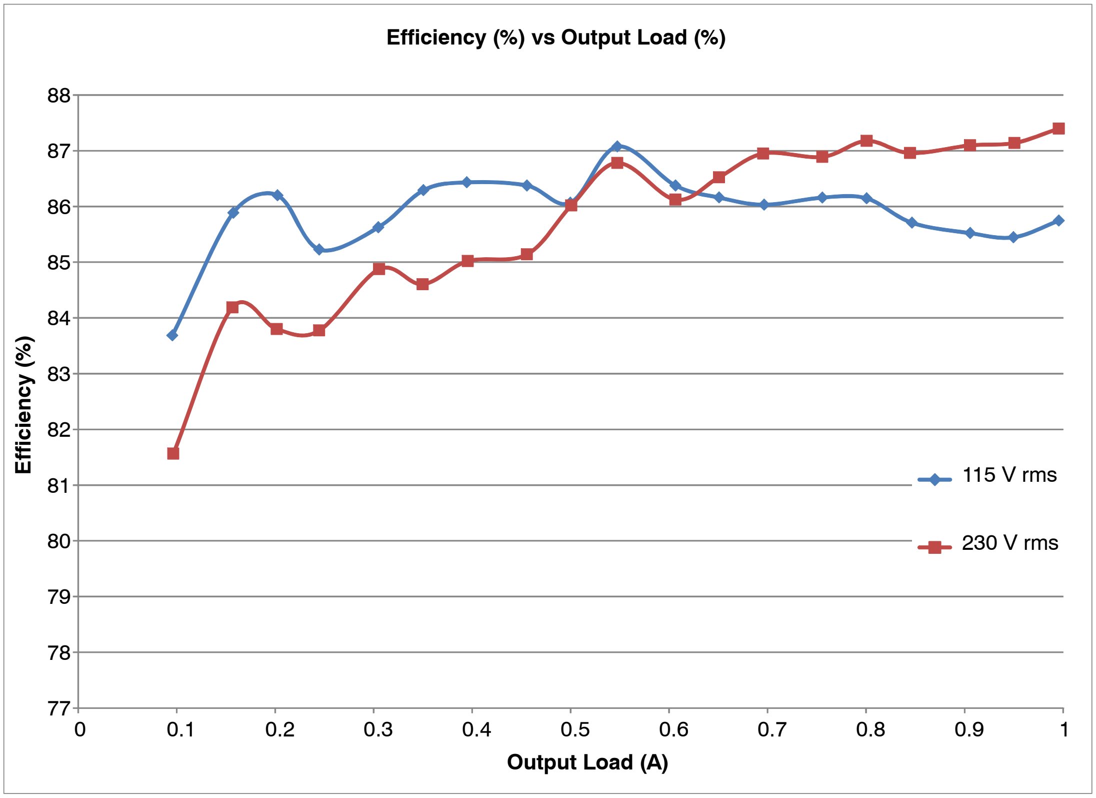

Figure 15. Efficiency (%) vs Output Current at 115 V rms and 230 V rms

If we expand our view on the light−load power consumption, in the range of 1−W output power, we can see that we can deliver more than 0.77 W in the output and keep the input consumption below 1 W.

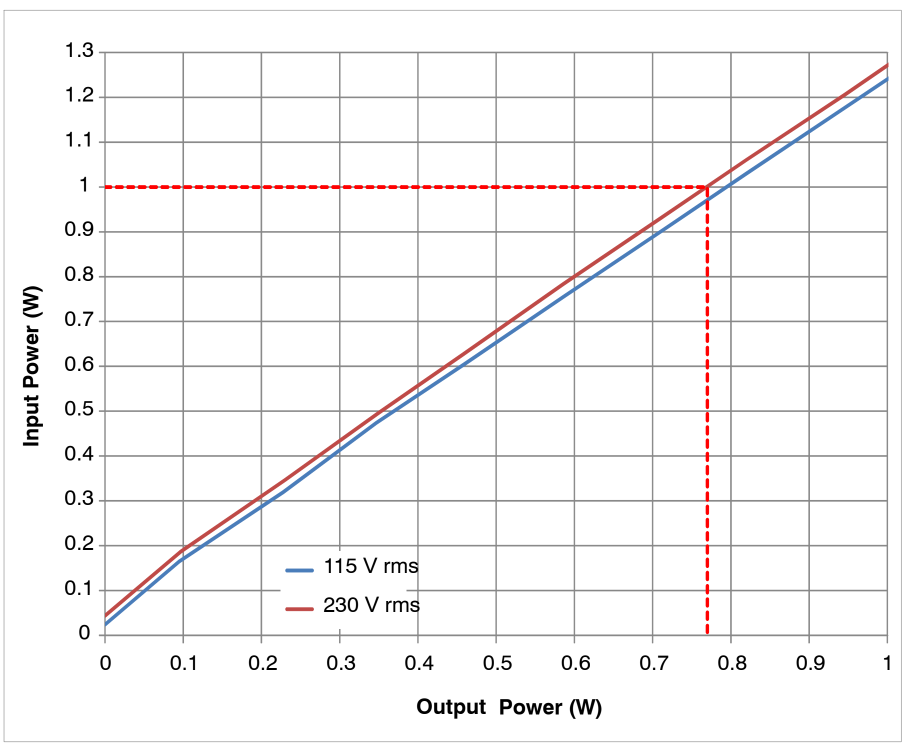

Figure 16. Low Power Consumption

Constant Voltage and Constant Current Regulation

Thanks to the NCP1362, both voltage and current are regulated to insure safe operation. When the load is below the nominal level (i.e. 1.1 A for this application), the output voltage is regulated to 12 V. Then, if the load increased, the current loop takes the control to limit the output current regardless the output voltage information. Finally, the BO/LFF pin improves the constant current regulation by sensing the input voltage and compensates the propagation delay effect at high line. These all functions put together allow us to extract the CC/CV curve depicted in the Figure 17.

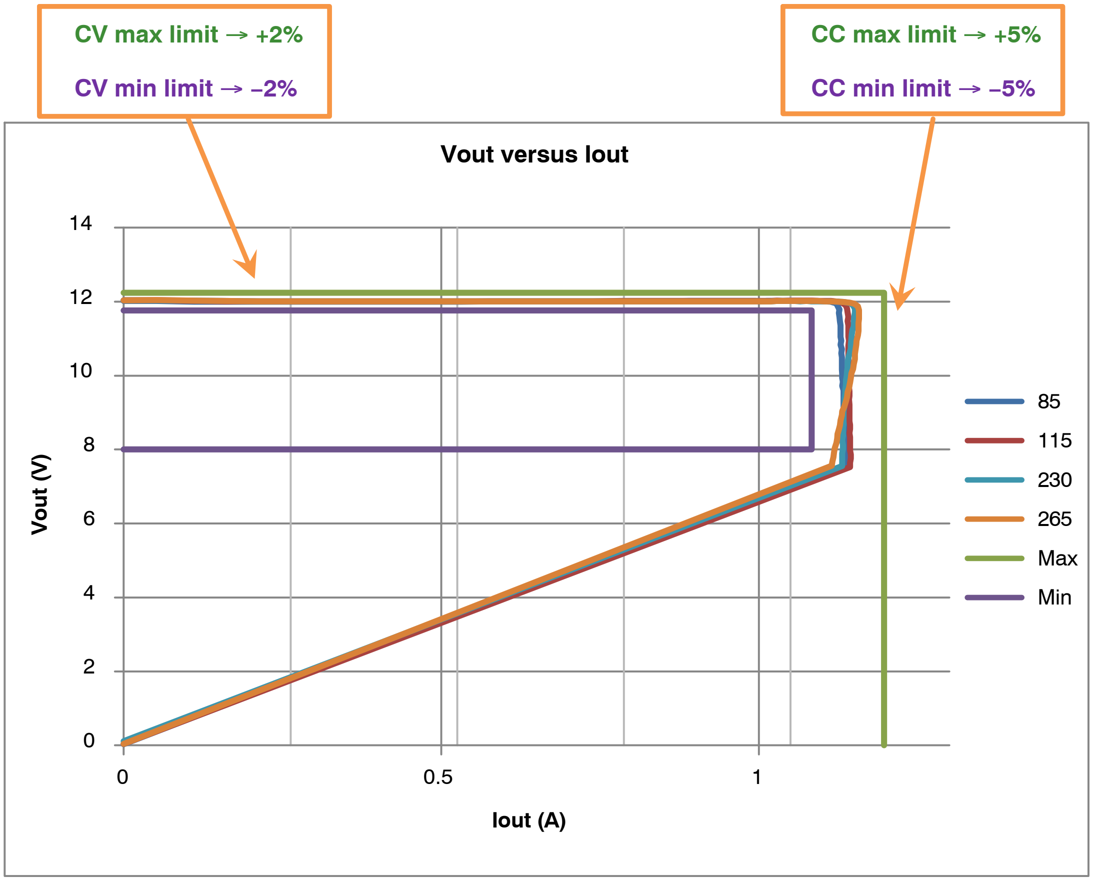

Figure 17. Constant Current (CC) / Constant Voltage (CV) Curve

Table 3. BILL OF MATERIAL (BOM)

Designator	Quantity	Description	Value	Tolerance	Manufacturer Part Number
C2	1	Ceramic capacitor, 1206, 200 V	470 pF	10%, 200 V	Standard
C3	1	X2 capacitor, 305 V	100 nF	305 V	B32921C3104
C4, C5	2	Electrolytic capacitor, 400 V	10 μF	400 V	UVC2G100MPD
C6	1	Ceramic capacitor, 0805, 35 V	2.2 μF	10%, 35 V	Standard
C7	1	Y1 capacitor, 440 V	100 pF	440 V	CD70−B2GA101KYNKA
C9, C16	2	Ceramic capacitor, 0805, 50 V	22 pF	10%, 50 V	Standard
C10	1	Ceramic capacitor, 0805, 50 V	100 pF	10%, 50 V	Standard
C11	1	Ceramic capacitor, 0805, 50 V	4.7 μF	10%, 35 V	Standard
C12	1	Ceramic capacitor, 0805, 50 V	4.7 nF	10%, 50 V	Standard
C14	1	Ceramic capacitor, 0805, 50 V	1 nF	10%, 50 V	Standard
C15	1	Ceramic capacitor, 0805, 50 V	100 nF	10%, 50 V	Standard
CM1	1	Common mode choke	2.2 mH	0.5 A	50225C
COUT1, COUT2	2	Polymer capacitor, 16 V	470 μF	20%, 16 V	PLF1C471MDO1
COUT3	1	Electrolytic capacitor, 16 V	47 μF	20%, 16 V	ECA1CAK470X
D1	1	Schottky Diode, SMB, 5 A, 100 V	NRVTSS5100	5 A, 100 V, SMB	NRVTSS5100ET3G
D2	1	Fast Recovery Diode, Axial, 1 A, 600 V	CSFMT108	1 A, 600 V, SOD123H	CSFMT108−HF
D3	1	Diode, Axial, 200 mA, 250 V	BAS21	200 mA, 250 V, SOD323	BAS21AHT1G
D4	1	Diode, SMD, 100 V	D1N4148	100 V	MMSD4148
D5	1	18 V Zener Diode	Zener	18 V, SOD123	Standard
DB1	1	Diode bridge, SMD, 0.8 A, 600V	HD06		Standard
IC1	1	PSR controller	NCV1362	SOIC8	NCV1362AADR2G
J1, J2	2	Output Connector	PM5.08/2/90	10 A, 300 V	PM5.08/2/90
L1	1	Radial Coil, 220 μH, 0.5 A, 10%	220 μF	10%, 0.5 A	7447462221
L2	1	Radial Coil, 1 μH, 3 A, 30%	1 μH	30%, 3 A	SRN4026−1R0Y
M2	1	MOSFET, 650 V, 6 A	FCU600N65	IPAK	FCU600N65S3R0
Q1	1	PNP transistor, SMD	BC857	SOT−23	BC857ALT1G
R4, R9	2	Ceramic Resistor, 1206, 0.25W, 200 V	68 kΩ	5%	Standard
R6	1	Ceramic Resistor, 1206, 0.25W	150 Ω	5%	Standard
R8	1	Through hole resistor, 1 W, 1%	5 Ω	1%	CMF605R0000FKBF
R10, R13, R19	3	Ceramic Resistor, 0805, 0.25 W	0 Ω	5%	Standard
R11	1	Ceramic Resistor, 0805, 0.25 W	16 kΩ	5%	Standard
R15, R17	2	Ceramic Resistor, 0805, 0.25 W	1 MΩ	5%	Standard
R16	1	Ceramic Resistor, 0805, 0.25 W	10 Ω	5%	Standard
R18	1	Ceramic Resistor, 0805, 0.25 W	47 kΩ	5%	Standard
R22	1	Ceramic Resistor, 0805, 0.25 W	10 kΩ // 300 kΩ	5%	Standard
R24	1	Ceramic Resistor, 0805, 0.25 W	4.3 kΩ	5%	Standard
R25	1	Ceramic Resistor, 0805, 0.25 W	10 MΩ	5%	Standard
R28	1	Ceramic Resistor, 0805, 0.25 W	75 kΩ	5%	Standard
R29	1	Ceramic Resistor, 0805, 0.25 W	240 kΩ	5%	Standard
R30	1	Ceramic Resistor, 0805, 0.25 W	1.2 kΩ	5%	Standard
R31	1	NTC, 100 kΩ at 25°C, Beta = 4190	100k @ 25°C	0.05	NTCLE100E3104JB0
ROUT1	1	Ceramic Resistor, 2512, 1 W	0R	5%	Standard
RS1	1	Ceramic Resistor, 0805, 0.25 W	1.3 Ω	1%	Standard
RS2	1	Ceramic Resistor, 0805, 0.25 W	3.0 Ω	1%	Standard
T1	1	Transformer, Wurth			7508111333r03

Conclusion

This application note has described the results obtained for a 12−W primary side regulation topology driven by the NCP1362 controller. Thanks to the dual frozen peak current in light and no load condition, the consumption have been improved. Also, the LineFeed Forward brings a better constant current regulation compared to previous PSR generation. The controller offers all necessary protections needed to safe power supply.

The author wishes to thank Wurth Elektronik for kindly providing samples for the transformer.

References

[1] NCP1362 Datasheet − NCP1362/D

[2] “Designing a PSR Quasi−Resonant adaptor driven by the NCP1362” by Yann Vaquette, AND90024/D.

[3] NCV1362WGEVB Evaluation board

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