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AND8473/D

Integrated Input Auto-Detection Mode for Video Drivers

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APPLICATION NOTE

Introduction:

Consumer electronic applications have always been demanding in terms of space and cost reductions. In addition to these two requirements, power saving has become increasingly important in every system with the recent changes in ENERGY STAR® standards. These considerations constituted the main focus for the next video driver generation offered by ON Semiconductor.

Today, the majority of systems which require analog video, are driving a Cvbs signal to preserve a standard definition capability as a backup output. Primarily, a YPbPr signal is needed for the analog 1080i high definition.

The chipset manufacturers for DVD and Blu−ray® players are facing energy saving challenges when the system has to enter into a “sleep mode”. This means that only part of the chipset functional blocks are turned off. Meanwhile the various supplies on the system are still active. This involves the very same supplies are also active for the video drivers and it imposes additional control to activate/deactivate the video driver. Consequently, if no enable logic is present, the power consumption is quite significant.

From the ENERGY STAR standards, it can be read that any DVD player, Blu−ray player or Set−Top Boxes have to consume less than 1 W in standby mode (see specification of ENERGY STAR Program Requirements for Audio/Video Version 2.0 – Figure 1).

To comply with this specification, chipset manufacturers need to keep their power supply consumption as low as possible. When the system enters into a standby mode, the integrated video DACs are turned off. Consequently, no more signals are driven through the video drivers.

The NCS2584 has the capability to automatically detect the presence of the video signals at its inputs (see Figure 2). Then, it is able to turn the drivers ON or OFF respectively when the input signals are active or not.

Table 1. SUMMARY OF ENERGY EFFICIENCY REQUIREMENTS PRODUCT

Product	Requirements		
	Tier 1 November 2009	**Tier 2 July 2010**	**Tier 3 March 2012**
Consumer AV Products	• Standby mode power consumption limit = 1 W	• Sleep mode power consumption limits (base, networking / control) • Auto Power Down requirements • Product function power consumption limits (display, networking / control, optical disc player) • Amplifier efficiency requirements (medium, large) • Idle power limits for all products if option to disable APD	• Sleep mode power consumption limits (base, networking / control) • Auto Power Down requirements • **More stringent** product function power consumption limits (display, networking / control, optical disc player) • **More stringent** amplifier efficiency requirements (medium, large) • Idle state power consumption limits for all products if option to disable APD
All Other AV Products	• Sleep mode power consumption limits (base + networking / control) • Auto Power Down requirements (for Digital Signal Processors, this is the only requirement) • Product function power consumption limits (display, networking / control, optical disc player) • Amplifier efficiency requirements (medium, large) • Idle state power consumption limits for all products if option to disable APD		

Figure 1. ENERGY STAR Specification Abstract

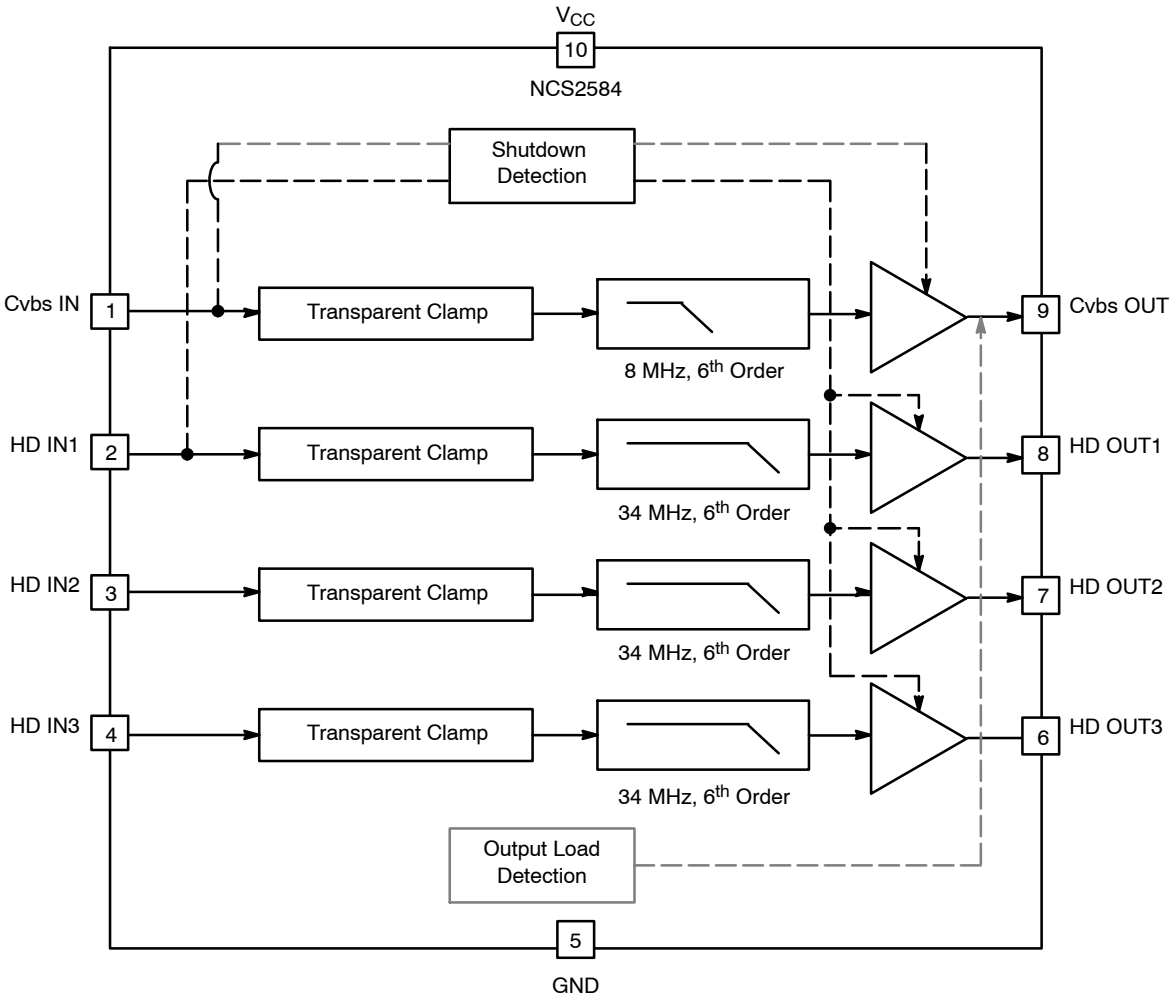

Figure 2. NCS2584 Block Diagram

The Signal Challenge:

Before approaching the challenge at the device level, a signal overview on the timing specifications will be presented in this section as the timing was the key parameter for this integrated input detection. On Figures 3 and 4, the Cvbs (480p) and on Figure 5, YPbPr (1080i) are the two types of signal that are introduced below as they are the analog signals driven in the most current Blu−ray Players and Set−Top−Boxes.

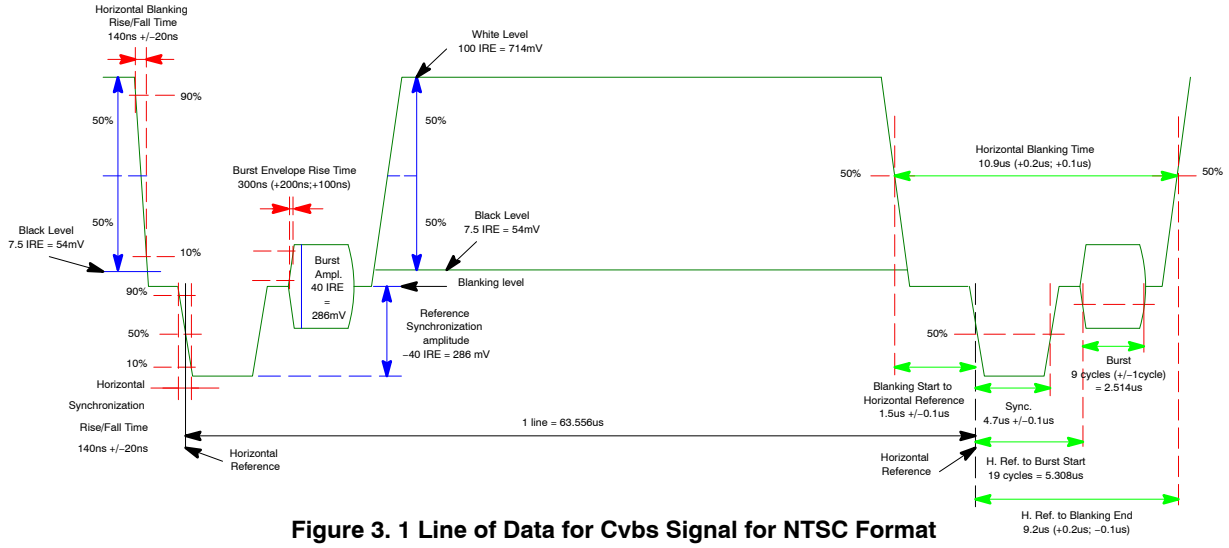

Figure 3. 1 Line of Data for Cvbs Signal for NTSC Format

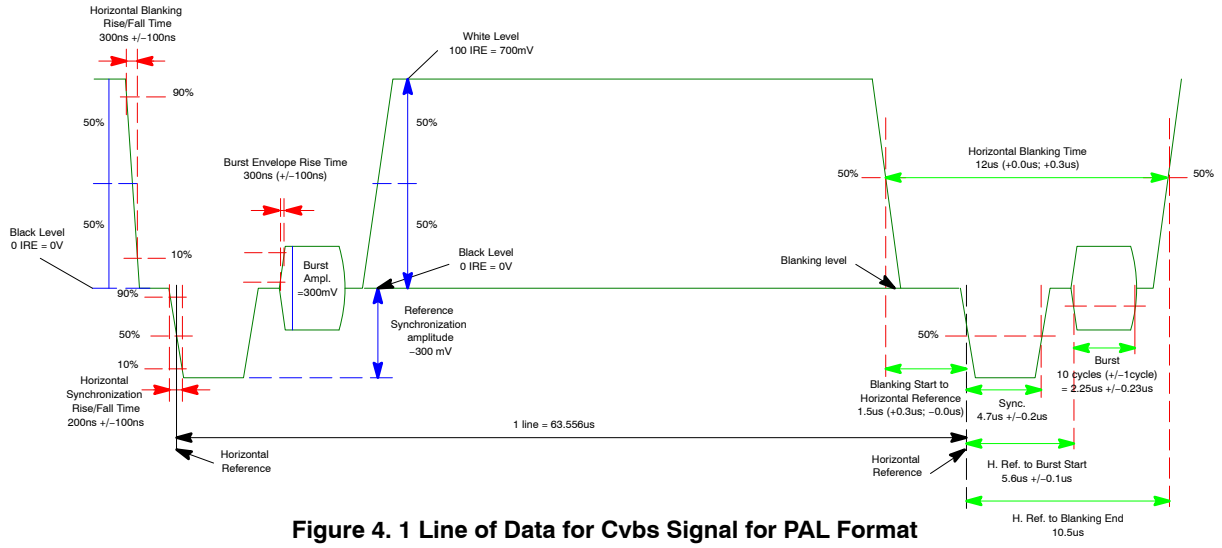

Figure 4. 1 Line of Data for Cvbs Signal for PAL Format

The focus will be put on the shortest timing specifications to understand the relevance of the T_{on} and T_{off} time specifications.

So, as it can be noticed, the horizontal negative peak synchronization time of the Standard Definition Cvbs (NTSC − Figure 3 and PAL − Figure 4) equals 4.7 μs is logically slower than the 1080i signal (592.59 ns).

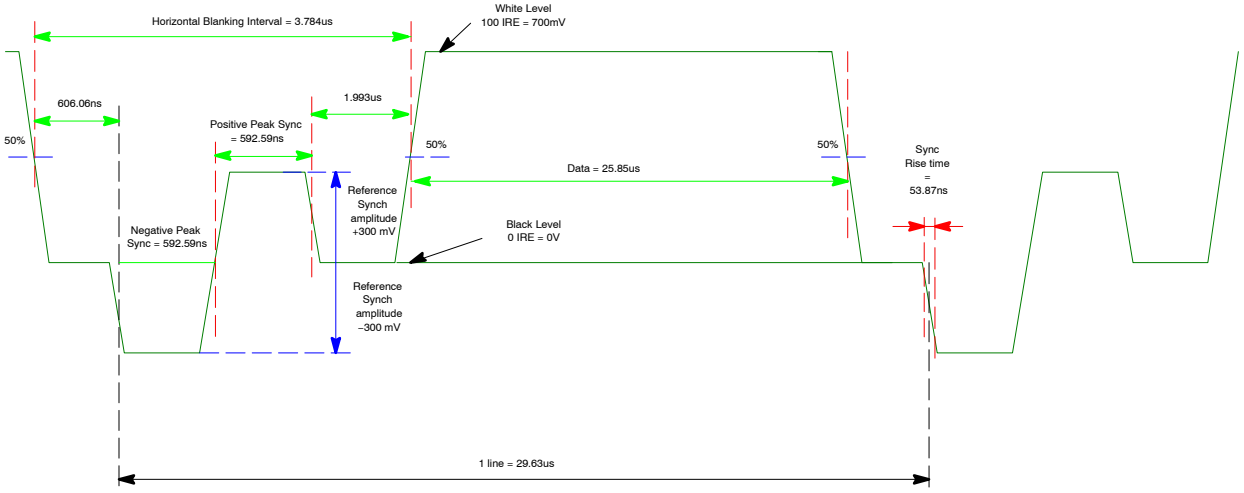

Figure 5. 1 Line of Data for 1080i60 Video Signal

The question could be asked about the vertical synchronization part of the signal. Figure 6 describes this part of the 1080i signal. It shows that the fastest timing information is also the negative synchronization which remains identical (592.59 ns).

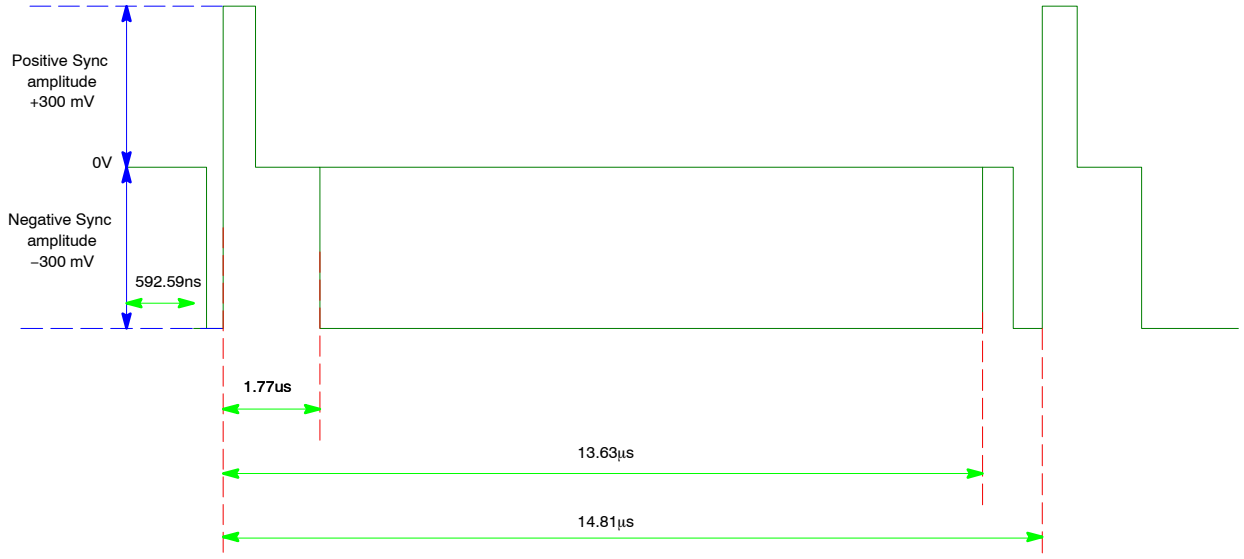

Figure 6. Vertical Synchronization for 1080i60 Signal

Then, it must be proven that turning ON the video driver fast enough, will allow the picture integrity to be preserved.

The Input Activation Principle:

Three questions need to be considered. When do we really start losing the picture? Consequently, how long does it take to the video driver to turn ON and how long does it take to the video driver to turn OFF?

It is known that every beginning of a picture starts with a vertical synchronization and every beginning of a line starts with a horizontal synchronization. In addition to that, one must take into account the boot sequence not only of the chipset from a complete OFF mode to a complete active mode, but also from a standby mode (where only some key blocks from the chipset are deactivated) to an active mode. Only after understanding these cases will the turn ON time be defined. Today, as every chipset is different one from another it can be generalized that a chipset is activated in the order of at least a tens of a microsecond from an OFF state or a standby state, and then it sends the video data.

The principle of the NCS2584 is that it can turn ON automatically in less than 2 µs as soon as it detects an input signal of a period greater than the length of a standard definition line which is equal to 63.556 µs (see Figure 3 and 4). In addition to the timing consideration, the detection is also based on amplitude thresholds. It ensures the user that even if there is a glitch on the line, the part doesn't turn ON accidentally and goes into an undetermined state.

The graph Figure 7 shows the measurement of the turn on time. It demonstrates that the theoretical turn on time is planned to be less the 2 µs. In this amount of time, the detection block timing delay is negligible (around 120 ns). The analog activation of the other stages like the 6^{th} order filter and the amplifier bring it up to 2 µs. In order to have a controlled signal, the equipment used here, is a signal generator with a programmed gated burst square wave signal. It allows the device alternatively to turn ON and OFF. Consequently, the T_{on} and T_{off} time can be measured. The top half screen represent the input and output signals while the bottom part of the screen is the zoom when the first signal edge appears.

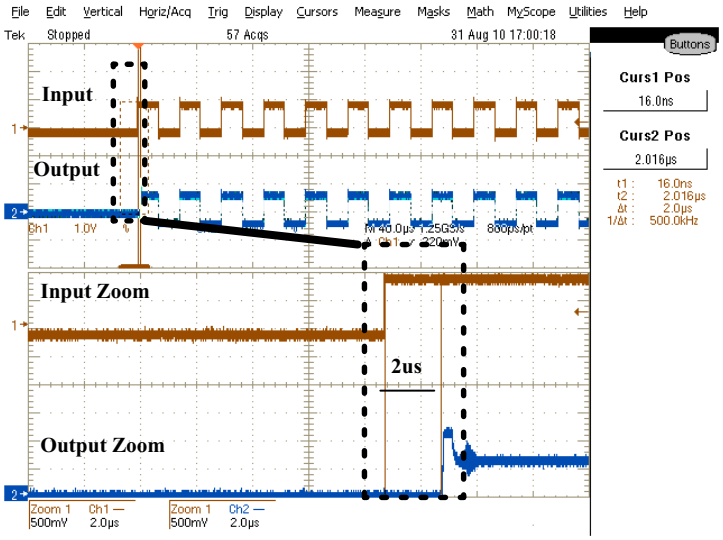

Figure 7. Turn ON Time Measurement

Below, Figure 8, shows a measurement result of the boot timing of a video chipset. It compares the sequence with a regular driver and the NCS2584. The first peak of the top curve corresponds to the moment when the user presses the ON button. It can first be noticed the overshoot when the system boots is significantly disappears due to the lack of horizontal synchronization after the spike. The video don't turn ON as no proper video signal is alive. Then, no information is lost due to the fast detection.

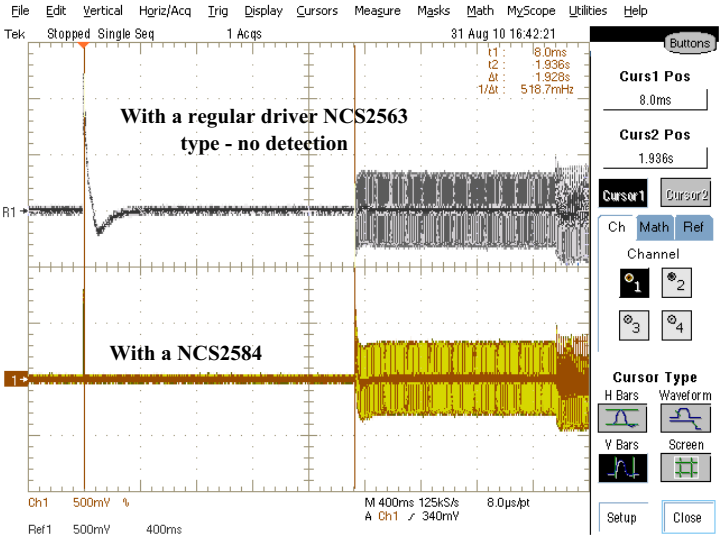

Figure 8. Boot Sequence of a Video Chipset

The signal during the boot sequence (OFF state to ON state) stimulates the part and activates it, then the NCS2584 turns ON fast enough to drive the video data without losing any information.

After defining how the integrated detection works, where it is happening needs to be identified.

For the standard definition channel there is no choice, and a detection point is consequently on this line as illustrated by Figure 2.

For the high definition line which constitutes three components: The Y, the Pb and the Pr signals, the detection is only performed on the Y channel. The reason for this is it that only the Y channel contains the synchronization information for such consumer applications.

To summarize the previous scenarios, the NCS2584 can detect the synchronization of a continuous video signal fast enough to preserve the picture integrity. Either from an OFF state to an ON state or from a standby mode to an ON state,

the NCS2584 can also be activated fast enough to drive the video patterns without any degradation of the picture.

The Deactivation Principle:

For the deactivation function, the video content is shutdown. The only concern is now to turn the part OFF in an amount of time determined by the length of one standard definition line (between two horizontal synchronization), in order that the human eye cannot detect any transition. In addition, the device makes sure the data are not interrupted mistakenly. For example, if the screen is black for several second, the voltage level will be constant and theoretically at 0 V but if the synchronization are still present, so the device must stay activated. For that matter, and as mentioned earlier, the function detects if there is a signal with a period of at least one time the period of a standard definition line (63.556 μs). When the chipset runs into a standby mode, the DACs output voltage levels are generally set to 0 V. As no more stimulus is present on the inputs of the NCS2584, the part goes into a very low current shutdown mode (5 μA) until the next stimulus re−activates the part. It is now consuming about 5 μA x 3.3 V = 16.5 mW while a regular video amplifier would consume up to 50 mA x 5 V = 250 mW (1/4 of the ENERGY STAR specification budget). Typically it takes 140 μs to shutdown (see Figure 9). The human eye can only detect a transition between two very different frames, a black screen followed by a white screen for example. This theoretical threshold frame rate is equal to 60 Hz (60 frames per second) or a period of 16.67 ms. It has now been proven that Toff ≤ 16.67 ms so the end user will not have any discomfort during their viewing experience.

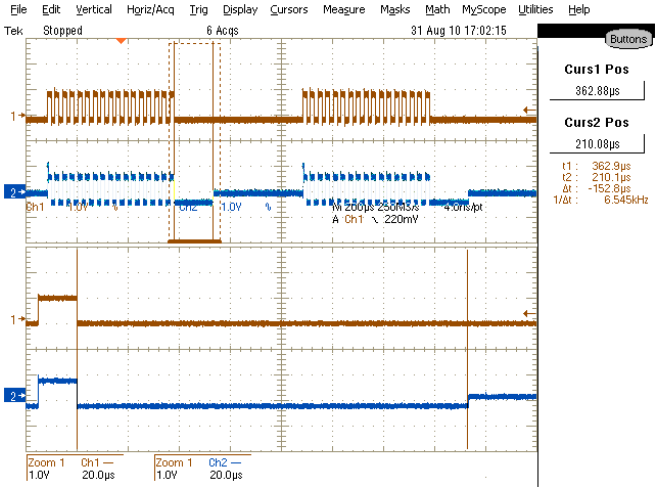

Figure 9. Turn OFF Time Measurement

This particular feature plays a major role by saving power supply to the system without any logic command from the chipset. It helps to comply with the new energy saving trends that hardware designers are facing.

Conclusion:

This latest generation of analog video drivers has been designed to support the power saving challenges of the consumer industry. Due to this embedded detection feature, system designers will not have to worry about how to improve their design for the analog video outputs. The NCS2584 will help to simplify the control of the video driver and will also be the best fit in an ENERGY STAR design compliance environment.

The question can remain on identifying if the TV RCA cable is plugged or not, and how is it controlled (see AND9046/D).

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