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AND8454/D

32 W, 32 V Universal Input AC-DC Printer Adapter using the NCP1237

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APPLICATION NOTE

Introduction

This ac adapter demonstration board targets a printer adapter application with a 32 V output, and a power capability of up to 80 W transiently (for 150 ms) and 32 W permanently. It exceeds the efficiency and standby power requirements of the US ENERGY STAR® Specification for External Power supplies (EPS) version 2.0.

It is built around the NCP1237, a fixed-frequency controller featuring frequency foldback and Soft-Skip™ to maximize efficiency in light load conditions. Additional functions include dual-level overcurrent protection for transient peak power, line voltage sensing for Brown-out protection, as well as overpower compensation to ensure a constant overload protection independent of the input voltage (for a detailed description of all these functions and recommendations on how to use this controller, please refer to the NCP1237 datasheet and other related documents at www.onsemi.com.

Specification

The demonstration board must operate across universal inputs, 85 Vac to 265 Vac (47 Hz to 63 Hz), and supply a regulated 32 V output capable of delivering 1 A continuously (32 W), and up to 2.5 A (80 W) for at least 120 ms, as defined in Figure 1. Its average efficiency as defined by ENERGY STAR should be higher than 87% (therefore exceeding the EPS 2.0 requirement of 84%), and its no load input power must be lower than 150 mW. In addition, the efficiency at an output of 1.0 W must be greater than 70%. The specification is summarized in Table 1.

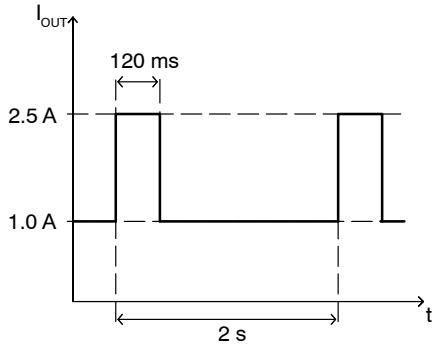

Figure 1. Transient Output Current Specification

Table 1: Summary of Specifications

Requirement	Min	Max	Unit
Input Voltage	85	265	Vac
Line Frequency	47	63	Hz
Output Voltage	31.5	32.5	Vdc
Output Current	–	1.0 (2.5 transient peak for 120 ms)	Adc
Output Power	–	32 (80 transient peak for 120 ms)	W
Average Efficiency (as defined by ENERGY STAR)	87	–	%
Efficiency at an output power of 1.0 W	70	–	%
No Load Input Power	–	150	mW
Output Ripple Voltage	–	±200	mV

Design Procedure

We will only highlight the design of the main components of the power supply. For a more comprehensive step-by-step design of a flyback converter, please refer to the ON Semiconductor website (www.onsemi.com).

The demonstration board schematic is based on the typical application schematic for the NCP1237, provided in Figure 2.

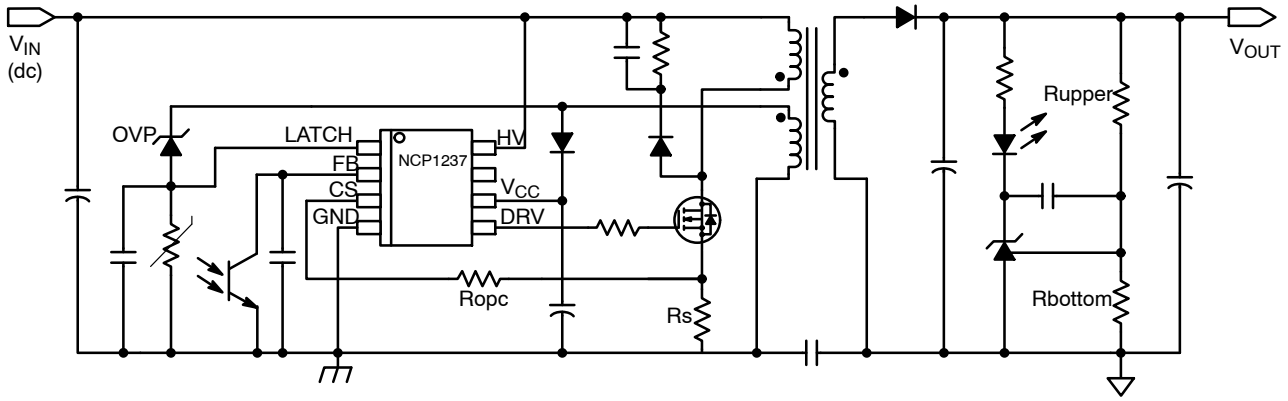

Figure 2. Typical Application Schematic

There is not one single recipe to design a flyback converter: one can initiate the design procedure with any of the power components and walk his way through the schematic. Each selection of a component restricts the choice for the others in order to meet the specification.

For the design of this printer adapter, the specification the most restrictive is the efficiency requirement: with such an aggressive target, the design procedure must focus on minimizing the losses. In a nutshell, we will strive to combine low peak current, well balanced reflected voltages on primary and secondary side, and low dissipation in snubbers and clamps.

Output Rectifier

We'll start the design from the secondary rectifier. The reason is that ON Semiconductor offers a low V_F Schottky diode very well suited for a high efficiency adapter, the MBR20H150, but its maximum reverse voltage is 150 V. After deducing the output voltage, and applying a derating on the maximum reverse voltage, there is not much voltage left allowed across the secondary winding. Refer to Figure 3 for a graphical explanation of the following calculations.

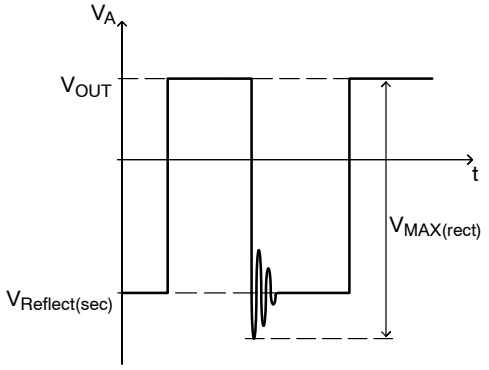

Figure 3. Typical Voltage V_A on the Anode of the Rectifier

The maximum voltage that we allow across the rectifier is:

$$V_{MAX(rect)} = V_{RRM} \cdot K_{derating(rect)} \quad \text{(eq. 1)}$$

Where $K_{derating(rect)}$ is the derating applied on the maximum reverse voltage across the rectifier, and V_{RRM} the maximum reverse voltage allowed for the rectifier.

Solving for a derating of 80 % and a reverse voltage of 150 V, $V_{MAX(rect)}$ must be less than 120 V. We have to keep in mind that this not only includes the reflected voltage from primary during on time, but also the voltage peak that appears on the anode of the rectifier when the MOSFET turns on. Let us now define K_{snub}, the ratio between the maximum negative voltage ($V_{MAX(rect)} - V_{OUT}$) and the reflected voltage $V_{Reflect(sec)}$: it represents the amount of overshoot beyond the reflected voltage plateau. The larger this ratio is, the lower the dissipation in the snubber that will be placed across the secondary rectifier.

$$V_{Reflect(sec)} = (V_{MAX(rect)} - V_{OUT}) \cdot K_{snub} \quad \text{(eq. 2)}$$

Solving for a snubber ratio of 1.4 and an output voltage of 32 V gives a reflected voltage of 62.5 V.

This imposes the turns ratio of the transformer, following equation 3.

$$V_{Reflect(sec)} = V_{IN(dc)} \cdot \frac{N_S}{N_P} \quad \text{(eq. 3)}$$

Solving for the maximum $V_{IN(dc)max}$ of 375 V, it gives a turns ratio $N_P / N_S = N = 6$

Primary MOSFET

Knowing the output voltage and the turns ratio, we can calculate the reflected voltage from secondary side to primary side of the transformer during off time:

$$V_{Reflect(prim)} = V_{OUT} \cdot N \quad \text{(eq. 4)}$$

Solving for the values calculated above gives a reflected voltage across the primary winding of 192 V.

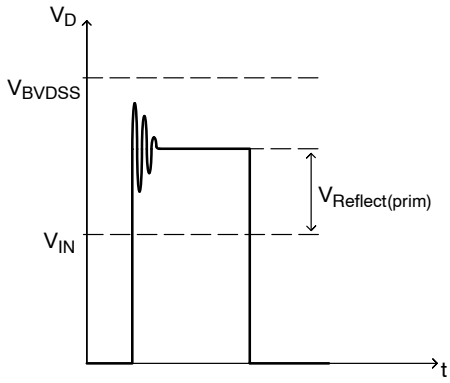

Figure 4. Typical Voltage V_D on the Drain of the MOSFET

As shown on Figure 4, we can now calculate the minimum breakdown voltage of the MOSFET V_{BVDSS} using equation 5. $K_{derating(switch)}$ is the derating applied on the breakdown voltage of the transistor and K_{clamp} the ratio between the maximum voltage that appears on the drain of the transistor and the reflected voltage to the primary.

$$V_{BVDSS} = \frac{V_{IN(dc)max} + V_{Reflect(prim)} \cdot K_{clamp}}{K_{derating(switch)}} \quad \text{(eq. 5)}$$

Solving for a clamped-to-reflected voltage ratio of 1.4 and a derating of 80%, we find that V_{BVDSS} should be at least 805 V.

We will choose an 800 V MOSFET and adjust the clamp voltage.

Note that if no derating is applied on the MOSFET and/or the rectifier, and/or we use the avalanche capability of the these components to clamp the voltage overshoots, the same converter could be designed with a 650 V or even a 600 V MOSFET (and a lower turns ratio, of 5 for example). However we will stick to the safe design calculated above, as our purpose is primarily to demonstrate the capabilities of the NCP1237 controller.

Transformer

We will design the transformer in such a way that the converter runs in discontinuous conduction mode (DCM) in normal conditions, and enter continuous conduction mode (CCM) during peak power transients. Since the duration of these transients is safely clamped by the NCP1237's transient timer, the transformer doesn't need to be designed thermally for the 80 W peak power, but only for 32 W. It must however be able to deliver the peak output current of 2.5 A without saturating.

At the transition from DCM to CCM, the converter runs in Borderline Conduction Mode (BCM), and the off time duration corresponds exactly to the demagnetization time of the transformer. In other words, the secondary current reaches 0 exactly when the MOSFET is turned back on, as shown on Figure 5.

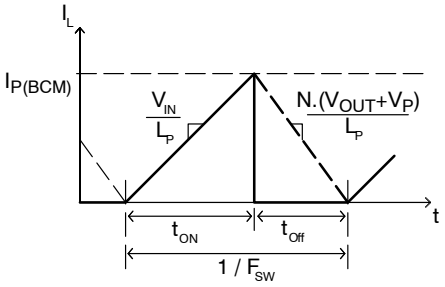

Figure 5. Transformer Current at the DCM-CCM Transition

As a result, we can write:

$$t_{ON} + t_{OFF} = \frac{L_p \cdot I_{P(BCM)}}{V_{IN}} + \frac{L_p \cdot I_{P(BCM)}}{N \cdot (V_{OUT} + V_F)} = \frac{1}{F_{SW}} \quad \text{(eq. 6)}$$

In addition, the output power can be defined as the power transferred from primary to secondary multiplied by the overall efficiency η of the conversion; the transferred power being the energy stored in the primary inductor during one cycle multiplied by the switching frequency. In the BCM case the output power is then equal to:

$$P_{OUT(BCM)} = \frac{1}{2} \cdot L_p \cdot I_{P(BCM)}^{\ 2} \cdot F_{SW} \cdot \eta \quad \text{(eq. 7)}$$

From which we can extract I_P:

$$I_{P(BCM)} = \sqrt{\frac{2 \cdot P_{OUT(BCM)}}{L_p \cdot F_{SW} \cdot \eta}} \quad \text{(eq. 8)}$$

Replacing I_P in equation 6 using equation 8, we obtain a way of calculating the primary inductance L_P, dependent on the output power $P_{out(BCM)}$ at which the application transitions from DCM to CCM:

$$L_p = \frac{\eta \cdot V_{IN(dc)}^{\ 2} \cdot N^2 \cdot (V_{OUT} + V_F)^2}{2 \cdot F_{SW} \cdot P_{OUT(BCM)} \cdot (V_{IN(dc)} + N \cdot (V_{OUT} + V_F))^2} \quad \text{(eq. 9)}$$

Solving for an efficiency of 87 %, a transition output power of 32 W and an input voltage of 100 V, we obtain L_P = 916 μH.

We will choose 1 mH, as it will further reduce the peak current, and give us a nice round number to ease up the rest of the calculations. With 1 mH and 100 V, the adapter will transition from DCM to CCM at 29.3 W at 100 V.

Let us now calculate $I_{P(max)}$, for an output power of 80 W. The converter is now running in CCM, and the current in the inductor doesn't go to 0 at the end of each cycle, as shown in Figure 6.

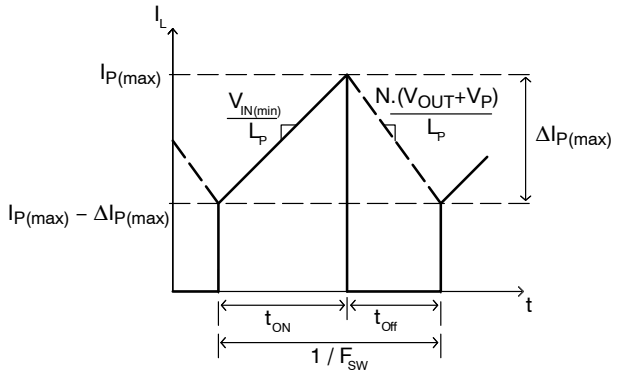

Figure 6. Inductor Current in CCM

$$P_{OUT(max)} = \left(\frac{1}{2} \cdot L_p \cdot I_{P(max)}{}^2 - \frac{1}{2} \cdot L_p \cdot (I_{P(max)} - \Delta I_{P(max)})^2\right) \cdot F_{SW} \cdot \eta \quad \text{(eq. 10)}$$

From it we can calculate I_P:

$$I_{P(max)} = \frac{P_{OUT(max)}}{\Delta I_{P(max)} \cdot L_p \cdot F_{SW} \cdot \eta} + \frac{\Delta I_{P(max)}}{2} \quad \text{(eq. 11)}$$

From Figure 6, we can also define ΔI_P as:

$$\Delta I_{P(max)} = \frac{V_{IN(dc)}}{L_P} \cdot \frac{D_{MAX}}{F_{SW}} \quad \text{(eq. 12)}$$

With $D_{MAX} = \dfrac{t_{ON(max)}}{t_{ON(max)} + t_{OFF(max)}} = \dfrac{\frac{L_p \cdot \Delta I_{P(max)}}{V_{IN(min)}}}{\frac{L_p \cdot \Delta I_{P(max)}}{V_{IN(min)}} + \frac{L_p \cdot \Delta I_{P(max)}}{N \cdot (V_{OUT} \cdot V_F)}}$, that simplifies into $D_{MAX} = \dfrac{N \cdot (V_{OUT} + V_F)}{V_{IN(min)} + N \cdot (V_{OUT} + V_F)}$ (eq. 13)

Using equations 12 and 13 we can rewrite equation 11 as follows:

$$I_{P(max)} = \frac{P_{OUT(max)} \cdot (V_{IN(min)} + N \cdot (V_{OUT} + V_F))}{N \cdot V_{IN(min)} \cdot (V_{OUT} + V_F) \cdot \eta} + \frac{N \cdot V_{IN(min)} \cdot (V_{OUT} + V_F)}{2 \cdot L_p \cdot F_{SW} \cdot (V_{IN(min)} + N \cdot (V_{OUT} + V_F))} \quad \text{(eq. 14)}$$

Solving for the maximum power of 80 W at the minimum voltage of 100 V, we find that the maximum peak current is $I_{P(max)} = 1.90$ A, with $\Delta I_{P(max)} = 1.02$ A and $D_{MAX} = 66$ %.

Sense Resistor

The sense resistor R_S is easily calculated from the $I_{P(max)}$ value, knowing the threshold of the current sense comparator.

This time the power equation is different, since only the energy corresponding to the current variation is transferred to the secondary.

$$R_S = \frac{V_{ILIM(min)}}{I_{P(max)}} \quad \text{(eq. 15)}$$

Solving with $V_{ILIM(min)} = 0.665$ V and $I_{P(max)} = 1.9$ A, it gives $R_S = 0.35$ Ω. Knowing that the previously calculated value for $I_{P(max)}$ didn't take into account any tolerances, we will choose 0.33 Ω for the sense resistor.

In the final schematic, the designator for the sense resistor is R7.

Overpower Compensation Resistor

There is a propagation delay from when the current reaches the maximum programmed value to when the MOSFET actually turns off: it is the sum of the internal propagation delay of the controller (speed of the CS comparator, the internal logic and the output driver), and the external propagation delay (any resistor between the DRV pin and the MOSFET's gate, and the turn-off time of the MOSFET). This delay is fairly constant, but the slope of the current is proportional to the input voltage, as shown on Figure 7. As a result the actual maximum power that the application can deliver increases with the input voltage.

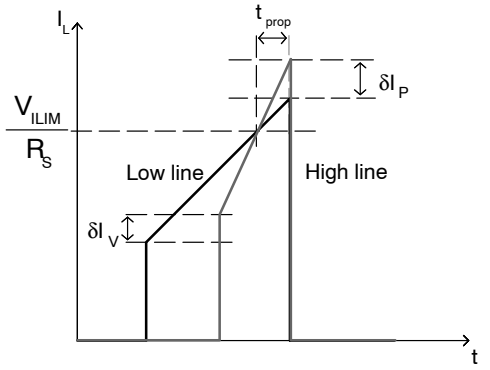

Figure 7. Delay from Max Peak Current to Turn-off

From Figure 7, we can calculate the peak current increase between two different input voltages:

$$\delta I_P = \frac{(V_{IN2} - V_{IN1}) \cdot t_{Prop}}{L_P} \qquad \text{(eq. 16)}$$

In our case we are interested in $\delta I_{P(max)}$, the peak current increase from the lowest to the highest input voltage. However, this equation requires the total propagation delay, which we can't know at this moment. We will thus use an estimated value of 1 μs, keeping in mind that we may have to optimize this value later if the propagation delay turns out to be significantly different than the assumed value. Solving for $V_{IN(min)}$ = 100 V and $V_{IN(max)}$ = 375 V, we obtain a $\delta I_{P(max)}$ of 275 mA.

To compensate for that, the maximum peak current threshold must be reduced when the input voltage increases. This is achieved in the NCP1237 by sourcing a current proportional to V_{IN} out of the CS pin: inserting a compensation resistor R_{OPC} between the CS pin and the sense resistor R_S adds an offset to the current sense signal, which is equivalent to reducing the peak current.

Since the compensation current is 0 at low line, we just need to estimate what offset is needed at high line to be able to calculate R_{OPC}.

$$R_{OPC} = \frac{R_S \cdot \delta I_{P(max)}}{I_{OPC}} \qquad \text{(eq. 17)}$$

That leads to a compensation resistor of 800 Ω.

However, when the primary current is close to the maximum, the converter is running in CCM, not in DCM. This means that even if the peak currents are the same at low and high line, the minimum current aren't: there is a difference δI_V, as shown on Figure 7. Therefore the maximum powers aren't the same in both cases, according to Equation 10.

We will need an extra offset to compensate for this effect. It can be calculated, but it involves a complicated equation, since we want to compensate for the difference in the valleys of the primary currents by offsetting the peak. This is not easy, so we will rather increase the value for the compensation resistor, and we will adjust it if needed after testing the board.

We choose to increase R_{OPC} by 50%, i.e. R_{OPC} = 1.2 kΩ.

In the final schematic, the designator for the overpower compensation resistor is R4.

Slope Compensation

Because the application runs in CCM at a duty ratio higher than 50% at low input voltage, slope compensation is needed to prevent sub-harmonic oscillations. Thankfully the NCP1237 already includes internal slope compensation, so there is nothing to adjust.

Overvoltage Protection

Building an Overvoltage Protection (OVP) using the latch pin of the NCP1237 is very simple. All is needed is to connect a Zener diode between the voltage to be sensed and the pin. No additional resistor is required, as the current is internally limited.

In our application, we choose to connect a 17 V zener diode between the supply voltage V_{CC} and the Latch pin: as soon as the output voltage increases, the supply voltage increases as well, and the Latch pin follows. When the Latch pin voltage reaches 2.5 V, corresponding to 19.5 V on the V_{CC} capacitor, the OVP is triggered, and the controller gets latched off.

In the final schematic, the designator for the OVP zener diode is ZD1.

Output Regulation and Feedback Loop

The feedback loop is classically built around a TL431, which provides reliable regulation with few components and at a low cost. We want to minimize the bias current in the resistor divider that senses the output voltage, as the losses associated with this bias current can be significant in no-load condition.

Let us choose a 20 kΩ bottom resistor R_{bottom}, which limits the bias current to 125 μA since the reference voltage of the TL431 V_{ref} is 2.495 V.

The upper resistor can be calculated from equation 18:

$$R_{upper} = R_{bottom} \cdot \frac{V_{OUT} - V_{REF}}{V_{REF}} \qquad \text{(eq. 18)}$$

Solving for V_{OUT} = 32 V, we obtain a value of 236.5 kΩ. We will choose a normalized value of R_{upper} = 237 kΩ.

In the final schematic, the designator for the upper resistor is R31, and R32 for the bottom resistor.

Final Schematic

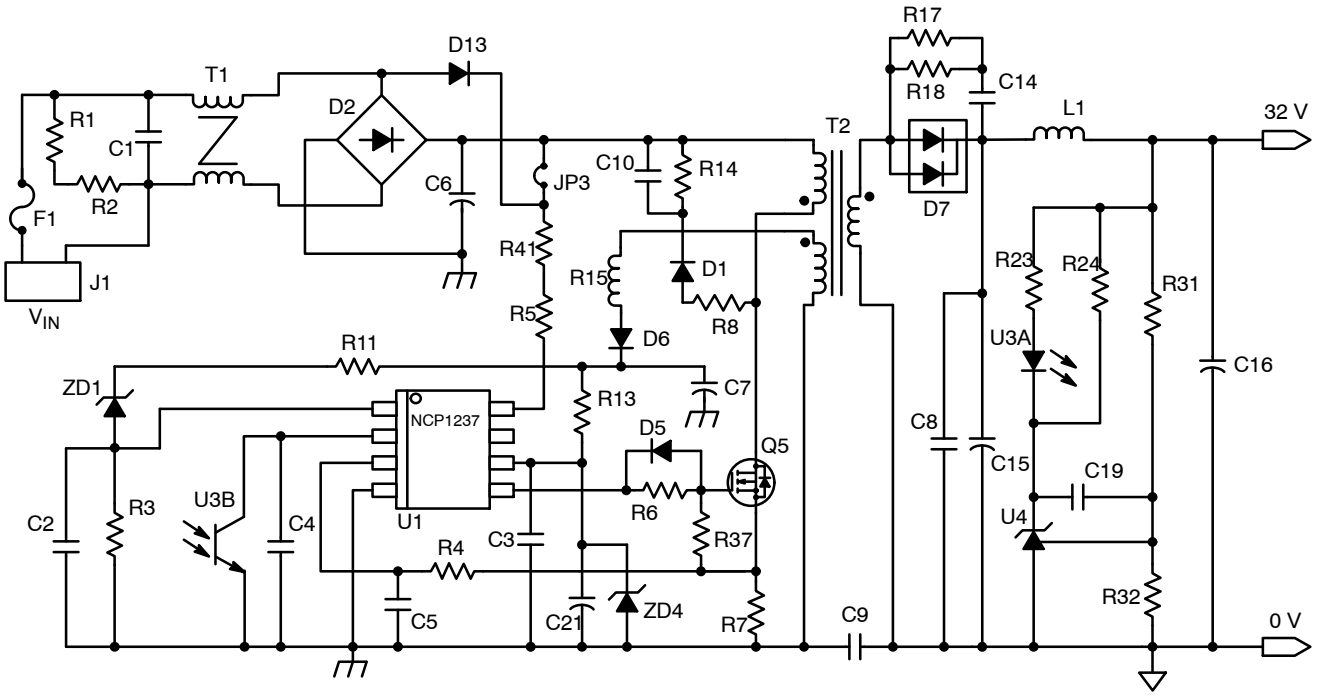

Figure 8. Final Schematic of the Printer Evaluation Board

Bill of Materials

Table 2: Bill of Materials of the Printer Evaluation Board

Reference	Value	Manufacturer	Description	Part number
C1	330 nF / 250 Vac	Kemet / Evox-Rifa	X2 film capacitor – 8.5x18 mm	PHE840MX6330MB11
C2, C4	1 nF / 25 V	Vishay	0805 ceramic	
C3	100 nF / 50 V	Vishay	0805 ceramic	
C5, C21	open	–	–	
C6	100 μF / 400 V	United Chemicon	Electrolytic capacitor – 18x32 mm	EKXG401ELL101MMN3S
C7	47 μF / 50 V	United Chemicon	Electrolytic capacitor	ECA-1HM470
C8	100 nF / 50 V	Vishay	0805 ceramic	
C9	2.2 nF / 250 Vac	Kemet / Evox-Rifa	Y2 film capacitor	PHE850EA4220MA01R17
C10	6.8 nF / 630 V	TDK	mid-voltage ceramic through-hole	FK20COG2J682J
C14	1.0 nF / 250V	TDK	mid-voltage ceramic through-hole	FK24C0G2E102J
C15	470 μF / 50 V	United Chemicon	Electrolytic capacitor	ECA-1HM471
C16	220 μF / 50 V	United Chemicon	Electrolytic capacitor	ECA-1HM221
C19	10 nF / 50 V	Vishay	1206 ceramic	
D1	MUR1100	ON Semiconductor	1 A / 1 kV through-hole rectifier	MUR1100EG
D2	W06G	Vishay	600 V through-hole bridge rectifier	W06G-E4/51
D5, D6	MMSD4148	ON Semiconductor	SOD123 commutation diode	MMSD4148T1G
D7	MBRF20H150	ON Semiconductor	TO220 fullpack 20 A / 150 V Schottky	MBRF20H150CTG
D13	1N4007	ON Semiconductor	1 A / 1000 V through-hole rectifier	1N4007G
F1	2.0 A	Littelfuse	392 series radial fuse	3921200
HS1, HS2	Heatsink	custom	Heatsink - 30x20x1.5 mm	
J1	770W-X2/10	Qualtek	AC connector	770W-X2/10
JP3	open	–	Jumper	
L1	4.7 μH / 4.2 A	Coilcraft	Power inductor	RFB0807-4R7L
Q5	4N80 fullpack	Infineon	4 A / 800 V MOSFET - TO220 fullpack	SPA04N80C3
R1, R2	1.5 MΩ / 200 V	Vishay	1206	
R3	14 kΩ	Vishay	0805	
R4	1.2 kΩ	Vishay	0805	
R5, R41	1 kΩ / 200 V	Vishay	1206	
R6	10 Ω	Vishay	1206	
R7	0.33 Ω		2512	
R8	47 Ω / 0.5 W		Axial through-hole	
R11	10 Ω	Vishay	1206	
R13	0 Ω	Vishay	1206	
R14	200 kΩ / 0.5 W		Axial through-hole	
R15	2.2 μH	Vishay	inductor 1206	ILSB-1206ER2R2K
R17, R18	200 Ω / 200 V	Vishay	1206	
R23	10 kΩ	Vishay	1206	
R24	3.3 kΩ	Vishay	1206	
R31	237 kΩ / 1%	Vishay	0805	
R32	20 kΩ / 1%	Vishay	0805	
R37	10 kΩ	Vishay	0805	
T1	2 x 10 mH	Epcos	Vertical common-mode choke	B82732R2142B030
T2	TO09161	Ice Components	Custom	TO09161
U1	NCP1237A 65kHz	ON Semiconductor	Fixed-frequency CM controller	NCP1237AD65DR2G
U3	PS2561	CEL-NEC	Optocoupler	PS2561-1-L-A
U4	TL431B	ON Semiconductor	Adj. Voltage Reference - TO-92	TL431B
ZD1	17 V	ON Semiconductor	SOD123 Zener diode	MMSZ5247BT1G
ZD4	open	–	–	

Board Layout

The demonstration board is built using a single sided FR4 board. Through hole components are placed on the top layer and surface mount components on the bottom layer. The board is constructed using 2 oz copper.

During the layout process care was taken to minimize high current loops area and keep sensitive nodes away from noisy nodes.

Figures 9, 10 and 11 show the top and bottom layers of the PC board.

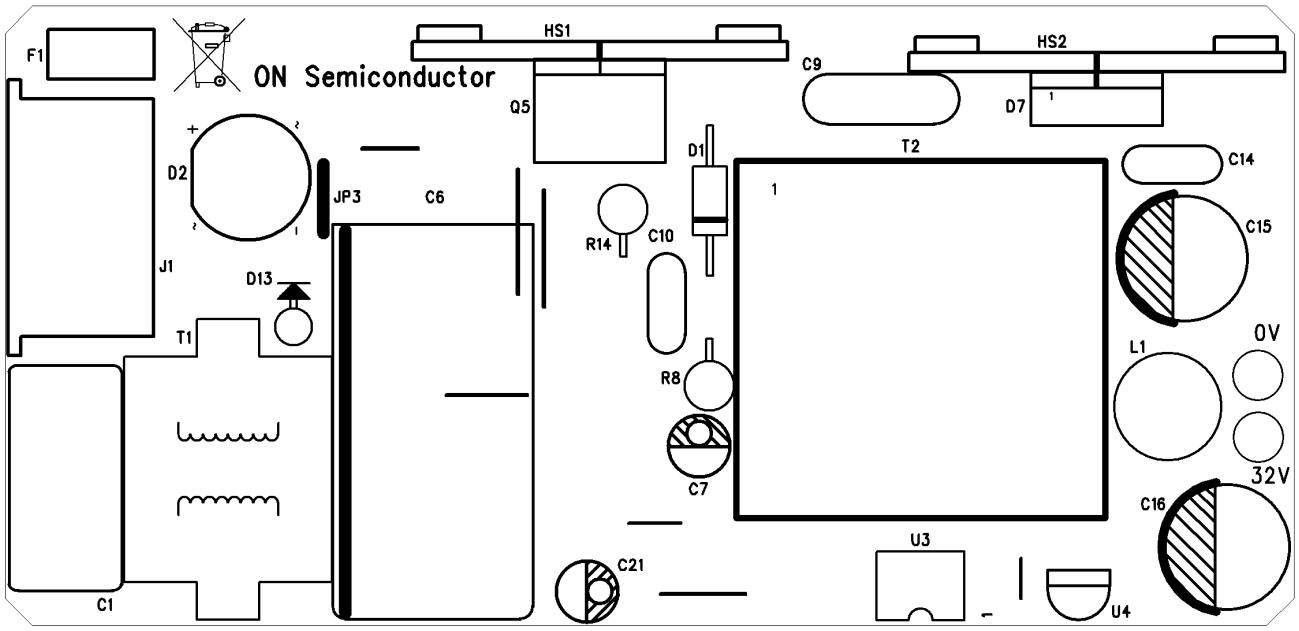

Figure 9. Top Layer Silkscreen

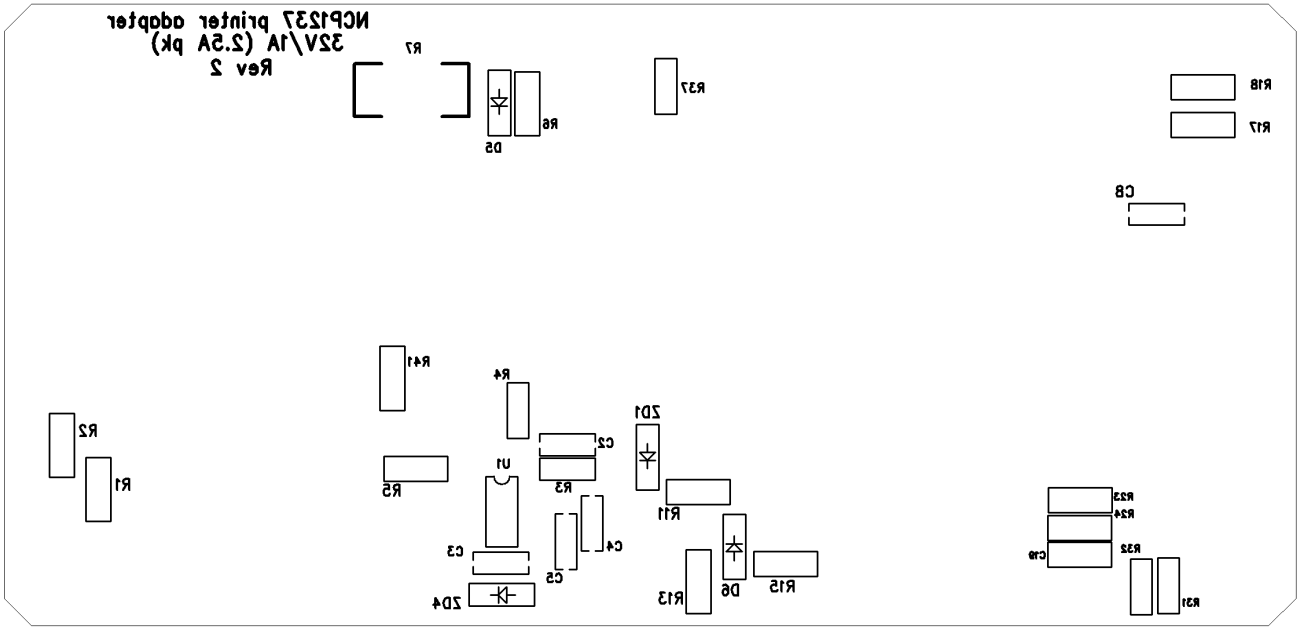

Figure 10. Bottom Layer Silkscreen

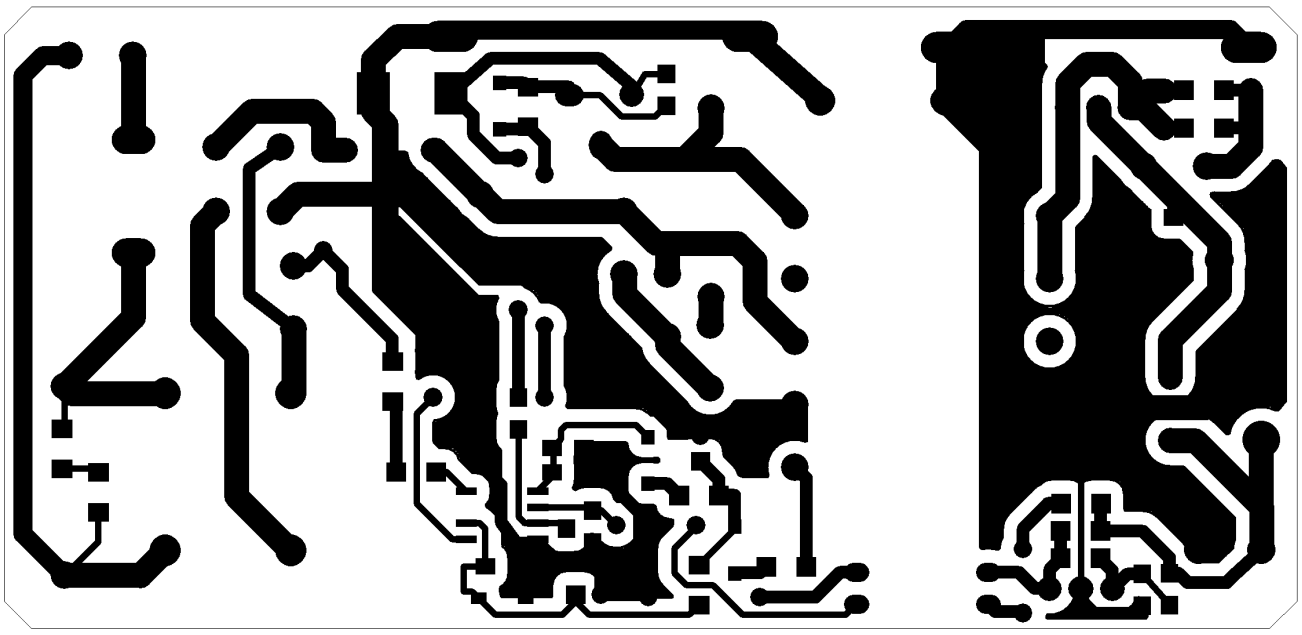

Figure 11. Bottom Layer Copper

Board Performance

Efficiency

All input power measurements were performed using a WT210 power meter from Yokogawa, in Wh mode over a period of 6 minutes per measurement. All output measurements were performed at the end of a 0.6 m long cable.

Energy Star Measurements:

	115 Vac	230 Vac	EPS 2.0 Compliance
32 W (100 %)	88.9 %	89.7 %	PASS
24 W (75 %)	88.7 %	88.9 %	
16 W (50 %)	88.1 %	88.1 %	
8 W (25 %)	86.7 %	86.3 %	
Average	88.1 %	88.3 %	PASS
No load input power	92 mW	133 mW	PASS

Additional Efficiency Measurements:

	115 Vac	230 Vac
3.2 W	82.1 %	79.7 %
1.89 W	78.0 %	76.0 %
0.93 W	72.6 %	69.9 %
0.48 W	65.4 %	62.1 %

Oscilloscope Shots

Figures 12 to 29 show typical waveforms and demonstrate the compliance to the specification.

Figures 12 and 13: the adapter operates in DCM below 32 W at low and high line
Figures 14 and 15: the frequency is reduced in light load condition
Figures 16 to 19: the controller enters skip mode in no load condition
Figures 20 to 23: the ripple on the output is less than 200 mV in all conditions
Figures 24 and 25: the adapter can deliver 2.5 A during 120 ms
Figures 26 and 27: the output stays within ±500 mV during no load to full load load steps
Figure 28 and 29: no overshoot appears on the output during start-up

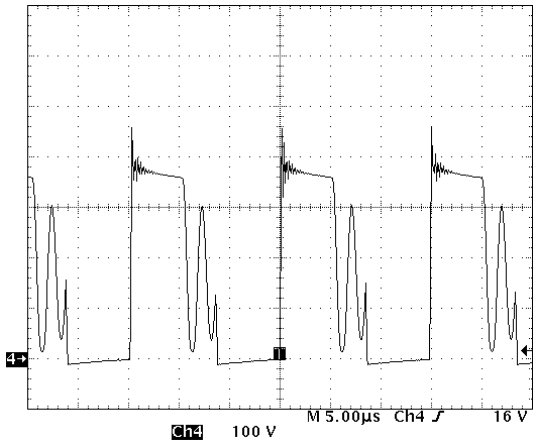

Figure 12. Drain Voltage in Full Load Condition (1 A at 115 Vac)

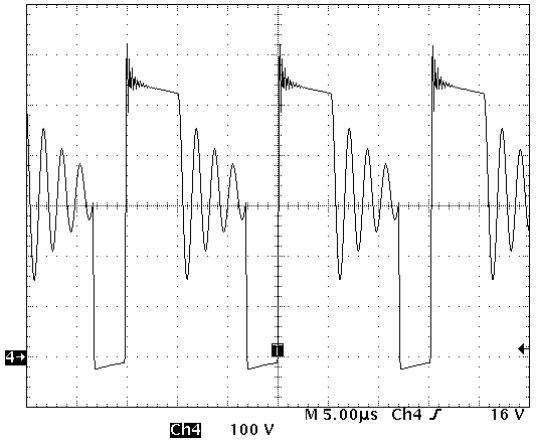

Figure 13. Drain Voltage in Full Load Condition (1 A at 230 Vac)

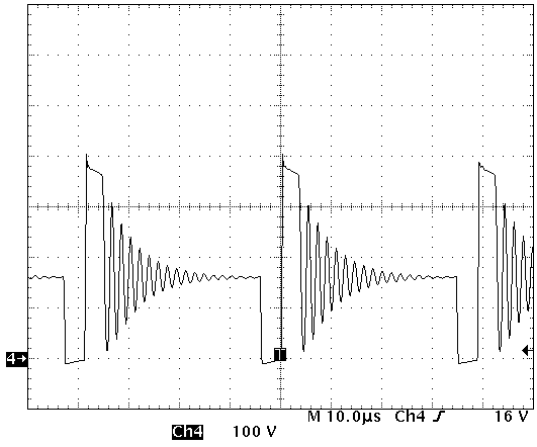

Figure 14. Drain Voltage in Light Load Condition (150 mA at 115 Vac)

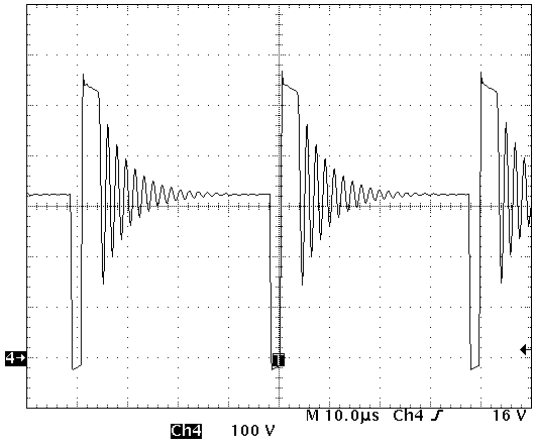

Figure 15. Drain Voltage in Light Load Condition (150 mA at 230 Vac)

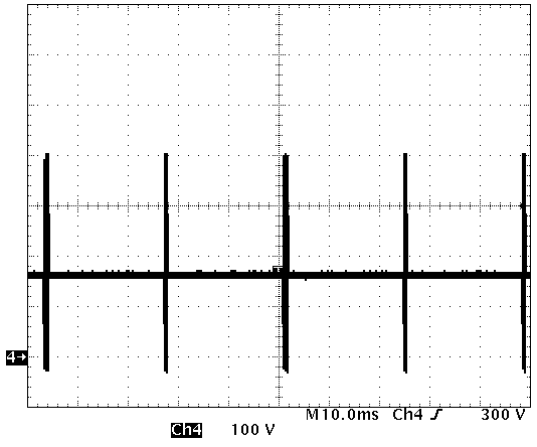

Figure 16. Skip Mode Observed on the Drain Signal in No Load Condition at 115 Vac

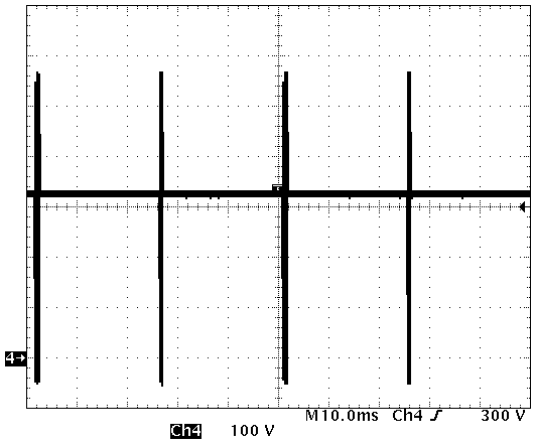

Figure 17. Skip Mode Observed on the Drain Signal in No Load Condition at 230 Vac

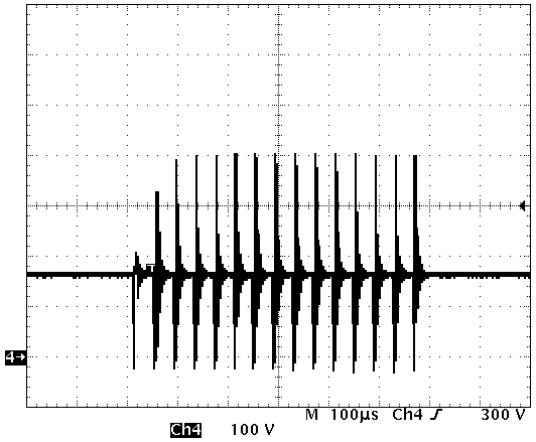

Figure 18. Zoom on the Drain Voltage in No Load Condition at 115 Vac

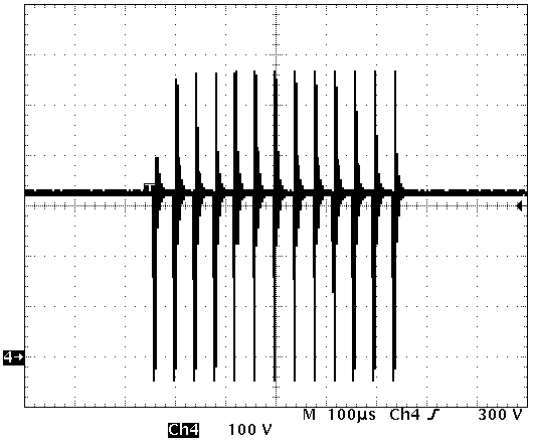

Figure 19. Zoom on the Drain Voltage in No Load Condition at 230 Vac

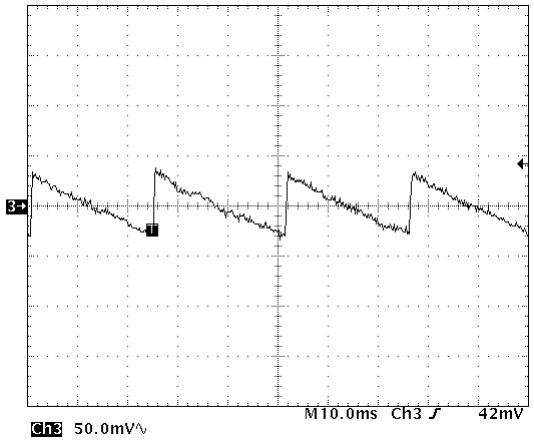

Figure 20. Output Voltage Ripple in No Load Condition at 115 Vac

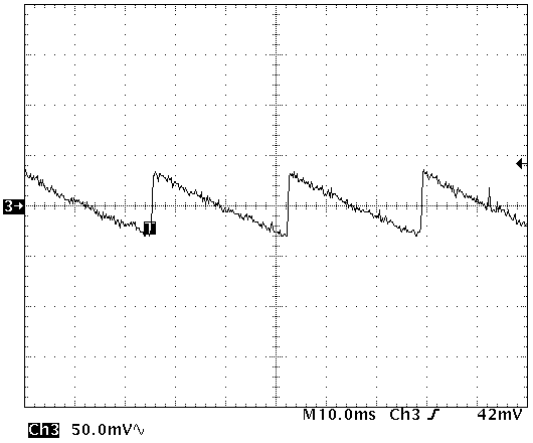

Figure 21. Output Voltage Ripple in No Load Condition at 230 Vac

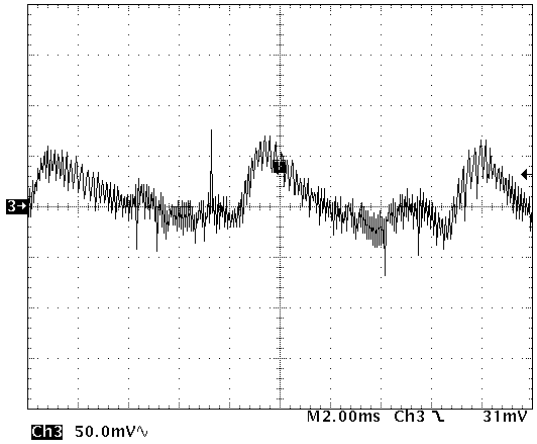

Figure 22. Output Voltage Ripple in Full Load Condition (1 A at 115 Vac)

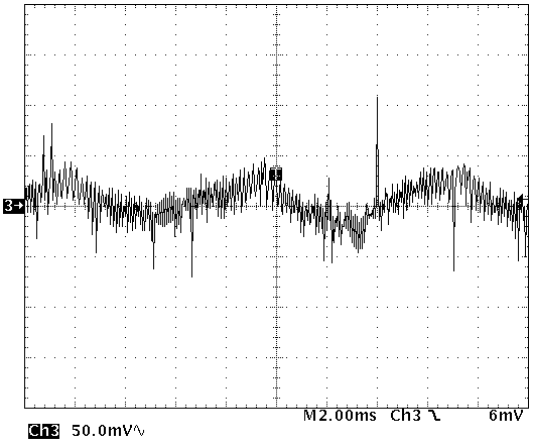

Figure 23. Output Voltage Ripple in Full Load Condition (1 A at 230 Vac)

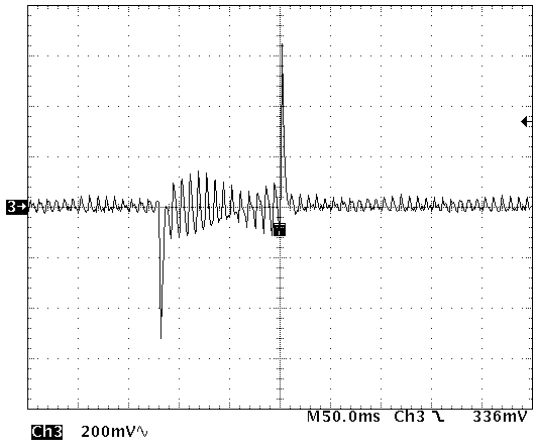

Figure 24. Output Voltage during Peak Power (1 A to 2.5 A to 1 A at 115 Vac)

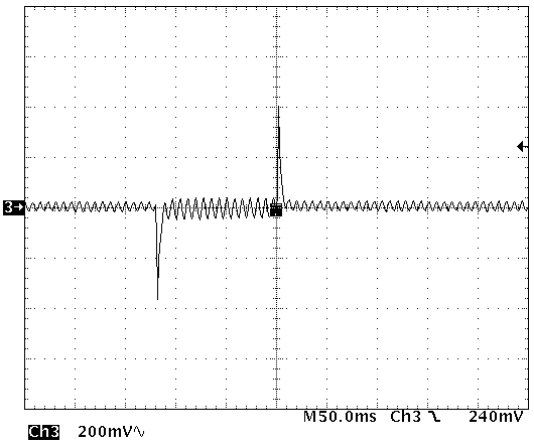

Figure 25. Output Voltage during Peak Power (1 A to 2.5 A to 1 A at 230 Vac)

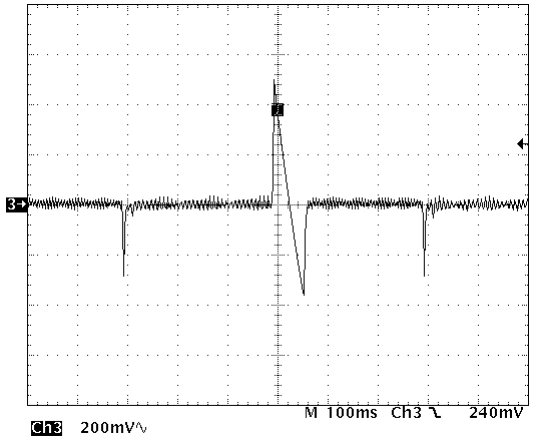

Figure 26. Output Voltage during a Load Step (1 A to 0 A to 1 A at 115 Vac)

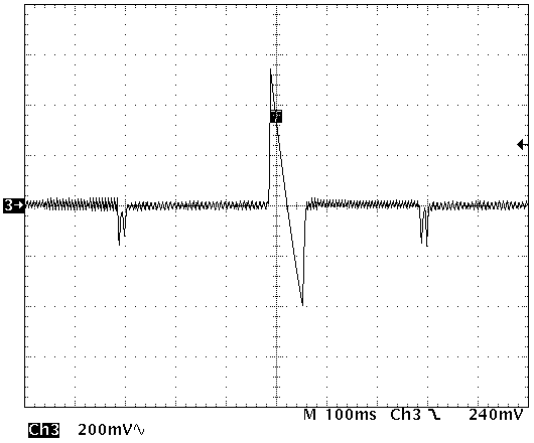

Figure 27. Output Voltage during a Load Step (1 A to 0 A to 1 A at 230 Vac)

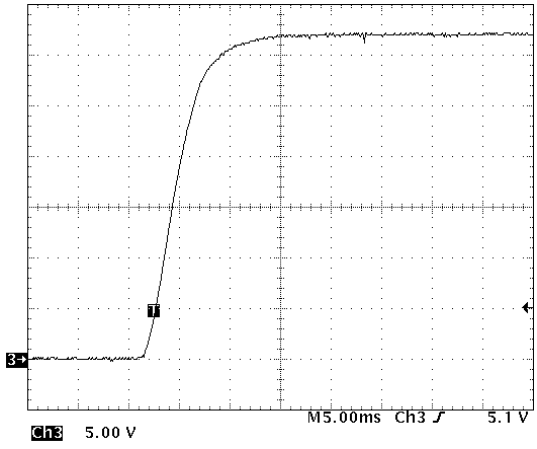

Figure 28. Output Voltage during Start-up (1 A at 115 Vac)

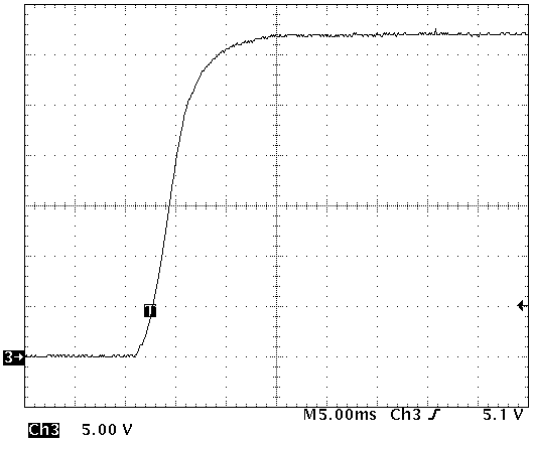

Figure 29. Output Voltage during Start-up (1 A at 230 Vac)

Disclaimer: This demonstration board is designed to demonstrate the features and flexibility of the NCP1237. This design is a guideline only and does not guarantee performance for any manufacturing or production purposes.

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