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Minimizing the Temperature Dependence of Digital Potentiometers (POTs)

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APPLICATION NOTE

Abstract

The digital POT has two temperature dependent parameters, the TC of the end-to-end resistance R_{POT} and the ratiometric TC. The temperature dependence of the parameters of an analog circuit using a digital POT is reduced if the performance of the circuit is shifted from the TC of the end-to-end resistance of the pot to the ratiometric TC.

The temperature dependence of electronic products can be reduced using a number of different approaches. One approach, for those products where it is possible, is to use a closed-loop, feedback system to calibrate the product's electronics before any measurement or signal processing activity is initiated. The calibration procedure can correct for any internal changes due to temperature or other environmental factors. A second approach is to use low temperature dependent components at the circuits' level.

A third approach is to use a circuit topology whose performance with temperature is shifted from high TC parameters to low TC parameters. This application note will look at the latter two approaches.

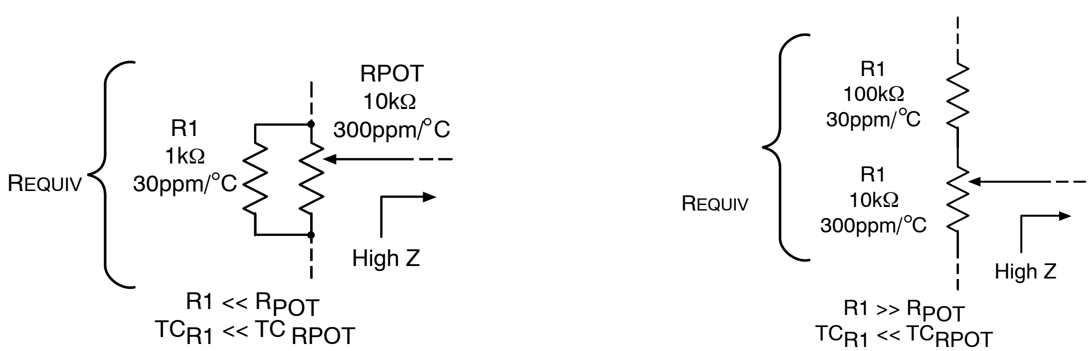
- **Adding Resistors in Parallel and in Series**
- **Circuit Topologies**
- Inverting Amplifiers
- Voltage Dividers
- I to V Convertors
- Comparator Circuits
- Square Wave Oscillator

ADDING RESISTORS IN PARALLEL AND IN SERIES

For certain applications, the temperature dependence of the pot can be minimized by adding a low TC resistor in parallel or in series with the end-to-end resistance. The resistor added in these combination circuits can be designed to mask out the effect of the high TC of the pot. If, in Figure 1, R_1 is chosen to be much less than R_{POT} in the parallel circuit and much greater than R_{POT} in the series circuit AND R_1 has a low TC compared to the TC of R_{POT}, then the TC of the equivalent resistance will approach that of R_1. For the parallel case, the wiper must see a high impedance in the application. For the sample values listed in the parallel circuit, the TCs are added statistically providing:

$$TC_{REQUIV} = \frac{1}{10\ k\Omega + 1\ k\Omega} \sqrt{\left\{(10\ k\Omega)(.00003)\right\}^2 + \left\{(1\ k\Omega)(.0003)\right\}^2}$$

$$TC_{REQUIV} = 38.6\ ppm/^{\circ}C$$



(a) Parallel

(b) Series

Figure 1. Adding Resistors in Parallel and in Series

For the conditions stated, the TC of the parallel combination (38.6 ppm/°C) approaches that of resistor R_1 (30 ppm/°C). This value can only used to illustrate the idea or concept of shifting the temperature dependence of the circuit from the potentiometer to an external fixed resistor. The above calculation assumes normal distributions and guaranteed values which are not the case for the TC of R_{POT}.

The role and effect of R_1 is the same for the dual series circuit. For the sample values listed in the series circuit, the TCs are added statistically providing:

$$TC_{REQUIV} = \frac{1}{10\ k\Omega + 100\ k\Omega}\sqrt{\{(10\ k\Omega)(.0003)\}^2 + \{(100\ k\Omega)(.00003)\}^2}$$

$$TC_{REQUIV} = 38.6\ ppm/^{\circ}C$$

CIRCUIT TOPOLOGIES

The nominal temperature coefficient of the end-to-end resistance of the digital POT is 300 ppm/°C. It is not a guaranteed parameter. The ratiometric temperature coefficient of the digital POT is 20 ppm/°C and is a guaranteed parameter. The temperature dependence of the parameter of an analog circuit is frequently related to the temperature dependence of the potentiometer and is minimized if the performance of the circuit is shifted to the ratiometric TC rather than the TC of R_{POT}. This Application Note takes a number of basic analog circuits and shows two versions or topologies of each, one which depends on the TC of R_{POT} and the other which depends on the ratiometric TC. In general, the ratiometric TC is applicable when the pot is used as a three terminal device. For temperature dependence reasons and others, the three terminal configuration of the potentiometer is superior to the two terminal version. The following circuits are discussed; amplifiers, voltage dividers, I to V convertors, comparator circuits, and a square wave oscillator. The principles illustrated in these circuits apply to others as well.

INVERTING AMPLIFIERS

The inverting amplifier circuits of Figure 2 represent two different ways of using a digital POT to program the circuit's voltage gain. The circuit of Figure 2a uses the digital POT as a two-terminal, variable resistance device while the Figure 2b version uses the digital POT as a three-terminal, resistive divider device. The voltage gain for Figure 2a is given as:

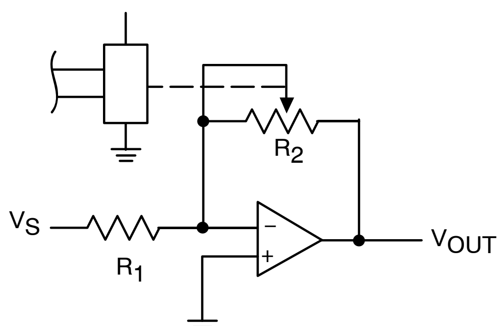
$$\frac{V_{OUT}}{V_S} = G = -\frac{R_2}{R_1} = -\frac{(p)R_{POT}}{R_1},\ \text{for } 0 \le p \le 1$$

where p is a dimensionless number and represents the proportional wiper setting from one end of the pot (0) to the other end (1). Because the voltage gain is directly proportional to R_{POT}, so is the temperature dependence. The voltage gain for Figure 2b is

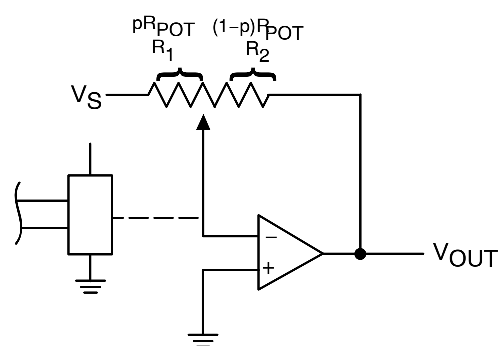
$$\frac{V_{OUT}}{V_S} = G = -\frac{R_2}{R_1} = -\frac{(1-p)R_{POT}}{pR_{POT}} = -\frac{(1-p)}{p},\ \text{for } 0 \le p \le 1$$

The temperature dependence of the gain is independent of R_{POT} but dependent on the position of the wiper whose temperature dependence is a function of the ratiometric TC. So also is the voltage gain. This circuit topology, compared to the first, has two other notable features (1) more accurate gain and (2) a pseudo-logarithmic gain behavior. The accuracy of the gain of Figure 2a depends on the accuracy of R_{POT} which is ±15%. The accuracy of the gain of Figure 2b depends on the accuracy of the resistive divider of the pot which is governed by its linearity or one LSB and is 1% for a 100 tap pot.

The same principles apply to the noninverting versions of the amplifier circuits.



(a) High Temperature Dependance



(b) Low Temperature Dependance

Figure 2. Inverting Amplifiers

VOLTAGE DIVIDERS

The output voltage for the voltage divider circuit in Figure 3a is

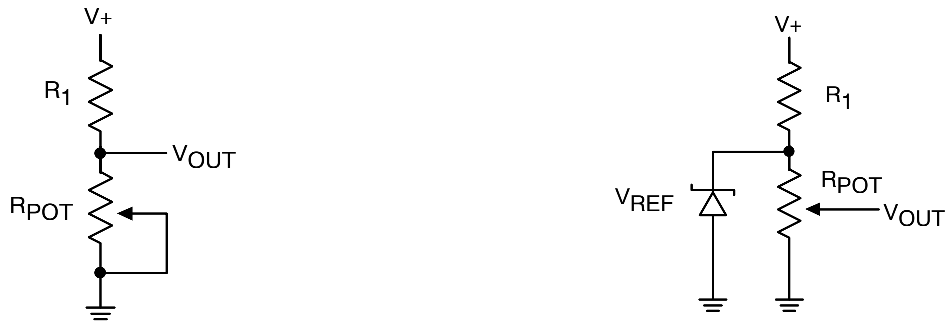
$$V_{OUT} = \frac{(p)R_{POT}}{R_1 + pR_{POT}}, \text{ for } 0 \le p \le 1$$

The output voltage for the circuit is proportional to the end-to-end resistance R_{POT} and hence is proportional to its temperature dependence.

If a low TC, voltage reference device, V_{REF}, is placed in parallel with the end-to-end resistance of the pot as shown in Figure 3b, the circuit's output voltage is:

$$V_{OUT} = pV_{REF}, \text{ for } 0 \le p \le 1$$

The temperature dependence of the output voltage will depend on the ratiometric TC of the pot. Although the high TC of R_{POT} changes the end-to-end resistance and hence the current through the potentiometer, the voltages of the resistive divider remain relatively constant.



(a) High Temperature Dependance **(b) Low Temperature Dependance**

Figure 3. Voltage Dividers

CURRENT TO VOLTAGE CONVERTORS

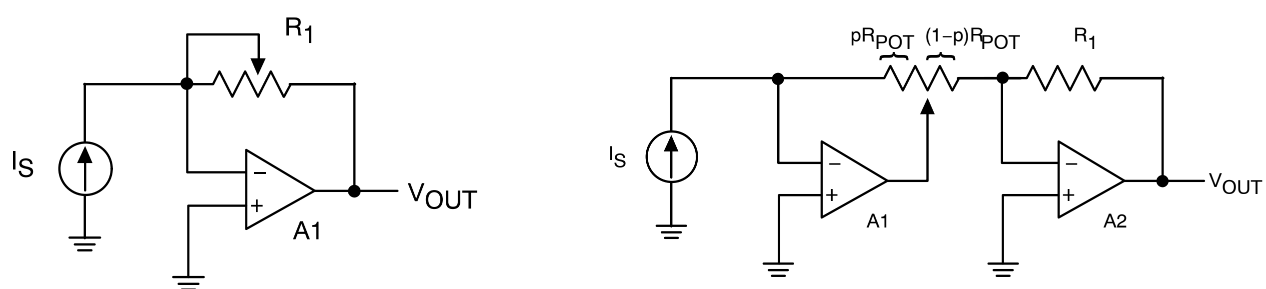
The output voltage for the I to V convertor in Figure 4a is

$$V_{OUT} = -I_S\ R_1 = -I_S\ p\ R_{POT}, \text{ for } 0 \le p \le 1$$

This basic circuit has many limitations including the temperature dependence on the potentiometer's TC of R_{POT}. The output voltage of the convertor in Figure 4b is

$$V_{OUT} = -I_S \frac{p}{(1-p)} R_1, \text{ for } 0 \le p \le 1$$

This version of the I to V convertor not only provides for a wide range of trans impedance gain but also has a temperature dependence related to the ratiometric TC of the pot.



(a) Basic **(b) Advanced**

Figure 4. I to V Convertors

COMPARATOR CIRCUITS

The performance of the two comparator circuits in Figure 5 is independent of the end to end resistance of the potentiometer. In the level detector circuit of Figure 5a, the signal source V_S and the reference voltage V_{REF} are summed through the potentiometer. The high-low status of the detector's output is determined by the input voltage VIN. For the circuit,

$$V_{IN} = (1 - p)V_S + p\,V_{REF}\text{, for } 0 \le p \le 1$$

The circuit in Figure 5b is a single-supply version of a programmable Schmitt Trigger or a comparator with hysterisis. The lower (V_{LL}) and upper (V_{UL}) limits of the hysterisis characteristic are a function of the relative setting of the potentiometer's wiper and are given as:

$$V_{LL} = (1 - p)\ 2.5\text{ V} \quad \text{and} \quad V_{UL} = 2.5\text{ V} + (p)2.5\text{ V}$$

where p is a dimensionless number from 0 to 1. The characteristic's lower limit can be programmed from 0 V to 2.5 V and the upper limit can be programmed from 2.5 V to 5 V. The two limits are complementary and relatively stable with temperature.

Figure 5. Comparator Circuits

SQUARE WAVE OSCILLATOR (555)

The 555 oscillator in Figure 6 has two key parameters, frequency of oscillation and duty cycle. For the basic circuit where $R_1 = R_2 = 0$,

$$f_{OSC} = \frac{1.44}{R_{POT}(2 - p)C}\text{, for } 0 \le p \le 1$$

and

$$DC = \frac{1}{(2 - p)}\text{, for } 0 \le p \le 1$$

The duty cycle is automatically independent of the pot's end-to-end resistance and is relatively temperature stable.

For applications where the temperature stability of the frequency of oscillation is critical, adding R_1 and R_2 reduces the dependence of the frequency of oscillation on R_{POT}. For this case,

$$f_{OSC} = \frac{1.44}{\left(R_1 + p\,R_{POT}\right) + 2\left(R_2 + (1 - p)\,R_{POT}\right)C}\text{, for } 0 \le p \le 1$$

The range of programmability of f_{OSC} is reduced by adding R_1 and R_2 but the values and temperature coefficients of R_1 and R_2 can be designed to dominate the parameter and its temperature dependence.

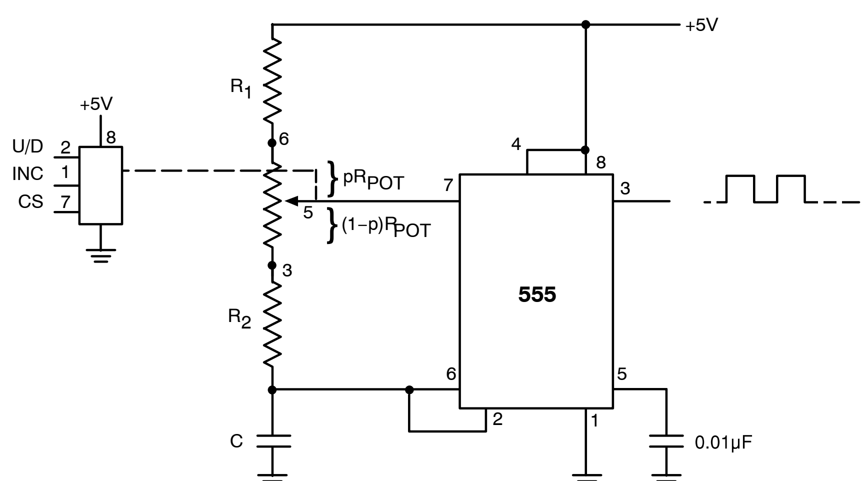


Figure 6. Square Wave Oscillator (555)

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