48 W, 24 V/7.5 V Universal Input AC-DC Printer Adapter Using the NCP1219

AND8393/D

Introduction

The NCP1219 is the newest part in the NCP12XX family of current−mode flyback controllers. The controller features dynamic self supply (DSS), eliminating the need for external startup circuitry, contributing to a cost effective, low parts count flyback controller design. The NCP1219 also includes a user programmable skip cycle threshold, reducing power dissipation at light loads and in standby mode. An externally provided latch signal delivered to the Skip/latch pin allows the realization of protection functionality.

The 48 W ac adapter demonstration board targets a printer adapter application with a 24 V output, reconfigurable to 7.25 V in standby mode selectable with an external signal. The use of DSS mode is demonstrated for low input voltages, while an auxiliary winding is used for higher input voltages to maintain standby power below 1 W. The NCP1219 demonstration board shows latched−mode protection function through the optional primary and secondary overvoltage protection circuits.

The demonstration board is designed as an off−line printer adapter power supply. The adapter operates across universal inputs, 85 Vac to 265 Vac (47 Hz – 63 Hz). The adapter supplies a regulated 24 V output. It can deliver a steady state 30 W output with transient capability of 48 W, as defined in Figure 1.

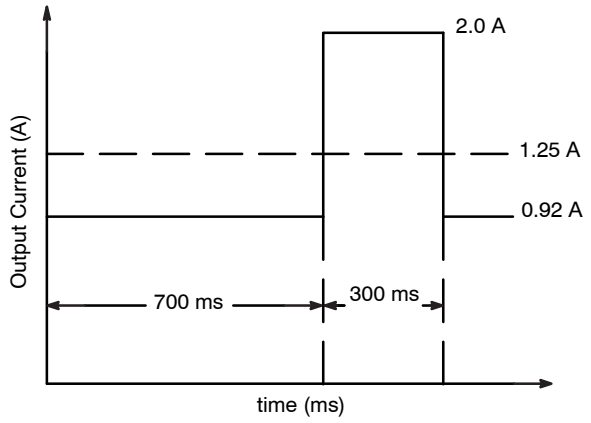

Figure 1. Transient Output Current Specification

The system has a low voltage standby mode enabled by pulling the MC node low. In standby mode the converter supplies 70 mA of standby current at 7.25 V while maintaining input power below 1 W. The system is self−contained, with the NCP1219 bias being provided by the bulk voltage through an internal startup circuit. The IC bias is provided by either DSS for low input voltages, or an auxiliary winding for higher input voltages. The specifications are summarized in Table 1.

Table 1. SUMMARY OF DEMONSTRATION BOARD SPECIFICATIONS

Requirement	Unit	Min	Max
Input Voltage	Vac	85	265
Line Frequency	Hz	47	63
Output Voltage	Vdc	23.8	24.2
Output Current	Adc	–	1.25 (2.0 transient peak)
Output Power	W	–	30 (48 transient peak)
Average Efficiency (EPA Energy Star 2.0 Compliance)	η_{avg}	83.5	–
Standby Voltage	Vdc	7	8
Standby Power	W	–	1
Output Ripple Voltage	mV	–	200
Output Voltage Under/Overshoot During Transient Load Step from 0.92 A to 2.0 A	mV	–	200

DESIGN PROCEDURE

The converter design procedure is divided into several steps:

- Power Component Selection
- Loop Stability Analysis and Compensation
- IC Supply Circuits
- External Protection Circuits
- Standby Reconfiguration Circuit

Throughout this application note, the minimum and maximum input voltages are referred as low and high line, respectively.

The demonstration board schematic is provided in Figure 2 for reference to component values throughout the design procedure.

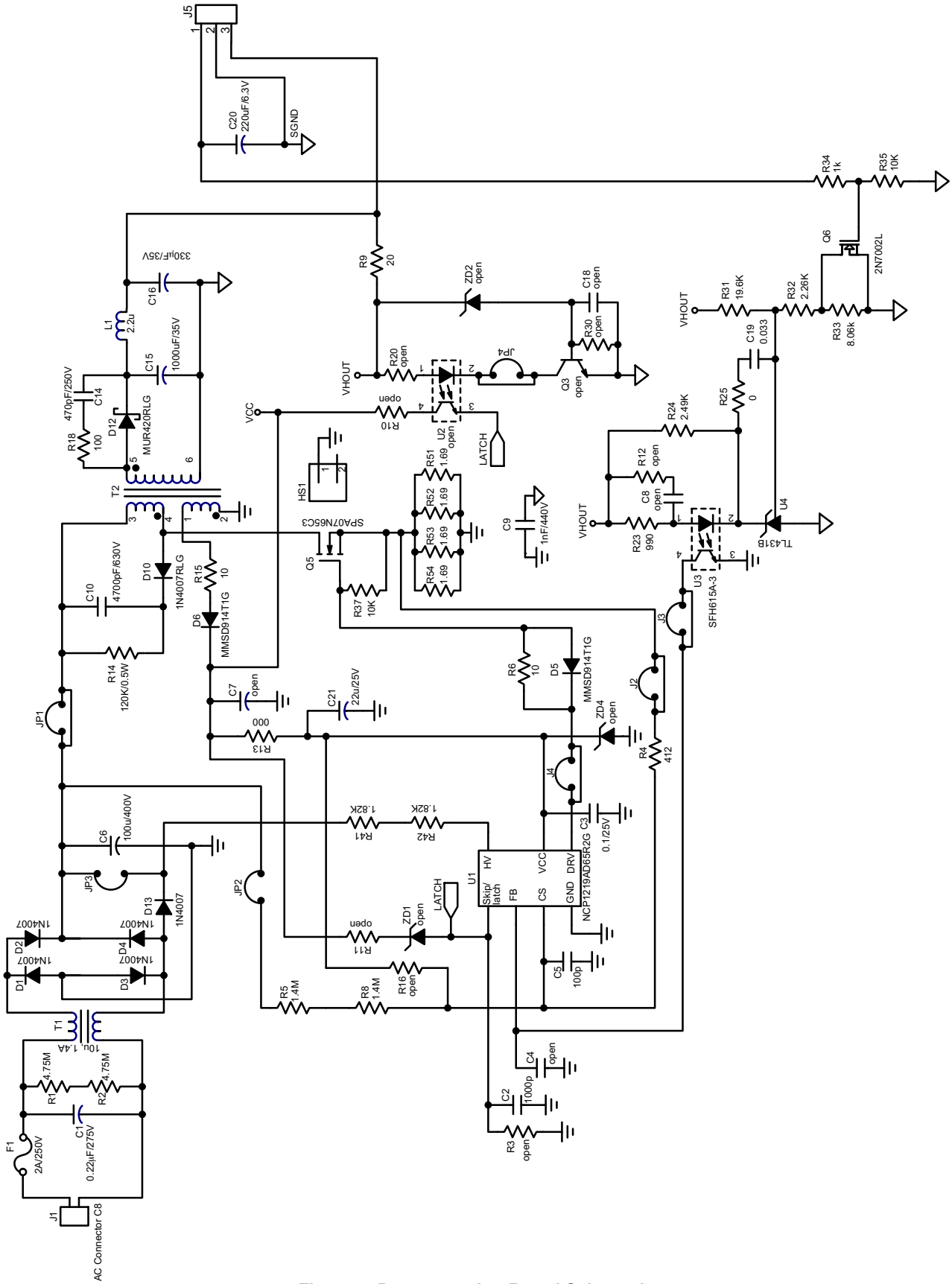

Figure 2. Demonstration Board Schematic

TRANSFORMER

The turns ratio, N, is chosen to minimize the voltage stresses placed on main switch, Q5, and the secondary diode, D12. N is calculated using Equation 1,

$$N = \frac{N_S}{N_P} = \frac{k_C \cdot \left(V_{out} + V_f\right)}{BV_{DSS} \cdot k_D - V_{OS} - V_{bulk(max)}} \quad \text{(eq. 1)}$$

where N_S is the number of turns on the secondary winding, N_P is the number of turns on the primary winding, k_c is the clamp voltage ratio, V_{out} is the regulated output voltage, V_f is the forward voltage drop of the secondary rectifying diode, BV_{DSS} is the breakdown voltage of the main switch, k_D is the derating factor of the main switch, V_{os} is the clamp voltage overshoot, and $V_{bulk(max)}$ is the maximum DC bulk voltage supplying the controller. Using a 650 V MOSFET with a derating factor of 0.8 and a clamp voltage ratio, k_c, of 1.6 yields a turns ratio of 0.303. This maintains sufficient margin for the voltage rating of the MOSFET.

The power components for the flyback topology can be selected for operation in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM). Measuring the tradeoffs of the two modes at the power level required for this design, the transformer is designed to make a transition between DCM and CCM at low line and a load current of 1.8 A. This ensures that the converter operates in DCM at nominal load. The critical primary inductance, $L_{P(crit)}$, to cause this transition is calculated using Equation 2.

$$L_{P\_crit} = \frac{\eta \cdot V_{bulk\_min}^2 \cdot \left(\frac{V_{out}+V_f}{N}\right)^2}{2 \cdot f_{osc} \cdot V_{out} \cdot I_{out\_crit} \cdot \left(V_{bulk\_min} + \frac{V_{out}+V_f}{N}\right)^2} \quad \text{(eq. 2)}$$

where f_{osc} is the switching frequency of the controller, and $I_{out(crit)}$ is the load current at which the transition between DCM and CCM occurs. By operating in the transition between DCM and CCM, the secondary RMS current is minimized, reducing the requirements on the transformer and output capacitor. For the demonstration board design, with a transition occurring at I_{out} = 1.8 A, the primary inductance is 350 μH.

SENSE RESISTOR

To calculate the value of the current current sense resistor, R_{sense}, the peak current of the primary winding of the transformer must first be calculated. The energy storage relationship is used to determine the peak primary current, calculated using Equation 3.

$$I_{peak} = \sqrt{\frac{2 \cdot P_{out}}{L_{P(crit)} \cdot f_{OSC} \cdot \eta}} \quad \text{(eq. 3)}$$

Using the specified peak output power to calculate the peak primary current:

$$\sqrt{\frac{2 \cdot 48\ W}{350\ \mu H \cdot 65\ kHz \cdot 85\%}} = 2.23\ A$$

The NCP1219 has a current limit comparator reference voltage, V_{ILIM}, of 1 V, typical. R_{sense}, is calculated using Equation 4.

$$R_{sense} = \frac{V_{PWM}}{I_{peak}} \quad \text{(eq. 4)}$$

This results in a value of 449 mΩ for R_{sense} (R51‖R52‖R53‖R54). A 430 mΩ resistor is chosen for sufficient margin to deliver the peak output power.

The primary rms current, $I_{L(rms)}$ is needed in order to calculate the power dissipation in the R_{sense}. First, the maximum duty ratio, D_{max}, is calculated using Equation 5.

$$D_{max} = \frac{V_{out}}{V_{out} + N \cdot V_{bulk(min)}} \quad \text{(eq. 5)}$$

The maximum duty ratio determines the change in primary current, ΔI_L, as shown in Equation 6.

$$\Delta I_L = \frac{V_{bulk(min)} \cdot D_{max}}{L_{pri} \cdot f_{OSC}} \quad \text{(eq. 6)}$$

Finally, ΔI_L is used to calculate $I_{L(RMS)}$ as in Equation 7.

$$I_{L(RMS)} = \sqrt{D_{max} \cdot \left(I_{peak}^{\ 2} - I_{peak} \cdot \Delta I_L + \frac{\Delta I_L^{\ 2}}{2}\right)} \quad \text{(eq. 7)}$$

The power dissipated in the sense resistor is then calculated using Equation 8.

$$P_{R_{sense}} = I_{L(RMS)}^{\ 2} \cdot R_{sense} \quad \text{(eq. 8)}$$

The power rating of the resistor is chosen to handle the maximum power dissipation. For this design, the worst case peak power dissipation is calculated to be 400 mW. Four 1206 surface mount resistors in parallel are chosen to dissipate the power. Note that this is the worst case power dissipation calculated assuming a continuous output current of 2 A. For normal operating conditions (I_{out} = 1.25 A), the power dissipation is 208 mW.

PRIMARY SWITCH

The main MOSFET switch, Q5, is selected to operate at a junction temperature of 120°C at an ambient temperature of 85°C. The maximum power dissipation for Q5 is calculated using Equation 9, where T_{MAX} is the maximum junction temperature, T_A is the ambient temperature, and $R_{\theta JA}$ is the thermal resistance of the MOSFET.

$$P_{max} = \frac{\left(T_{max} - T_A\right)}{R_{\theta JA}} \quad \text{(eq. 9)}$$

An isolated TO−220 with an $R_{\theta JA}$ of 80°C/W results in a maximum power dissipation of 438 mW. The $R_{DS(on)}$ required to satisfy the maximum power dissipation at

nominal load is approximated by Equation 10. The value is taken from the datasheet curves for the desired junction temperature, provided by the MOSFET manufacturer.

$$R_{DS(on)} = \frac{P_{max}}{I_{L(RMS)}^{2}} \quad \text{(eq. 10)}$$

The MOSFET is sized so that the thermal requirements are met under nominal load (30 W). Equation 3 is used to determine the peak current, in this case using 30 W for P_{out}, yielding a peak current of 1.7 A.

The controller operates in DCM at low−line and nominal load. The equation for the primary rms current in DCM is shown in Equation 11. In this example, the primary rms current is calculated to be 0.69 A.

$$I_{L(RMS)} = I_{peak} \cdot \sqrt{\frac{D_{max}}{3}} \quad \text{(eq. 11)}$$

Substituting the resulting primary rms current into Equation 10, we find an $R_{DS(on)}$ of less than 1.1 Ω is required. The Infineon SPA07N65C3 n−channel MOSFET, with $R_{DS(on)}$ = 600 mΩ is used in this design. This is a conservative approach to the selection of Q5. The $R_{\theta JA}$ used to calculate the maximum power dissipation assumes the MOSFET operates in free air, without a heat sink. This design includes an aluminum heat sink attached to the body of the TO−220, reducing the thermal resistance and increasing the maximum power capability of the MOSFET.

SECONDARY RECTIFIER

The peak inverse voltage, PIV, of D12 is calculated by Equation 12.

$$PIV = V_{bulk(max)} \cdot N + V_{out} \quad \text{(eq. 12)}$$

$$375\ V \cdot 0.303 + 24\ V = 138\ V$$

Applying a silicon derating factor of 0.8 to PIV, the minimum breakdown voltage of D12 must be greater than 173 V. An MUR420, 200 V ultrafast rectifier is selected. The power dissipated in the secondary diode, P_d is approximated by Equation 13, where V_f is the forward voltage of the selected diode, and I_{out} is the nominal output current of the converter.

$$P_d = V_f \cdot I_{out} \quad \text{(eq. 13)}$$

OUTPUT CAPACITOR

The output capacitor is selected to satisfy the output voltage ripple requirements of the controller. The output capacitor must supply the entire output current during the controller on time. The capacitor value is calculated using Equation 14,

$$C_{out} = \frac{I_{out} \cdot t_{on(max)}}{V_{ripple}} \quad \text{(eq. 14)}$$

where $t_{on(max)}$ is the maximum on time of the controller, which can be calculated using D_{max} from Equation 5. For this design, Equation 14 results in a capacitor value of 70 μF.

The effective series resistance, ESR, of the capacitor also plays a significant role in the selection of the output capacitor. The secondary peak current charges the output capacitor during each cycle, and the ESR must not cause a voltage drop greater than the ripple voltage. The acceptable ESR is calculated using Equation 15,

$$ESR \le \frac{V_{ripple}}{I_{sec(peak)}} \quad \text{(eq. 15)}$$

where $I_{sec(peak)}$ is proportional to the primary peak current by the turns ratio, as given by Equation 16.

$$I_{sec(peak)} = \frac{I_{pri(peak)}}{N} \quad \text{(eq. 16)}$$

An ESR of 31 mΩ is required to meet the 200 mV output ripple requirement.

The output capacitor also has a specified rms current capability that must be considered. The rms current seen by the capacitor, $I_{Cout(RMS)}$, is calculated using Equation 17,

$$I_{Cout(RMS)} = \sqrt{I_{sec(RMS)}^{2} - I_{out(avg)}^{2}} \quad \text{(eq. 17)}$$

where $I_{out(avg)}$ is the maximum dc load current supplied by the converter and $I_{sec(RMS)}$ is the secondary rms current. For the maximum load current, the controller operated in CCM and $I_{sec(RMS)}$ is calculated using Equation 18.

For this design at maximum load, $I_{Cout(RMS)}$ is 2.44 A. An output capacitor with an ESR of 18 mΩ and an rms ripple current capability of 2.77 A is selected, and the resulting capacitor value is 1000 μF.

$$I_{sec(RMS)} = \sqrt{(1 - D_{max}) \cdot \left(I_{sec(peak)}^{2} - I_{sec(peak)} \cdot \frac{\Delta I_L}{N} + \frac{\Delta I_L^{2}}{N_2 \cdot 3} \right)} \quad \text{(eq. 18)}$$

AUXILIARY SUPPLY REGULATOR

The HV pin of the NCP1219 can be tied directly to the bulk storage capacitor and used to supply the IC in the absence of an auxiliary winding, for instance, during the startup of the adapter. The startup current is controlled internally and supplied to the V_{CC} capacitor through the V_{CC} pin. While V_{CC} is less than the Inhibit threshold voltage, the V_{CC} capacitor is charged with a current source of 200 μA (typical). Once the inhibit threshold is exceeded, the startup current (typically 13.5 mA) is supplied to the V_{CC} capacitor. When $V_{CC(on)}$ is exceeded, the internal current source is disabled, and the V_{CC} capacitor is discharged until V_{CC} decreases to less than $V_{CC(MIN)}$, at which time the startup current source is enabled, starting the DSS cycle over again.

The demonstration board contains several options for the HV pin connection and the biasing of V_{CC}. An auxiliary winding is used to supply V_{CC} at high line conditions in order to satisfy the low standby power requirement of 1 W.

Option 1 – Bulk Connection with Forward Auxiliary Winding

Connecting the HV pin to the bulk voltage and using a forward auxiliary winding provides an IC bias dependant on input voltage, but independent of the output voltage. This is required in this design due to the dual output voltage design. Otherwise the converter would require additional circuitry to prevent the converter from entering DSS mode during the standby conditions. Figure 3 shows this configuration. The voltage is supplied by the auxiliary winding through a series diode.

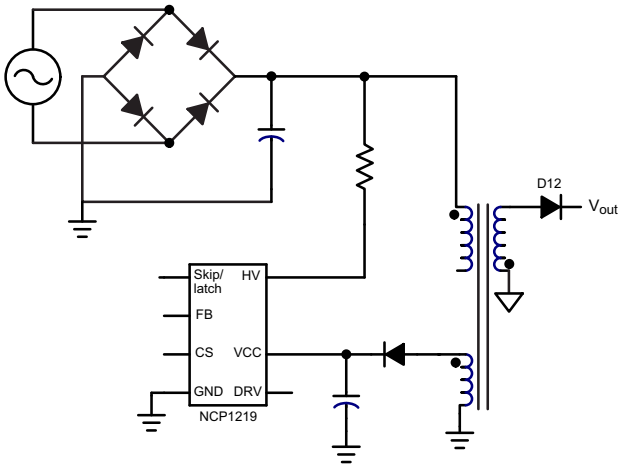

Figure 3. V_{CC} Connection Using a Forward Auxiliary Winding with DSS at Low−Line

The voltage on the V_{CC} pin can not exceed 20 V. Therefore the ratio between the number of turns on the auxiliary winding, NA, and the primary winding, N_A/N_P, is chosen to maintain V_{CC} below 20 V at the maximum input voltage. N_A/N_P is calculated using Equation 19.

$$N_A/N_P = \frac{\left(V_{CC} + V_f\right)}{V_{bulk}} \qquad \text{(eq. 19)}$$

This implies that, as the input voltage drops, the auxiliary winding can not supply the IC. When V_{CC} reduces to $V_{CC(MIN)}$, the startup circuit is enabled and the IC bias is supplied to the V_{CC} capacitor by the internal current source. Alternately, an auxiliary voltage greater than 20 V can be used by clamping V_{CC} using a zener diode, minimizing the input voltage at which the controller enters DSS mode. This is shown in Figure 4.

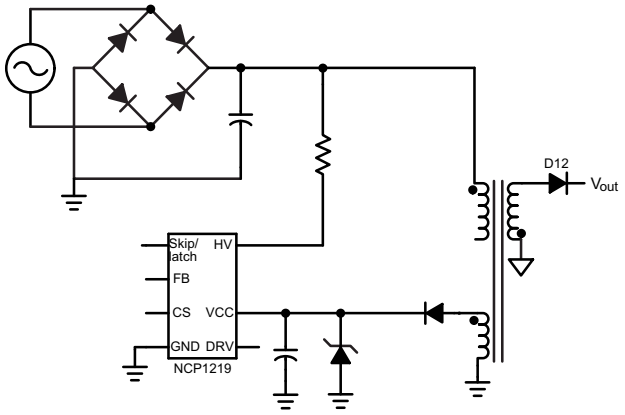

Figure 4. V_{CC} Connection using a Forward Auxilliary Winding with Added Zener

Option 2 – Full−time DSS Mode (No Auxiliary Winding)

The auxiliary winding is not necessary with DSS mode, so the connection to the auxiliary winding can be removed altogether, as shown in Figure 5.

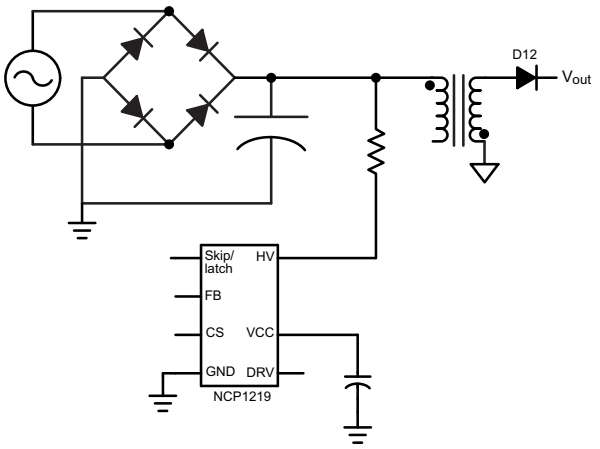

Figure 5. V_{CC} Connection with Full−Time DSS Mode (No Auxiliary Winding)

If standby power dissipation is not an issue, this option eliminates the extra components used with the auxiliary

winding. Care must be taken not to exceed the thermal capability of the IC. The power dissipated during DSS mode is approximated by Equation 20.

$$P_{DSS} = I_{CC3} \cdot V_{HV} \quad \text{(eq. 20)}$$

where V_{HV} is the HV pin voltage, and I_{CC3} is the controller supply current during normal switching operation. I_{CC3} has a component that is dependant on the gate charge of Q5, as shown in Equation 21,

$$I_{CC3} = I_{CC2} + Q_{g(tot)} \cdot f_{SW} \quad \text{(eq. 21)}$$

where $Q_{g(tot)}$ is the total gate charge of Q5.

The amount of power the controller is capable of dissipating depends on many factors, including the V_{CC} capacitor value, airflow conditions, proximity of the controller to other heat generating components on the board, and the layout of the metal traces on the board and their heat spreading characteristics. To determine the thermal characteristics of the controller in the application, the demonstration board is placed in a controlled ambient temperature and the V_{HV} that results in temperature shutdown is measured. $R_{\theta JA}$ of the controller is given by Eequation 22,

$$R_{\theta JA} = \frac{T_{SHDN} - T_A}{P_{DSS}} \quad \text{(eq. 22)}$$

where T_A is the ambient temperature of the system and T_{SHDN} is the junction temperature at which a thermal shutdown (TSD) fault occurs. For the demonstration board, with the HV pin tied directly to V_{bulk}, a V_{HV} of 257 V results in a TSD event, and $R_{\theta JA}$ is calculated as 82.5°C/W.

It is common to include a resistor, R_{bulk}, in series between the bulk voltage and the HV pin to spread the power dissipation between the controller and R_{bulk}. R_{bulk} often consists of at least two resistors in series for protection against shorted component testing. The same power dissipation limit is imposed on the controller as in the case where no series resistor is used. Therefore, adding R_{bulk} allows the maximum bulk voltage to increase by dissipating the difference in the power while the startup circuit is charging C_{CC}. The increased bulk voltage is given by Equation 23,

$$V_{bulk} = \frac{P_{DSS}}{I_{CC3}} + I_{start} \cdot R_{bulk} \quad \text{(eq. 23)}$$

where P_{DSS} is found by rearranging Equation 22 and using the $R_{\theta JA}$ measured above.

When adding the series resistors, it is recommended to maintain a minimum V_{HV} of 40 V to ensure there is enough headroom to allow the startup circuit to supply I_{start} to the V_{CC} pin. Therefore, at low line, the resistance between the bulk voltage and the HV pin can not exceed that given by Equation 24,

$$R_{bulk} \leq \frac{\left(V_{bulk(min)} - 40\ V\right)}{I_{start(min)}} \quad \text{(eq. 24)}$$

where $I_{start(min)}$ is the specified minimum startup current provided to the V_{CC} pin. $I_{start(min)}$ = 5 mA and assuming $V_{bulk(min)}$ = 90 V, the added series resistance should be no more than 10 kΩ. For the demonstration board, R_{bulk} is chosen as 3.6 kΩ so that I_{start} is 14.7 mA across the input voltage range. For this demonstration board, with R_{bulk} = 3.6 kΩ, I_{start} = 14.7 mA and a maximum ambient temperature of 85°C, the resulting maximum V_{bulk} is 310 V, a 53 V increase in comparison to the limit when connecting directly to the bulk voltage.

The power dissipated by R_{bulk} during the DSS cycle is found using the rms current supplied through the startup circuit during the DSS cycle, given by Equation 25,

$$P_{Rbulk} = R_{bulk} \cdot \left(I_{start(RMS)}\right)^2 \quad \text{(eq. 25)}$$

Option 3 – Half−Wave Rectified Connection

To reduce the power dissipation of DSS mode at high input voltage, the HV pin is connected to the half−wave rectified node of the bridge rectifier in place of the bulk voltage. Figure 6 illustrates this configuration.

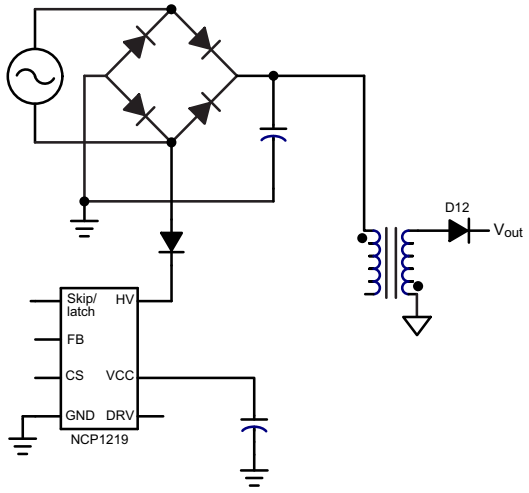

Figure 6. V_{CC} Connection with Full−time DSS Mode Supplied By the Half−Rectified Sine Wave

The average voltage applied to the HV pin is reduced because, during half of the input voltage cycle, the HV voltage is a function of the input sinusoid and the other half of the cycle the input voltage is zero. The half−wave rectified waveform is illustrated in Figure 7.

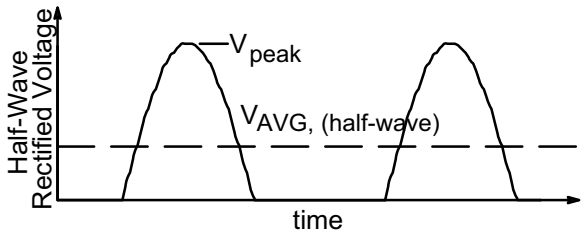

Figure 7. Half−Wave Rectified Waveform

The average HV pin voltage, $V_{AVG(half-wave)}$, is calculated using Equation 26.

$$V_{AVG(half-wave)} = \frac{V_{Peak}}{\pi} \quad \text{(eq. 26)}$$

In comparison, using the example from option 2 (full−time DSS mode with the HV pin connected to V_{bullk}), power dissipation, P_{DSS}, of 270 mW, and a junction temperature of 107°C is achieved.

The techniques mentioned above can be explored in different combinations to optimize standby power and thermal performance of the NCP1219.

FEEDBACK NETWORK

The negative feedback loop that controls the output voltage senses the output voltage using a voltage divider and compares it to the internal reference voltage of a TL431 precision reference. The output current of the TL431 is then a function of the bias that is required to force the internal reference of the TL431 and the output voltage to be equal. The TL431 output drives the cathode of an optocoupler, providing isolation between the primary and secondary side of the converter. The collector of the optocoupler is connected to the FB pin of the NCP1219, closing the feedback loop, as shown in Figure 8.

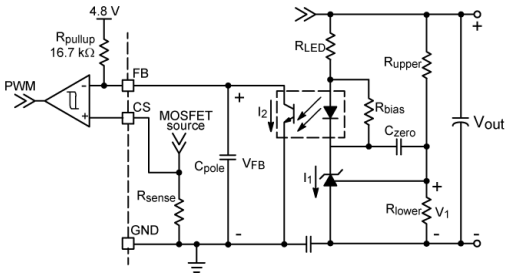

Figure 8. Feedback Network

V_{FB} is compared to V_{CS} to determine the on time. If there is an increase in load current, V_1 begins to decrease with V_{out}. This causes I_1 to decrease. The optocoupler collector current, I_2, also decreases causing V_{FB} to increase, increasing on time for the next switching cycle. The timing diagram describing the feedback loop is shown in Figure 9.

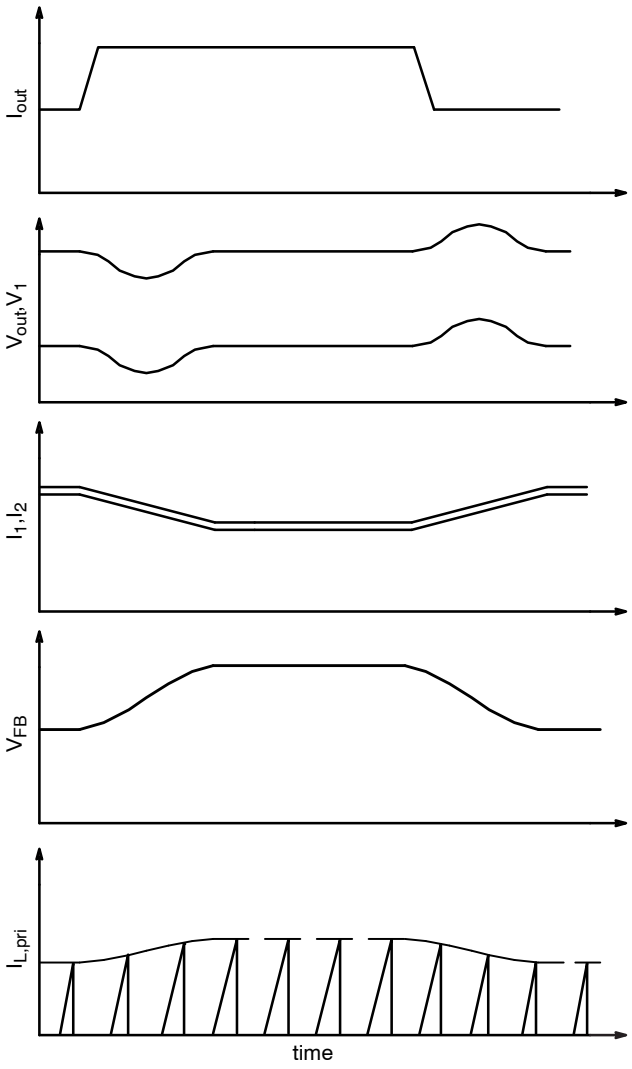

Figure 9. Feedback Loop Timing Diagram

STANDBY RECONFIGURATION CONTROL

The demonstration board has a dual output voltage mode. In normal operation, the converter provides a 24 V regulated output. During standby mode, the output supplies 7.25 V with a standby current of 70 mA. The output voltage level is selected by actively altering the voltage divider supplying the feedback loop. An additional resistor is connected in series with R32. A small signal MOSFET (Q6) is placed in parallel with the added resistance, as shown in Figure 10.

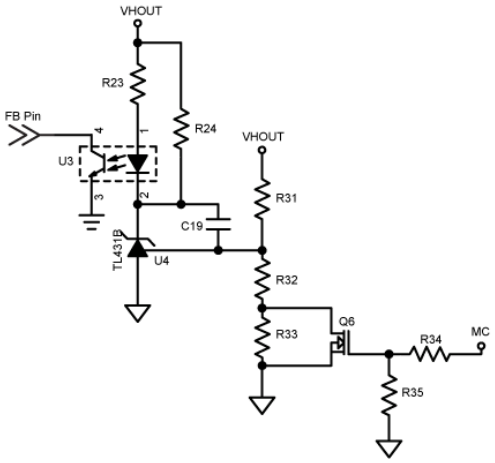

Figure 10. Standby Mode Reconfiguration Circuit

When 5 V is applied to the MC pin, Q6 turns on and R33 is bypassed. In this mode, the voltage divider is set by R31 and R32 only, providing 24 V to the output. If the MC pin is grounded or floating Q6 is off connecting R33 in series with R32. This reduces the voltage divider value and sets the output to 7.25 V.

LOOP STABILITY

The output voltage regulation is provided by the negative feedback loop described in the previous section. If the feedback loop is not stable, the converter oscillates. To ensure the stability of the converter, the closed loop frequency response phase margin should be greater than 45° at the crossover frequency. The first step in stabilizing the closed control loop is to analyze the frequency response of the power stage. Its contribution will determine the pole and zero placement. The gain and pole and zero placement of the feedback network are selected to achieve the desired crossover frequency and phase margin.

onsemi provides the excel based design tool ”FLYBACK AUTO”. It provides an automated method of compensating the feedback loop of an isolated flyback converter using the TL431 and an optocoupler. The tool takes system level inputs from the user, such as bulk input voltage, output voltage, output current, and controller switching frequency. A screenshot of the parameter capture screen is shown in Figure 11.

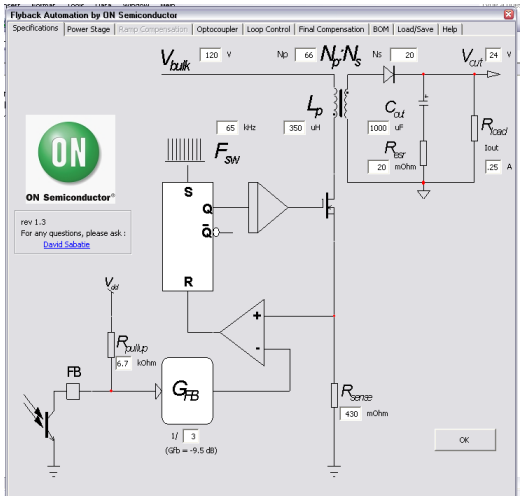

Figure 11. Screenshot of the Parameter Capture Screen from the Design Tool FLYBACK AUTO

After the input and output parameters are entered, the frequency response of the power stage is calculated. The response is presented both numerically, showing the frequency of each pole and zero, along with the dc gain of the power stage and graphically through the use of a Bode plot. This is shown in the screenshot presented in Figure 12.

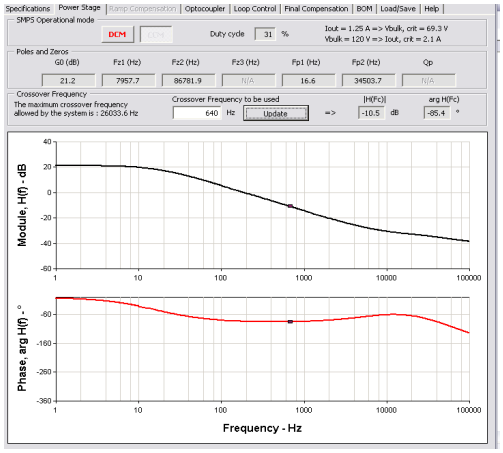

Figure 12. Screenshot of the Power Stage Frequency Response from the FLYBACK AUTO tool

Next, the contribution of the optocoupler to the frequency response of the system is considered. The pole of the compensation is selected to be less than that of the optocoupler. The user enters information about the optocoupler collected from the datasheet or through frequency response characterization of the chosen optocoupler. The optocoupler chosen for the demonstration board design is a Vishay SFH615A−3. Using the test setup shown in Figure 13, the optocoupler frequency response and CTR are measured. For the frequency response measurement, the dc bias of the 2.49 kΩ resistor is adjusted until the collector of the optocoupler measured 2.5 V.

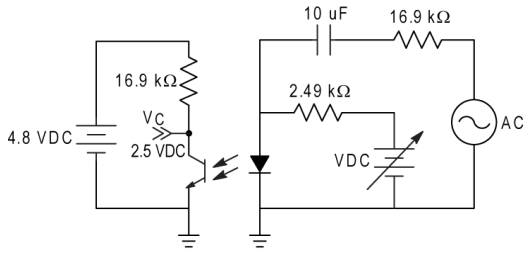

Figure 13. Optocoupler Frequency Analysis Test Circuit

From Figure 14, the crossover frequency of the SFH615A−3 is measured at 4.7 kHz. From the dc bias of the optocoupler, the current transfer ratio, CTR is measured as 41%. These values are used in the optocoupler page of the compensation tool.

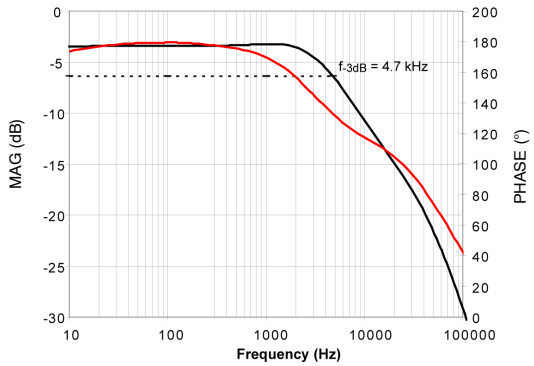

Figure 14. Frequency Response of Vishay's SFH615A3 Optocoupler

This data is entered into the tool and the capacitance contribution of the optocoupler is calculated.

The pole and zero placement of the type 2 compensation configuration is provided by the design tool based on the desired crossover frequency and phase margin entered by the user. If the desired crossover frequency causes the pole frequency of the compensation network to exceed the pole frequency of the optocoupler, then the crossover frequency is automatically reduced.

The total loop response is provided by the design tool based on the power stage response, optocoupler pole location, and the type 2 compensation design. The user can check the frequency response at various input voltages and load conditions to verify system stability over all conditions, as shown in Figure 15.

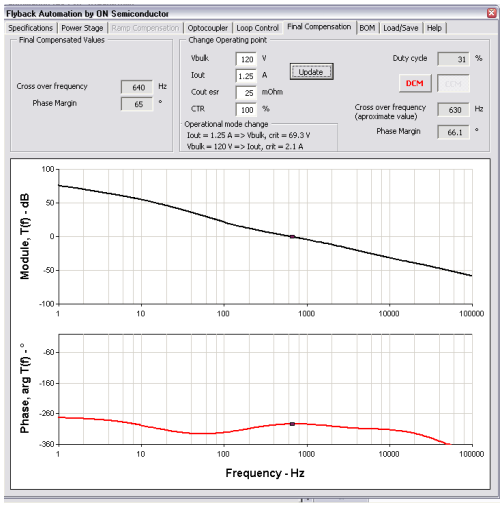

Figure 15. Screenshot of the Total Frequency Response Given By the Design Tool FLYBACK AUTO

A bill of materials for the compensation network is provided by the tool based on the calculations of the compensation network, as shown in Figure 16.

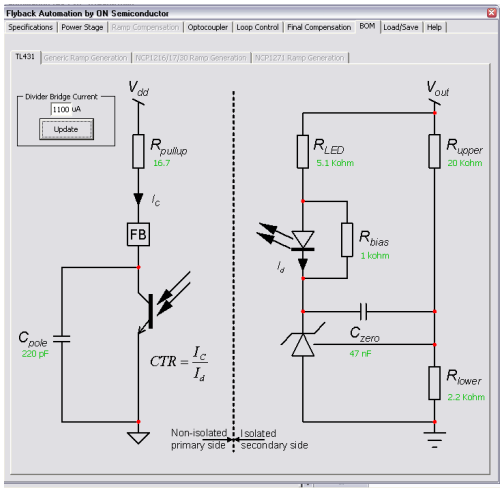

Figure 16. Screenshot of the Final Feedback Network Bill of Materials

The design tool provides a good starting point; a solution that allows the user to quickly set up a stable feedback network. It does not, however, release the designer from measuring the frequency response of the system and optimizing the loop stability and transient response tradeoffs. Using an AP Instruments AP200 frequency response analyzer, the frequency response of the power stage is confirmed, as shown in Figure 17. The measured gain boost required for a crossover frequency of 1 kHz is 17 dB, slightly higher than estimated by the compensation tool.

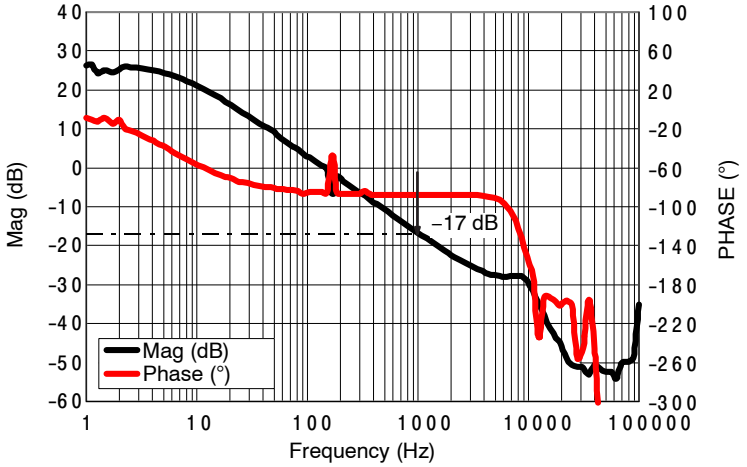

Figure 17. Frequency Response of the Power Stage

The pole introduced by the optocoupler needs to be considered. The pole location is dependant on the biasing conditions of the optocoupler. The internal 16.7 kΩ pullup resistor and the output capacitance of the optocoupler set the pole at 4.7 kHz, as shown in Figure 14. The location of this pole limits the available bandwidth of the system.

The demonstration board design uses the k−factor approach to pole and zero placement, and a phase margin of 65° is chosen. For the type 2 compensation network, the k−factor is found using Equation 27,

$$k = \tan\left(\frac{PM - PS - 90}{2} + 45\right) \qquad \text{(eq. 27)}$$

where PM is the desired phase margin, and PS is the phase brought by the power stage. For a crossover frequency, f_c, of 1 kHz, the phase caused by the power stage is −88°. The resulting k value is 4.2. The pole frequency, f_p, is calculated using Equation 28.

$$f_p = f_C \cdot k \qquad \text{(eq. 28)}$$

The pole frequency for this design is equal to 4.2 kHz. The zero frequency, f_z, is calculated using Equation 29,

$$f_z = \frac{f_C}{k} \qquad \text{(eq. 29)}$$

The zero frequency is set to 240 Hz.

The bandwidth of the optocoupler can be used to set the pole location of the compensation network. In this case, adding capacitance to satisfy the k−factor calculations limits the bandwidth of the system and causes slowing of the transient response and increased output ripple. The capacitance needed to place the zero is calculated using Equation 30.

$$C_{zero} = \frac{1}{2 \cdot \pi \cdot f_z \cdot R_{upper}} \qquad \text{(eq. 30)}$$

For this design, a value of 33 nF is chosen for C_{zero}.

The required gain boost (G_{fc}) needed to compensate the system and provide a crossover frequency of 1 kHz is measured as 17 dB. The gain provided by the compensation network is calculated using Equation 31.

$$G = 10^{\frac{G_{fC}}{20}} \qquad \text{(eq. 31)}$$

The R_{LED} value needed to produce this gain is calculated using Equation 32.

$$R_{LED} = \frac{R_{pullup} \cdot CTR}{G} \qquad \text{(eq. 32)}$$

From the measurements and the resulting gain, R_{LED} is 990 Ω.

The open loop response is measured by injecting an ac signal across R19 using a network analyzer and an isolation transformer as shown in Figure 18. The open loop response is the ratio of B to A.

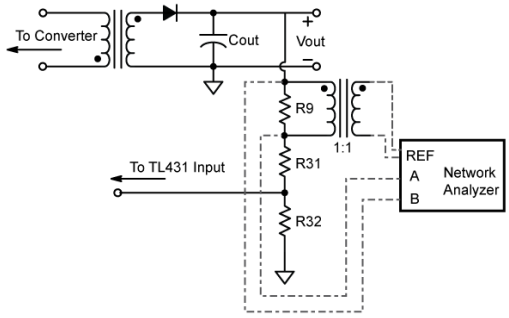

Figure 18. Open Loop Frequency Response Measurement Setup

The resulting loop response after compensation is shown in Figure 19, where the crossover frequency is 1.3 kHz, with a phase margin of 60°, measured at low−line and nominal load current.

Figure 19 compares the measured results to the frequency response produced by the “FLYBACK AUTO” tool. There is good agreement for frequencies at or below the crossover frequency. There is divergence at higher frequencies due to the double pole of the output filter on the demonstration board. The frequency of the double pole (f_{dp}) is given by Equation 33.

$$f_{dp} = \frac{1}{2 \cdot \pi \cdot \sqrt{L1 \cdot C16}} \quad \text{(eq. 33)}$$

where L1 is the output inductor and C16 is the output filter capacitor, which results in a pole frequency of 7.2 kHz. The “FLYBACK AUTO” tool does not include an output filter in the compensation design.

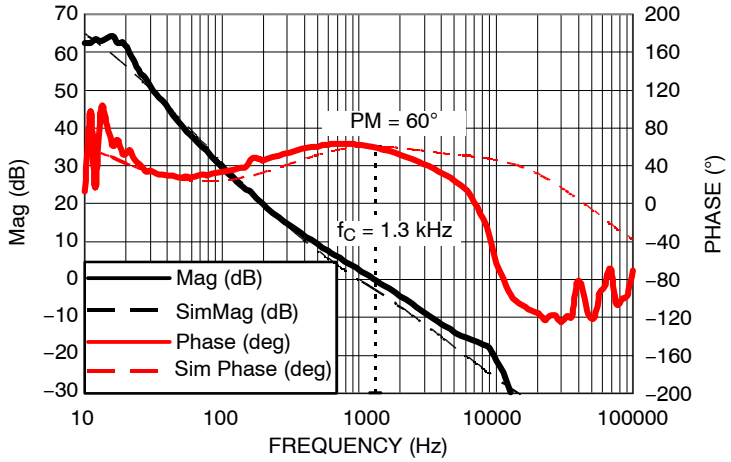

Figure 19. Total Loop Response Measured at Low Line and Nominal Load Current

SKIP MODE FOR REDUCED STANDBY POWER DISSIPATION

The NCP1219 employs an adjustable skip level that reduces input power in light load and standby conditions. V_{FB} is compared to $V_{Skip/latch}$. If V_{FB} decreases to less than $V_{Skip/latch}$, the drive pulses stop until the feedback loop causes V_{FB} to increase to greater than $V_{Skip/latch}$. $V_{Skip/latch}$ is adjustable by connecting an external resistor between the Skip/latch and GND pins, as shown in Figure 20. If no resistor is connected between the pins, the skip threshold is the default value, V_{skip}. If the voltage on the Skip/latch pin exceeds 1.3 V, then the skip threshold is clamped to $V_{skip(MAX)}$, typically 1.3 V.

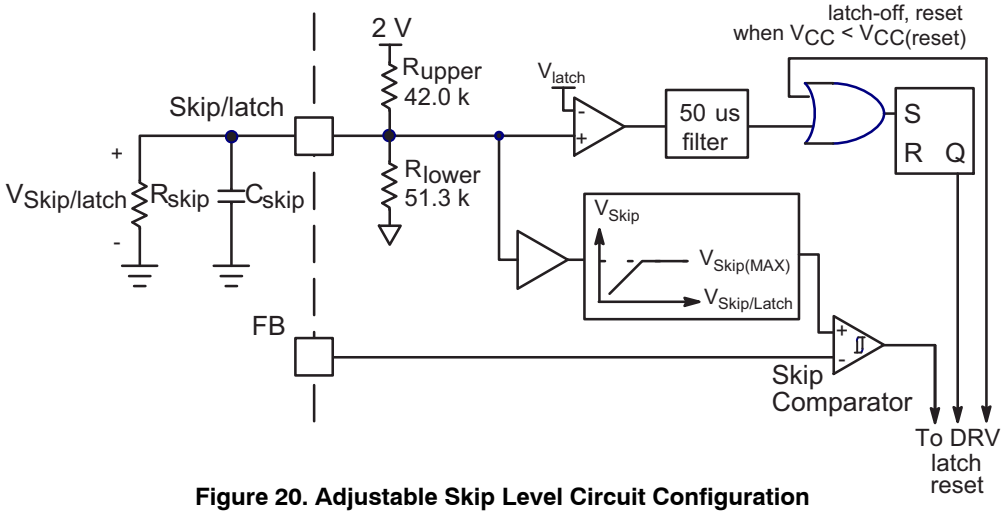

Figure 20. Adjustable Skip Level Circuit Configuration

Under light load conditions, the controller enters skip mode. As seen in Figure 21, when V_{FB} (C3) decreases to less than $V_{Skip/latch}$ (C1) the drive pulses stop (C4). This in turn causes V_{FB} to increase as V_{out} decreases.

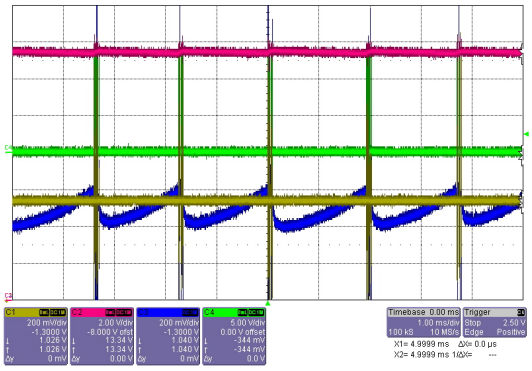

Figure 21. Skip Mode Operation Waveforms; C1 = $V_{Skip/latch}$, C2 = V_{CC}, C3 = V_{FB}, C4 = V_{DRV}

For the demonstration board design, the NCP1219 default skip threshold is used to reduce component count. Selecting a higher skip threshold has tradeoffs. If the skip voltage is set too high, during normal operation at nominal loads the system is in skip mode. This can cause audible noise. On the other hand, when the board is operating in standby mode and the load is very low, a higher skip threshold minimizes the number of switching cycles per skip cycle. This reduces standby power.

OVERPOWER COMPENSATION

For this demonstration board, without overpower compensation, overcurrent protection occurs at a measured output power of 67.2 W at high line and 57.4 W at low line conditions. The variation in overcurrent output power with input voltage is due to the propagation delay (t_{delay}) of the PWM comparator. t_{delay} has an increased effect on the power delivered at high line than at low line as shown in Figure 22.

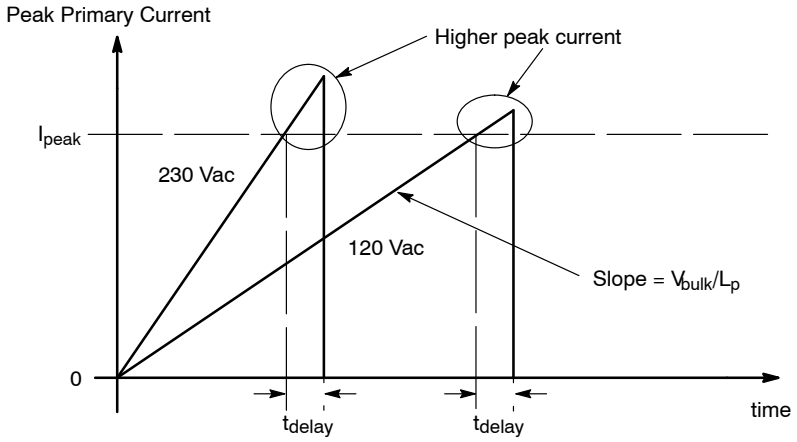

Figure 22. Overpower Effect Due to Propagation Delay

This effect is called “Over power” because it increases the power at which the overcurrent protection disables the controller. Specifically, for a DCM flyback system, the total power delivered to the output including the propagation delay effect is:

$$P_{out} = \frac{1}{2} \cdot L_P \cdot \left(I_{peak} + \frac{V_{bulk}}{L_p} \cdot t_{delay} \right)^2 \cdot f_{SW} \cdot \eta \quad \text{(eq. 34)}$$

The NCP1219 is designed with a very short t_{delay} (59 ns typical). This minimizes the overpower. If a tighter overpower limit is required, then overpower compensation is implemented by using the circuits shown in Figures 23 and 24.

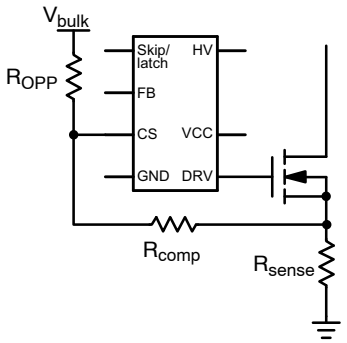

Figure 23. Overpower Compensation Circuit Using the Bulk Capacitor Voltage

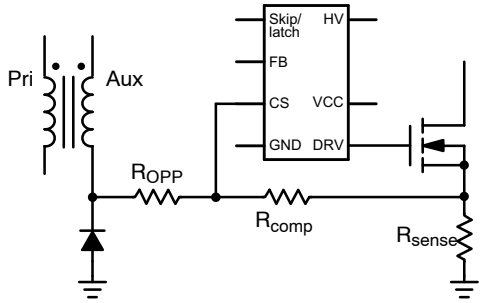

Figure 24. Overpower Compensation Circuit Using a Forward Auxiliary Winding

The circuit in Figure 23 modifies the I_{peak} setpoint proportional to the HV bulk level. The voltage divider formed by R_{OPP} and R_{comp} creates an offset that compensates for the propagation delay, but increases power dissipation. Figure 24 provides another option that results in reduced power dissipation. By altering the connection of the auxiliary winding diode, a new setpoint is created whose voltage is proportional to V_{in}. The power dissipation is reduced by a factor of $(N_{pri}:N_{aux})^2$.

To determine the required amount of compensation, first the peak current for the overcurrent power at high line is calculated using Equation 35.

$$I_{peak} = \sqrt{\frac{2 \cdot P_{out}}{L_p \cdot f_{OSC} \cdot \eta}} \quad \text{(eq. 35)}$$

Using the measured output power at high line, the calculated peak current of 2.63 A causes a voltage on the sense resistor, as in Equation 36.

$$V_{sense(peak)} = I_{peak} \cdot R_{sense} \quad \text{(eq. 36)}$$

The resulting sense voltage is 1.13 V. Under high line conditions, the desired overpower output current is 2.5 A (60 W). Calculate the sense voltage associated with the desired output power using the same method. In this case, an output power of 60 W results in a sense voltage of 1.06 V. The difference between the calculated sense voltages is given by Equation 37.

$$V_{CS(offset)} = V_{sense(peak1)} - V_{sense(peak2)} \quad \text{(eq. 37)}$$

For this design $V_{CS(offset)}$ is 70 mV. This represents the offset voltage required on the CS pin to force the controller to enter overcurrent protection at the desired output power. If the circuit in Figure 23 is chosen, the R_{OPP} resistor is selected to ensure the power dissipation of the circuit does not exceed the desired maximum, P_{OPP}. For this design 50 mW is selected. The resistor value is calculated using Equation 38.

$$R_{OPP} = \frac{V_{bulk(max)}^2}{P_{OPP}} \quad \text{(eq. 38)}$$

R_{OPP} creates a current that flows through R_{comp}, creating the necessary offset ($V_{CS(offset)}$) on the CS pin to compensate for the propagation delay. The current is calculated with Equation 39.

$$I_{OPP} = \frac{V_{bulk(max)} - 1\ V}{V_{CS(offset)}} \quad \text{(eq. 39)}$$

The ramp compensation resistor also creates an offset voltage due to the ramp compensation current supplied by the controller. The internal current ramp has a slope of 8.12 μA/μs. The controller on time is measured near the current limit in order to determine the peak voltage on the ramp compensation resistor. The total effect of the added compensation is shown in Equation 40.

$$R_{ramp} = \frac{V_{CS(offset)}}{8.12\ A/s \cdot t_{on} + \frac{V_{bulk(max)} - 1}{R_{OPP}}} \quad \text{(eq. 40)}$$

R_{OPP} is chosen to be 2.8 MΩ. R_{ramp} is chosen to be 412 Ω to achieve an overcurrent limit at 60 W under high line conditions. The low line overcurrent limit must also be confirmed to ensure that the peak power is delivered with the overpower compensation circuit. The low line current limit for this design is measured to be 2.2 A (52.8 W).

OVERVOLTAGE PROTECTION

Overvoltage protection (OVP) is implemented on this demonstration board using one of two options; primary side overvoltage protection or secondary side overvoltage protection.

Primary side OVP is implemented as shown in Figure 25. With the auxiliary winding in a flyback configuration, V_{CC} is proportional to the output voltage. A zener diode and series current limiting resistor are connected between the Skip/latch pin of the controller and V_{CC}. If the output voltage starts to rise, V_{CC} rises and current starts to flow through ZD1. The zener current causes the voltage on the Skip/latch pin to exceed the latch threshold and the controller enters latched fault mode.

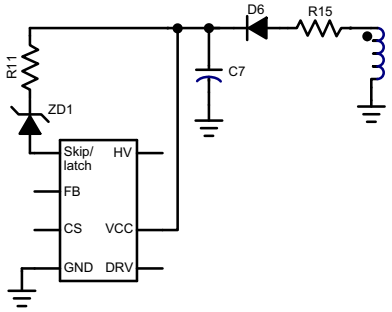

Figure 25. Primary Overvoltage Protection Circuit

A secondary side OVP latch function is implemented using the circuit shown in Figure 26. The primary and secondary sides are isolated using an optocoupler. The zener diode ZD2 starts to conduct if the output voltage exceeds the regulated voltage. The current conducted by ZD2 biases Q3 and causes current to flow from the cathode of the optocoupler. The optocoupler transistor turns on and the voltage on the Skip/latch pin increases, latching the controller. The value of R10 is chosen in order to limit the voltage applied to the Skip/latch pin during a fault condition.

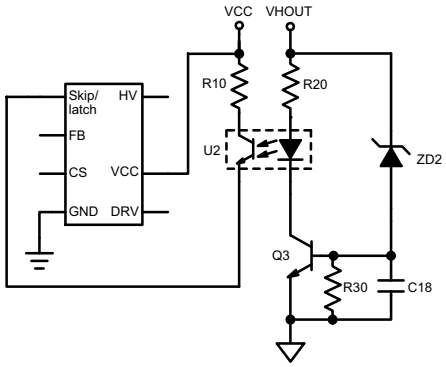

Figure 26. Secondary Overvoltage Protection Circuit

LATCH PROTECTION

The latching fault protection offered by the NCP1219 can also be used to implement other convenient board level protection functions besides the overvoltage protection options included on this demonstration board. For example, the latch pin may be used to implement temperature shutdown externally using an NTC element driving the base of a bipolar transistor, Q1, as shown in Figure 27. The NTC value is chosen so that the voltage divider made between it and R_{be} turn on Q1 at the proper temperature. Once the controller enters a latched fault, V_{CC} must decrease lower than $V_{CC(reset)}$ to reset the controller. This is typically achieved by removing power from the mains.

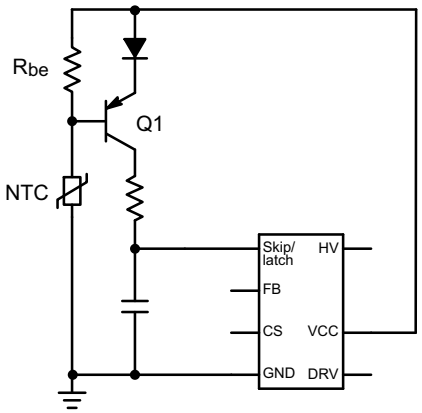

Figure 27. Temperature Shutdown Latch Circuit

Any other generic latched fault can be implemented using a circuit similar to Figure 28. A fault signal is applied to the base of an npn bipolar transistor, Q2, whose cathode drives the base of a pnp bipolar transistor, Q1, bringing the Skip/latch pin high.

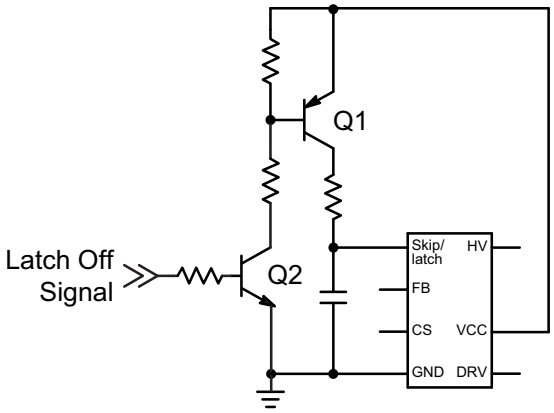

Figure 28. Generic Latched Shutdown Example

SOFT−START

Soft−start reduces stress during power up by slowly increasing the peak current until the soft−start timer expires. The NCP1219 implements soft−start by comparing the CS pin voltage to the lesser of the internal divided by three FB voltage or the internal soft−start ramp. The soft−start management block of the NCP1219 controller enables the soft−start voltage ramp to rise in 4.8 ms. Figure 29 shows the current sense waveform taken differentially across the sense resistor, as the current ramps up during the first 4.8 ms of the startup time.

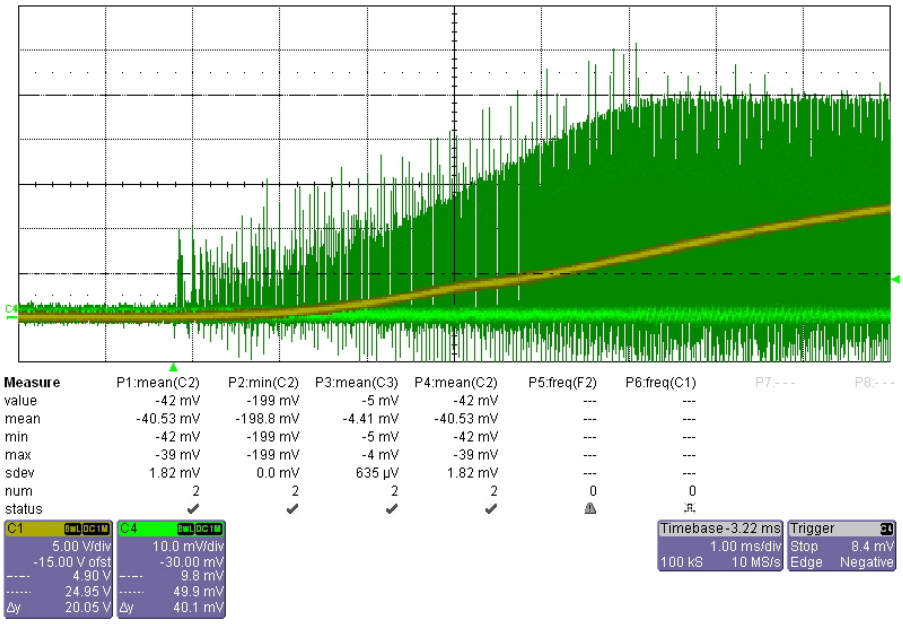

Figure 29. Startup Waveforms Showing Soft−Start Behavior; C1 = V_{out}, C4 = V_{CS}/20

BOARD LAYOUT

The demonstration board is built using a double sided FR4 board. Through hole components are placed on the top layer and surface mount components on the bottom layer. The board is constructed using 2 oz copper.

During the layout process care was taken to:

1. Minimize trace length, especially for high current loops.
2. Use wide traces for high current connections.
3. Use a single ground connection.
4. Keep sensitive nodes away from noisy nodes such as the drain of the power switch.
5. Place decoupling capacitors close to the pins of IC.
6. Sense output voltage at the output terminal to improve load regulation.

Figure 30 shows the top layer of the PC board, including the silkscreen, copper, and soldermask.

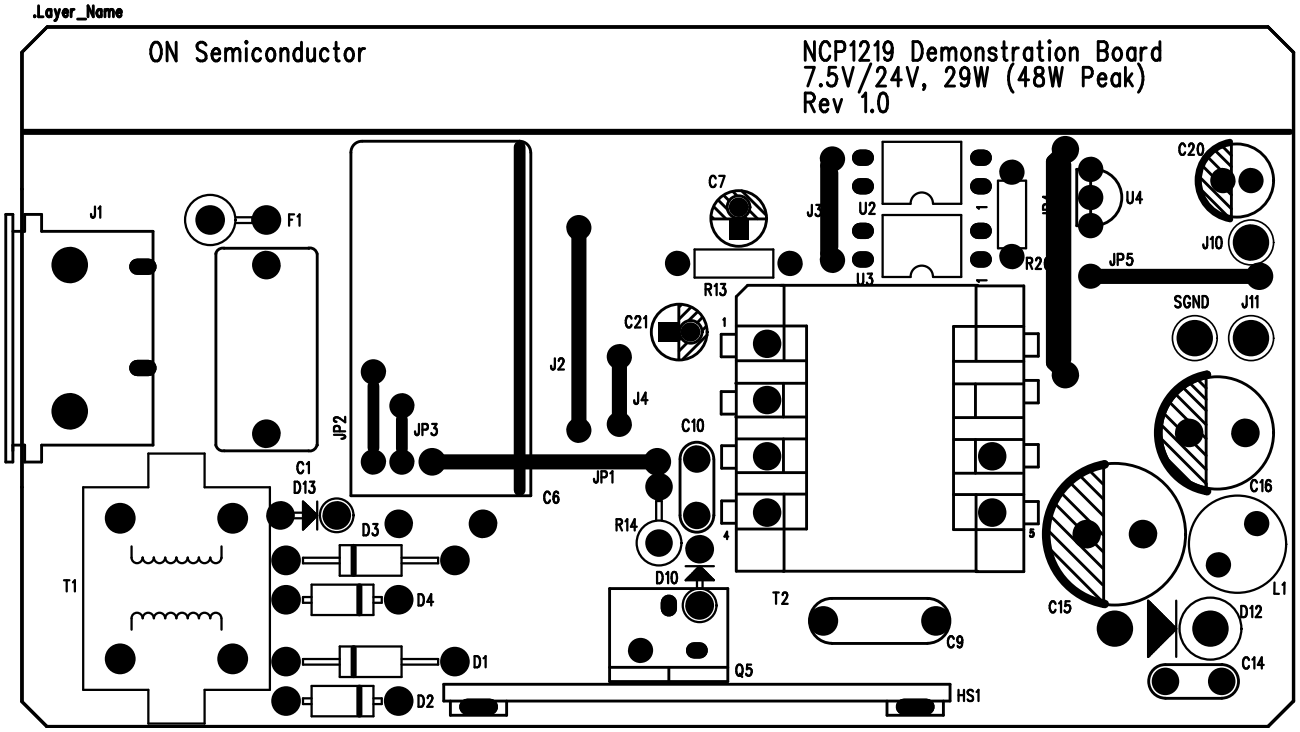

Figure 30. Layer 1 (Top)

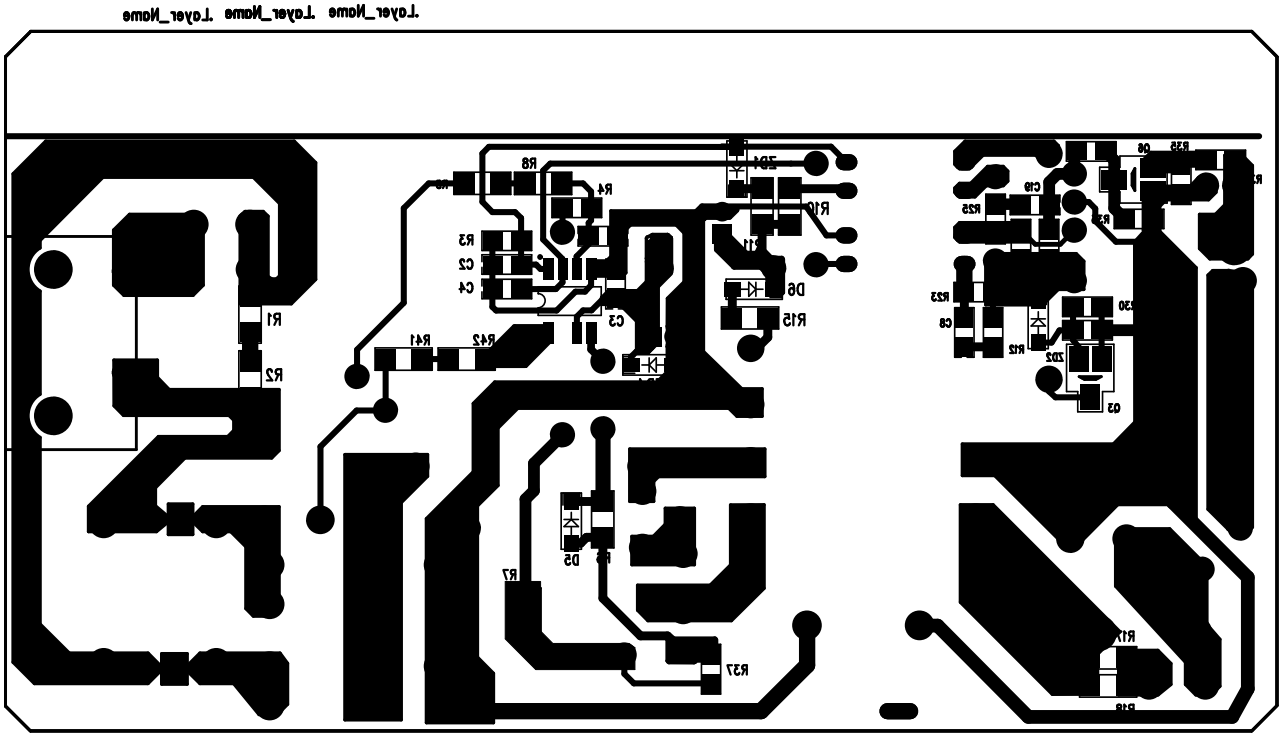

Figure 31. Layer 2 (Bottom)

Figure 31 shows the bottom layer of the PC board, including the silkscreen, copper, and soldermask.

The layout files may be available. Please contact your sales representative for availability.

DESIGN VALIDATION

The top and bottom view of the board are shown in Figures 32 and 33, respectively.

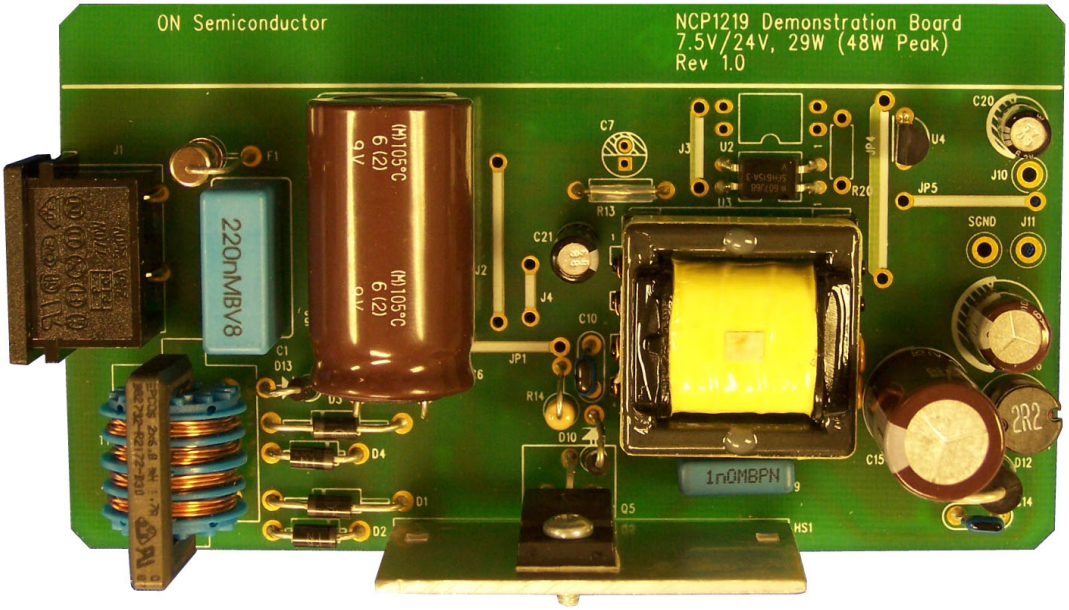

Figure 32. NCP1219 Demonstration Board Top View

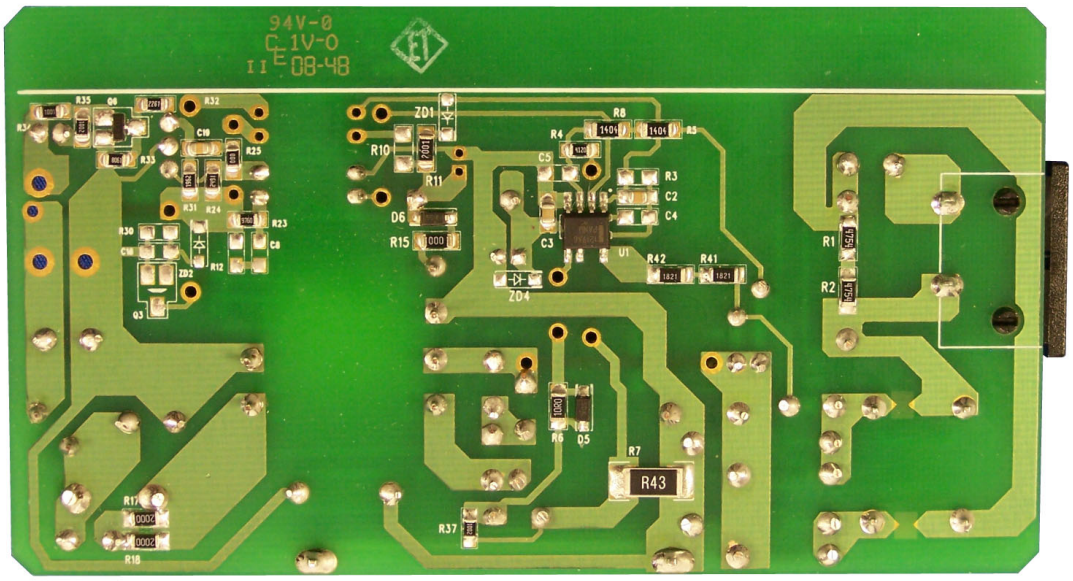

Figure 33. NCP1219 Demonstration Board Bottom View

The bill of materials that accompanies the demonstration board circuit schematic of Figure 2 is listed in Table 2.

Table 2. BILL OF MATERIALS

Designator	Qty	Description	Value	Footprint	Manufacturer	Manufacturer Part Number
C1	1	Capacitor, Metalized Poly Film	0.22 μF, 275 V	Radial	Kemet/ Evox−Rifa	PHE840MX6220MB06
C2	1	Capacitor, Ceramic, SMD	1000 pF	SM/0805	Vishay	VJ0805Y102KXXA
C3	1	Capacitor, Ceramic, SMD	0.1 μF	SM/0805	Vishay	VJ0805Y104KXXA
C4	1	Capacitor, Ceramic, SMD	open	SM/0805	−	−
C5	1	Capacitor, Ceramic, SMD	100 pF	SM/0805	Vishay	VJ0805Y101KXXA
C6	1	Capacitor, Electrolytic	100 μF, 400 V	Radial	United Chemicon	EKXG401ELL101MMN3S
C7	1	Capacitor, Electrolytic	open	−	−	−
C9	1	Capacitor, Ceramic, Y−cap	1 nF, 440 V	Radial	Kemet/ Evox−Rifa	ERO610RJ4100M
C10	1	Capacitor, Ceramic, Through Hole	4700 pF, 630 V	Radial	TDK	FK20C0G2J472J
C14	1	Capacitor, Ceramic, Through Hole	470 pF, 250 V	Radial	TDK	FK18C0G2E471J
C15	1	Capacitor, Electrolytic	1000 μF, 35 V	Radial	United Chemicon	EKZE350ELL102MK25S
C16	1	Capacitor, Electrolytic	330 μF, 35 V	Radial	United Chemicon	EKZE350ELL331MJ16S
C18	1	Capacitor, Ceramic, SMD	open	SM/0805	−	−
C19	1	Capacitor, Ceramic, SMD	0.033 μF	SM/0805	Vishay	VJ0805Y333KXJA
C20	1	Capacitor, Electrolytic	220 μF, 6.3 V	Radial	United Chemicon	ESMG6R3ELL221ME11D
C21	1	Capacitor, Electrolytic	22 μF, 25 V	Radial	United Chemicon	ESMG250ELL220ME11D
D1 D2 D3 D4 D10 D13	6	Diode, Rectifier	1 A, 1000 V	Axial	**onsemi**	1N4007RLG
D5 D6	2	Switching Diode	100 V	SOD−123	**onsemi**	MMSD914T1G
D12	1	Diode, Ultrafast Rectifier	4 A, 200 V	Axial	**onsemi**	MUR420RLG
F1	1	Fuse, Radial Lead	2 A, 250 V	Radial	Littelfuse	3921200000
HS1	1	Heatsink	−	Custom		
J1	1	AC Connector	IEC 320−C8	Through Hole	Qualtek	770W−X2/10
J2	1	Electrical Connection on Top Layer of PCB	−	−	−	−
J3	1	Electrical Connection on Top Layer of PCB	−	−	−	−
J4	1	Electrical Connection on Top Layer of PCB	−	−	−	−
J5	1	Header, 1 Row of 3	−	0.156	Molex	26−64−4030
JP1	1	Electrical Connection on Top Layer of PCB	−	−	−	−
JP2 JP3	2	jumper wire	22 AWG	−	Belden	8021
JP4	1	Electrical Connection on Top Layer of PCB	−			
L1	1	Inductor, Power	2.2 μH	Radial	Coilcraft	RFB0807−100L
MECHANICAL	1	Screw	M3 8 mm	−	Building Fasteners	MPMS 003 0008 PH
MECHANICAL	2	Insulating tubing	22 AWG	−	SPI Technology	TTI−S22−1100−NAT
Q3	1	Transistor, NPN Bipolar	open	SOT−23	−	−
Q5	1	MOSFET, Power	7 A, 650 V	TO−220−3−31, FullPAK	Infineon	SPA07N65C3
Q6	1	MOSFET, Small Signal	115 mA, 60 V	SOT−23	**onsemi**	2N7002LT1G
R1 R2	2	Resistor, SMD	4.75 MΩ	SM/1206	Vishay	CRCW12064M75FKEA
R3	1	Resistor, SMD	open	SM/0805	−	−
R4	1	Resistor, SMD	412 Ω	SM/0805	Vishay	CRCW0805412RFKEA
R5 R8	2	Resistor, SMD	1.4 MΩ	SM/1206	Vishay	CRCW12061M40FKEA
R6 R15	2	Resistor, SMD	10 Ω	SM/1206	Vishay	CRCW120610R0FKEA
R9	1	Resistor, Through Hole	20 Ω	Axial	Yageo	MFR−25FBF−20R0
R10 R11	2	Resistor, SMD	open	SM/1206	−	−
R13	1	Resistor, Through Hole	0 Ω	Axial	Panasonic − ECG	ERD−S2T0V
R14	1	Resistor, Through Hole	120 kΩ	Axial	Vishay	HVR3700001203JR500

Table 2. BILL OF MATERIALS

Designator	Qty	Description	Value	Footprint	Manufacturer	Manufacturer Part Number
R16	1	Resistor, Through Hole	open	Axial	–	–
R18	1	Resistor, Through Hole	100 Ω	Axial	Vishay	5093NW100R0JBC
R20	1	Resistor, Through Hole	open	Axial	–	–
R23	1	Resistor, SMD	976 Ω	SM/0805	Vishay	CRCW0805976RFKEA
R24	1	Resistor, SMD	2.49 kΩ	SM/1206	Vishay	CRCW08052K49FKEA
R25	1	Resistor, SMD	0 Ω	SM/0805	Vishay	CRCW08050000Z0EA
R30	1	Resistor, SMD	open	SM/0805	–	–
R31	1	Resistor, SMD	19.6 kΩ	SM/1206	Vishay	CRCW080519K6FKEA
R32	1	Resistor, SMD	2.26 kΩ	SM/0805	Vishay	CRCW08052K26FKEA
R33	1	Resistor, SMD	8.06 kΩ	SM/0805	Vishay	CRCW08058K06FKEA
R34	1	Resistor, SMD	1 kΩ	SM/0805	Vishay	CRCW08051K00FKEA
R35 R37	2	Resistor, SMD	10 kΩ	SM/0805	Vishay	CRCW120610K0FKEA
R41 R42	2	Resistor, SMD	1.82 kΩ	SM/1206	Vishay	CRCW12061K82FKEA
R51 R52 R53 R54	4	Resistor, SMD	1.69 Ω	SM/1206	Vishay	CRCW12061R69FNEA
T1	1	Inductor, Common Mode Choke	10 mH	Through Hole	Epcos	B82732R2142B30
T2	1	Transformer, Flyback	400 μH	Custom, Through Hole	ICE Components	TO09002−1
U1	1	Switchmode Controller	NCP1219	SOIC−7	**onsemi**	NCP1219AD65R2G
U2	1	Optocoupler	open	DIP−4	–	–
U3	1	Optocoupler	150% CTR	DIP−4	Vishay	SFH615A−3
U4	1	Programmable Precision Reference	TL431B	TO−92	**onsemi**	TL431BCLPRMG
ZD1	1	Diode, Zener	open	SOD−123	–	–
ZD2 ZD4	2	Diode, Zener	open	SOD−123	–	–

1. Coilcraft components can be ordered at http://www.coilcraft.com
2. Epcos components can be ordered at http://www.epcos.com
3. ICE Components can be ordered at http://www.icecomponents.com
4. Infineon components can be ordered at http://www.infineon.com
5. Kemet components can be ordered at http://www.kemet.com
6. TDK components can be ordered at http://www.tdk.com
7. Vishay Components can be ordered at http://www.vishay.com

The converter performance is evaluated and compared to the original goals. From Table 1, the evaluation criteria includes:

1. Efficiency.
2. Standby input power.
3. Step load response.
4. Output voltage ripple.

The efficiency of the converter is measured across the universal input voltage range. Figure 34 shows the efficiency vs output current at 90 Vac, 100 Vac, 115 Vac, 230 Vac and 265 Vac.

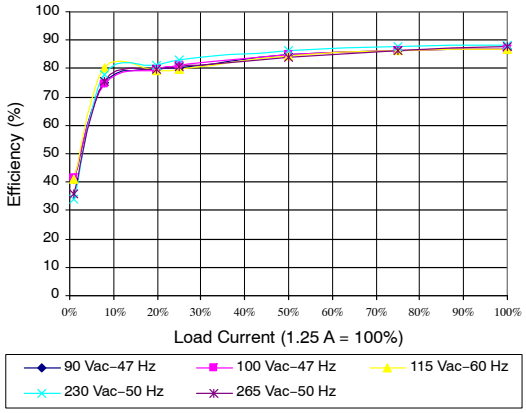

Figure 34. Efficiency vs. output current

The average efficiency, η_{avg}, as defined by the Energy Star 2.0 External Power Supply (EPS) specification, was calculated for various input voltages. The results are shown in Figure 35. The converter is Energy Star 2.0 compliant, maintaining η_{avg} greater than 83.5%.

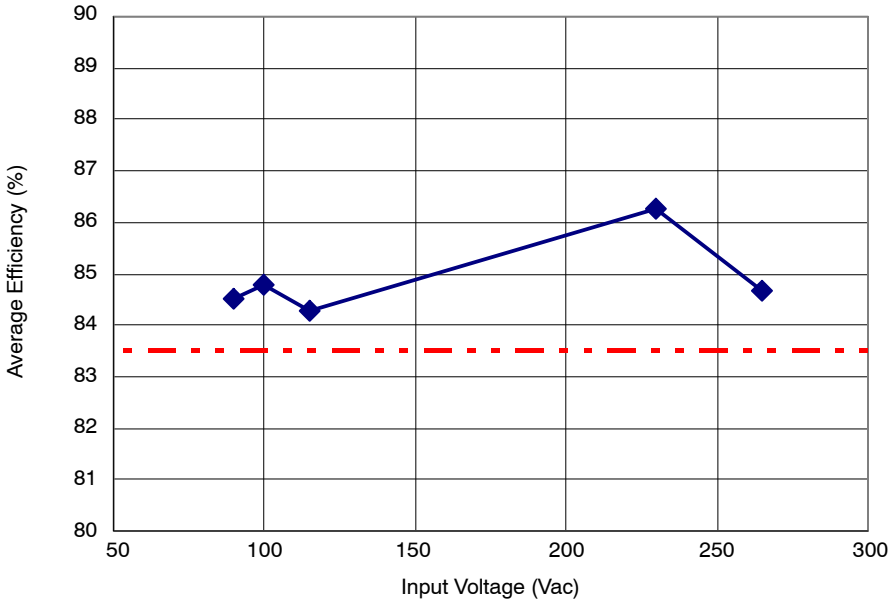

Figure 35. Average Efficiency vs. Line Voltage

The standby input power requirement is less than 1 W over the range of input voltage. Figure 36 shows the standby input power versus input voltage. Starting at low line, the input power rises with increasing input voltage. At line voltages less than 180 Vac, the controller operates in DSS mode, because the forward auxiliary winding voltage is less than that required to maintain V_{CC} greater than $V_{CC(MIN)}$. A portion of the standby input power is due to the startup circuit. As the input voltage increases, the auxiliary winding begins to supply the controller and the startup circuit is no longer active. A sudden drop in the standby input power is observed when DSS is disabled. As the input voltage continues to increase, so does the input power.

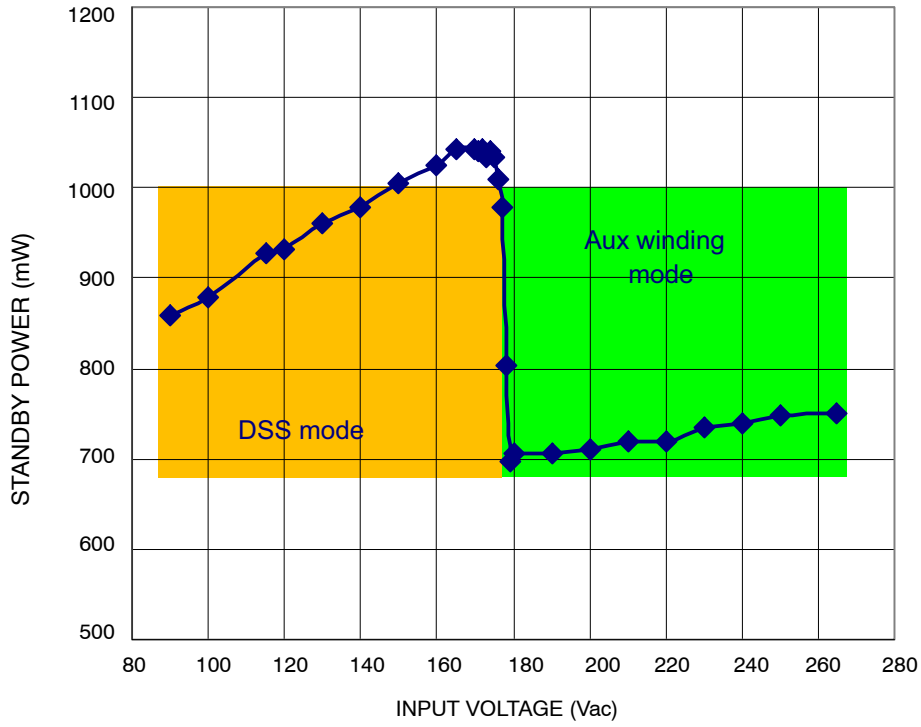

Figure 36. Standby Power versus Input Voltage (Forward Auxiliary Winding Connection)

The output voltage ripple is measured at 16 mV at high line and full load. It is significantly less than the 50 mV target. The output voltage ripple waveform at high line and full load is shown in Figure 37. The ripple measured at the switching frequency appears as expected. The output filter eliminates the ripple associated with the switching frequency, leaving only low amplitude spikes of noise that are due to the switch transitions.

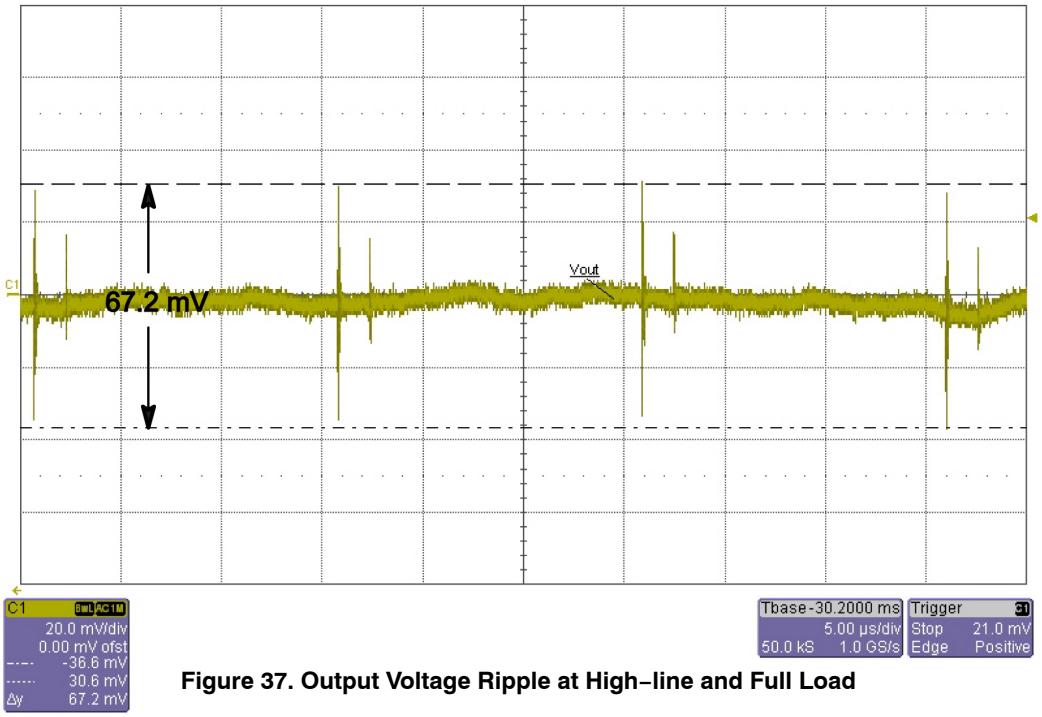

Figure 37. Output Voltage Ripple at High−line and Full Load

If the output ripple is observed on a longer time scale, a component of the NCP1219 frequency jitter is observed. The frequency jitter generated by the controller spreads the energy generated during switching, reducing electromagnetic interference, EMI. The bandwidth of the system is not high enough to prevent this component. This is shown in Figure 38. The output ripple due to the frequency jitter is still within the target limits.

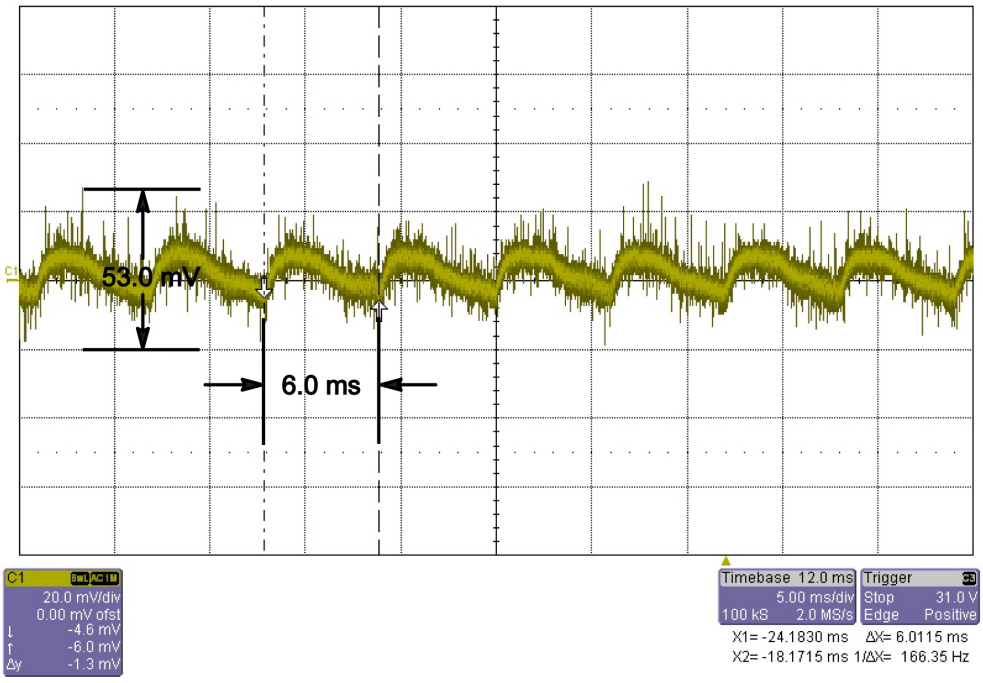

Figure 38. Frequency Jitter Component of Output Ripple at Nominal Load Current

The dynamic response of the converter at 24 V is evaluated stepping the load current from 0.92 A to 2.0 A and from 2.0 A to 0.92 A. The step load response is shown in Figure 39. The output response to the load step is measured as 150 mV, and recovery occurs in less than 5 ms. Response to the transient load condition confirms the results of the loop stability analysis.

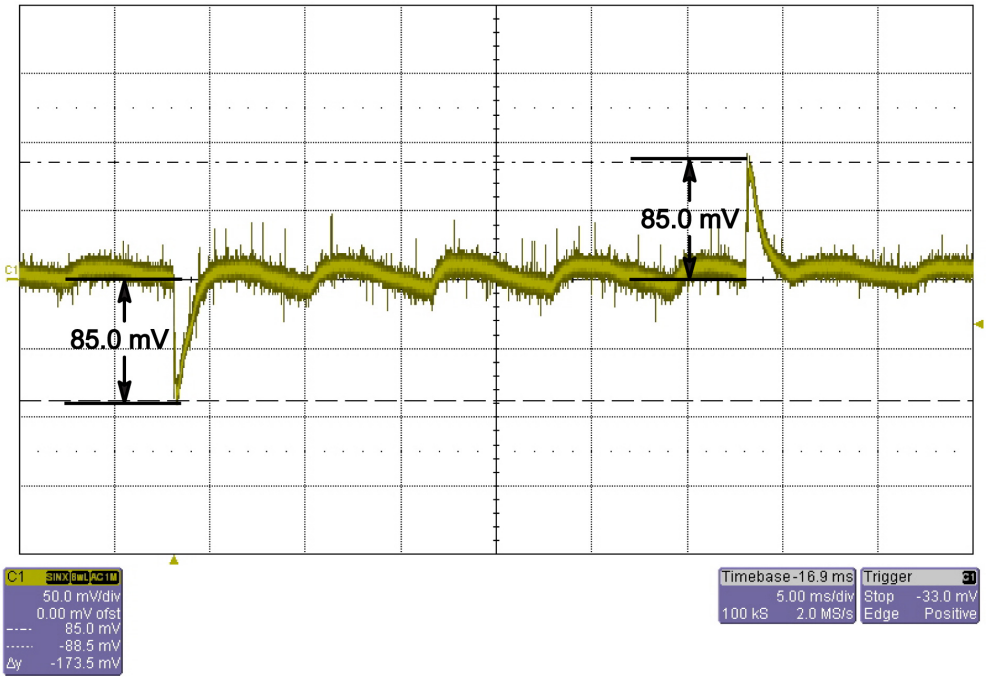

Figure 39. Output Voltage Response to a Step Load from 0.92 A to 2.0 A

The frequency jitter component of the output waveform previously described can be seen during the transient response measurement.

THERMAL PERFORMANCE

This demonstration board is designed to operate with out forced airflow as in an external printer power supply. The thermal performance of the board is evaluated using an infrared camera. Figures 40 through 43 show several images of the board during a continuous load step as described in Figure 1. Images include top and bottom layers at low and high line. All images were taken in open air conditions without forced airflow.

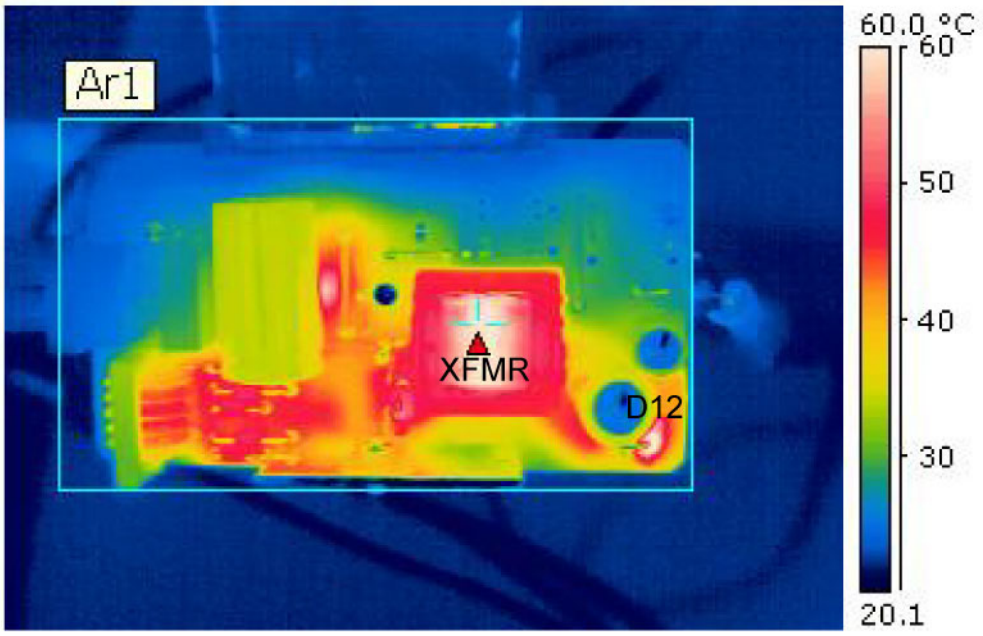

Figure 40. Thermal Image of the Top of the Board at Low Line During a Continuous Load Step Condition

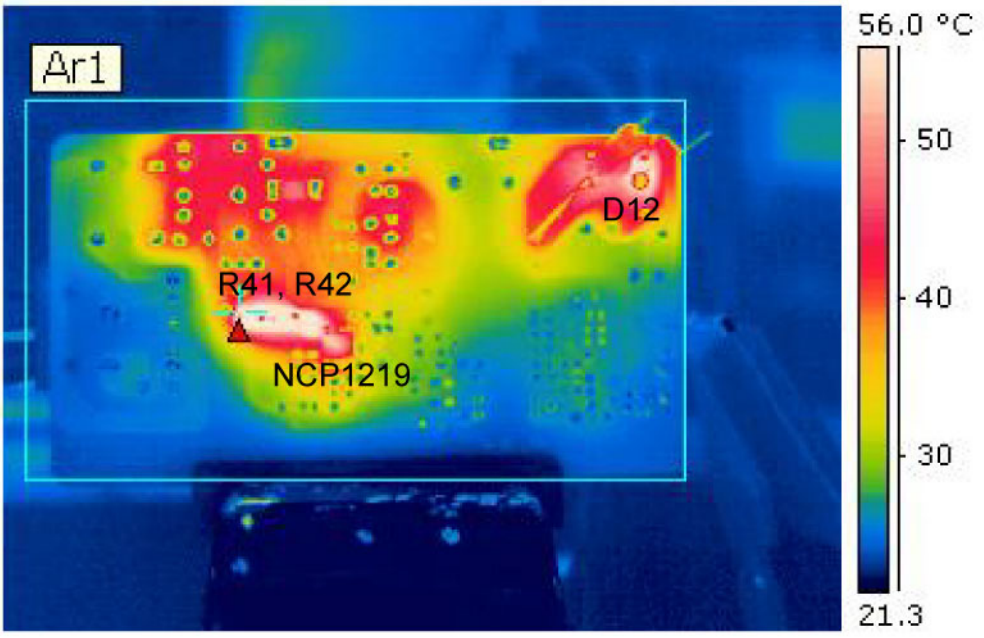

Figure 41. Thermal Image of the Bottom of the Board at Low Line During a Continuous Load Step Condition

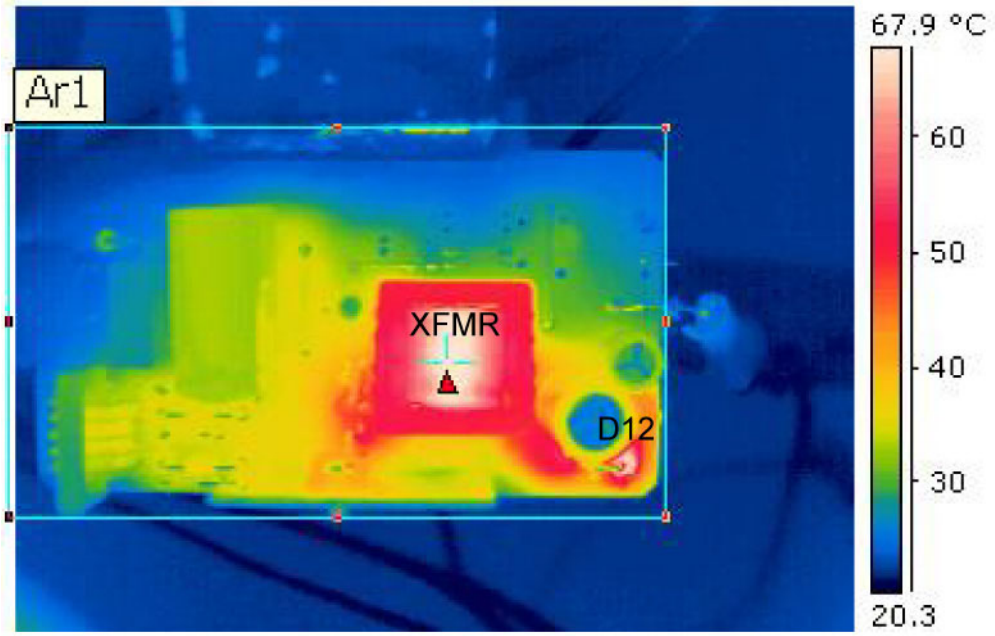

Figure 42. Thermal Image of the Top of the Board at High Line During a Continuous Load Step Condition

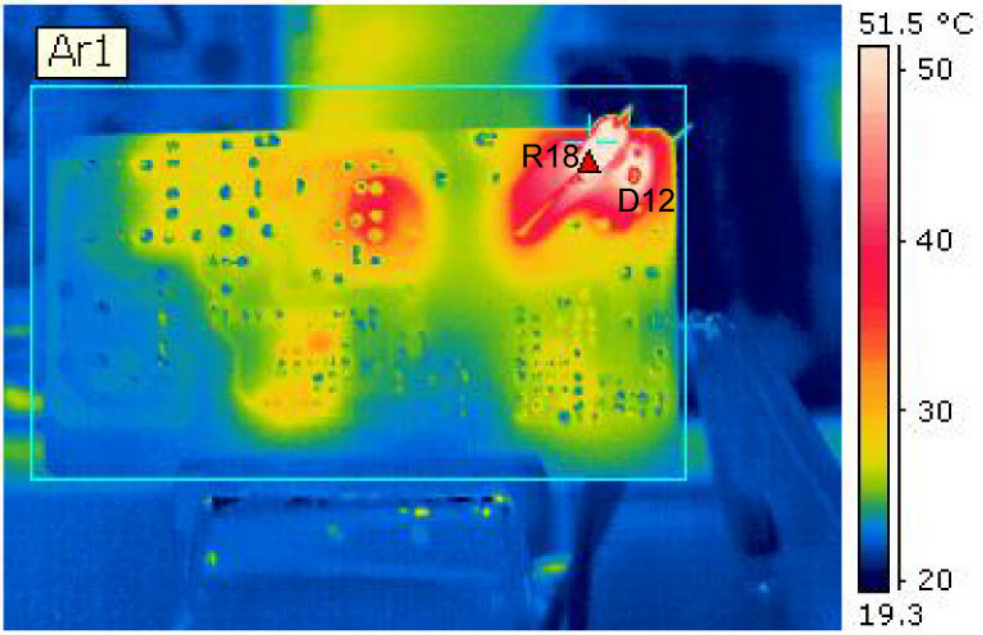

Figure 43. Thermal Image of the Bottom of the Board at High Line During a Continuous Load Step Condition

Most of the losses on the board are on the main switch, transformer, secondary rectifier (D12) and secondary snubber resistor (R18). The main switch losses are dominated by on state conduction losses, but the aluminum heat sink reduces the power dissipation in the device. High peak currents during the load step create heating in the transformer, as seen in Figures 40 and 42. The losses in D12 during load step conditions are shown in the lower right−hand corner of the board in Figures 40 and 42. The heat spreading from D12 can also be seen on the bottom side of the board. The secondary snubber is designed to prevent overvoltage stress on the secondary rectifier. The power dissipation in R18 occurs at high line conditions when the snubber acts to clamp the voltage on the diode, as seen in the upper right hand corner of the board. At low line, DSS mode is active and the power dissipation in the controller and the series HV resistors (R41 and R42) can be seen in Figure 41.

SUMMARY

A 30 W (48 W) converter is designed and built using the flyback topology. The converter is implemented using the NCP1219. The average load efficiency is measured above 83.5% over the complete operating range.

The standby input power is measured below 1 W under universal mains operating ranges. The low standby power is achieved using a forward auxiliary winding with DSS operating at low line conditions only. The converter complies with Energy Star 2.0 EPS requirements.

The converter provides excellent transient response by minimizing overshoot, undershoot, and recovery time. Output voltage ripple is measured at 16 mV. Phase margin and crossover frequency are measured at 60° and 1.3 kHz, respectively.

This demonstration board is designed to demonstrate the features and flexibility of the NCP1219. This design is a guideline only and does not guarantee performance for any manufacturing or production purposes.

REFERENCES

1. Basso, Christophe P. Switch−Mode Power Supplies SPICE Simulations and Practical Designs. 1st ed. New York, NY: MacGraw Hill.
2. Pressman, Abraham I. Switching Power Supply Design. 1st ed. New York, NY: MacGraw Hill.
3. PWM Controller with Adjustable Skip Level and External Latch Input Datasheet NCP1219, www.onsemi.com.

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