AND8366

AMIS−4168x Fault Tolerant Transceiver Design Considerations Using CANLSFT

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Introduction

The new AMIS−41682 and AMIS−41683 are interfaces between the protocol controller and the physical wires of the bus lines in a control area network (CAN). The AMIS−41683 is identical to the AMIS−41682 but has a true 3.3 V digital interface to the CAN controller. The device provides differential transmit capability but will switch in error conditions to a single−wire transmitter and/or receiver. Initially it will be used for low speed applications, up to 125 kB, in passenger cars.

Both AMIS−41682 and AMIS−41683 are implemented in I2T100 technology enabling both high−voltage analog circuitry and digital functionality to co−exist on the same chip.

This application note describes design considerations using AMIS−41682 and AMIS−41683 in low speed fault tolerant CAN networks conform to ISO 11898−3. More technical information can be found in:

- AMIS−41682 Datasheet (http://www.onsemi.com)
- ISO 11898−3 standard

Key Characteristics AMIS−41682 / AMIS−41683

Device Parameters

Table 1. KEY DEVICE PARAMETERS FOR THE AMIS−41682 AND AMIS−41683

Key	AMIS−41682	AMIS−41683
Current consumption in normal mode (I_{CC})	7 mA (recessive) 17 mA (dominant)	7 mA (recessive) 17 mA (dominant)
Current consumption in stand−by modes (I_{BAT} + I_{CC})	30 μA	30 μA
Minimum operating voltage	5 V	5 V
Prevention of V_{BAT} reverse current	Yes	Yes
WAKE−B sensitivity	Both edges	Both edges
True 3.3 V microcontroller interface	No	Yes
NERR reporting of open failures	During frame and inter frame space	During frame and inter frame space

System Parameters

Table 2. KEY SYSTEM PARAMETERS FOR THE AMIS−41682 AND AMIS−41683

Key	AMIS−41682/3
System Size	≤ 32 nodes
Speed	40 – 125 kbps
Emission	++
Immunity	++
TxD dominant monitoring	yes
Extended bus failure management (including Failure 3a CANH to V_{CC})	yes
Resolved problem of arbitration across open failures	yes

Pullup Resistors AMIS−41683

To interface with true 3.3 V microcontrollers AMIS−41683 has open drain outputs for RxD and ERR−B. To calculate the pullup resistor two considerations are important:

- A too high resistance value will create extra delay when charging the equivalent input capacitance Ci (see Figure 1).
- A too low resistance will negatively influence the V_{OL} level.

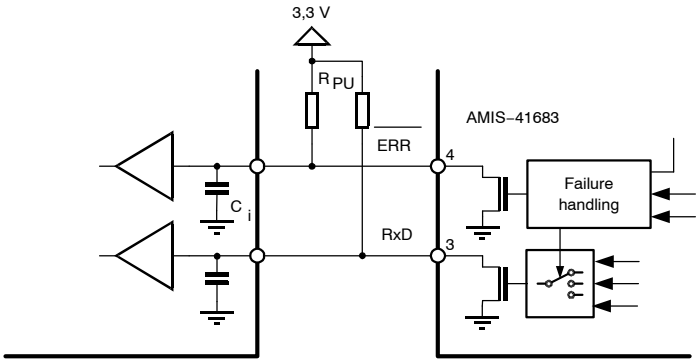


Figure 1. Pullup Resistor to Interface with True 3.3 V Microcontrollers

Calculating R_{PU} for Minimum Propagation Delay

The extra delay can be seen as the time needed to charge $\mathbf{C}_i$ up to 70% of the 3.3 V supply. This is given by:

$$t_{delay} = 1.2 * R_{PU} * C_i \qquad \text{(eq. 1)}$$

The typical propagation delay can be found in the data sheet and is given in Table 3.

Table 3. PROPAGATION DELAY

Symbol	Parameter	AMIS−41683
$t_{PD(H)}$	Typical propagation delay TxD to RxD (high)	750 ns

Assuming that this delay is symmetrical between TxD to BUS and BUS to RxD and that the extra delay should be less than 10% gives $\mathbf{t}_{delay} < 37$ ns. Calculating further with $\mathbf{C}_i = \mathbf{C}_{input} + \mathbf{C}_{interconnect}$ = 3.5 pF + 3.0 pF = 6.5 pF in Equation 1 yields in:

$$R_{PU} = \frac{t_{delay}}{(1.2 * C_i)} \qquad \text{(eq. 2)}$$

$$R_{PU} = \frac{37 \text{ ns}}{(1.2 * 6.5 \text{ pF})} = 4.74 \text{ k}\Omega \qquad \text{(Res.1)}$$

Verifying R_{PU} for Maximum V_{OL}

The maximum sink current when RxD or ERR−B are pulled low via the open drain outputs of the AMIS−41683 is given by:

$$I_{SINK} = \frac{3.3 \text{ V}}{4.74 \text{ k}\Omega} = 696 \ \mu\text{A} \qquad \text{(Res.2)}$$

This current is far below the maximum I_{sink} = 1.6 mA to guarantee a $\mathbf{V}_{OL} < 0.4$ V as can be seen in the data sheet and in Table 4.

Table 4. OUTPUT LOW LEVEL OF THE OPEN−DRAIN OUTPUTS RXD AND ERR−B

Symbol	Parameter	AMIS−41683
$V_{OL,max}$	Low level output voltage @ I_{sink} = 1.6 mA	< 0.4 V

Series Resistor at Pin BAT

The optional resistor R_{BAT} gives the AMIS−41682/3 additional protection against automotive transients (ISO 7637 part 5). It is not really needed because the high voltage part of the circuit is designed to withstand these high energetic pulses.

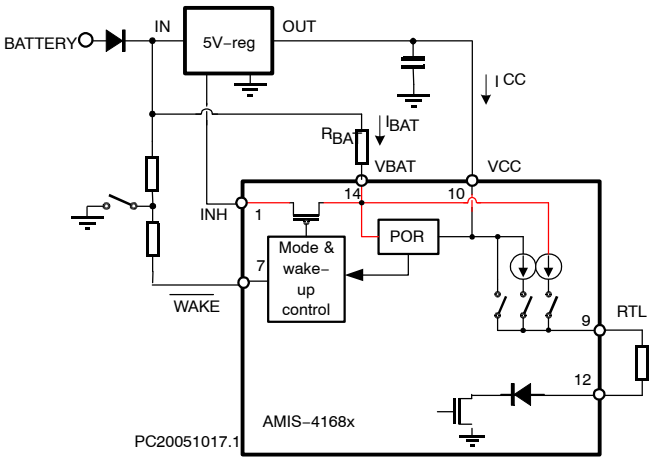


Figure 2. Connection via R_{BAT} to V_{BAT} Indication of Currents

The higher this series resistor the better the protection. However bigger series resistance results in a higher voltage drop thus increasing minimum operating battery voltage. To calculate this drop the maximum current consumption from V_{BAT} in normal and low power mode needs to be determined.

Normal Mode

In normal mode the maximum voltage drop over $\mathbf{R}_{BAT}$ is given by:

$$V_{DROPN} = R_{BAT} * I_{BAT} \quad \text{(eq. 3)}$$

Calculating with $\mathbf{R}_{BAT}$ = 1 kΩ the parameters from copied from the AMIS−41682/3 data sheets yields in:

$$V_{DROPN} = 1\ k\Omega * 230\ \mu A = 230\ mV \quad \text{(Res.3)}$$

Low Power Mode

In low power mode the maximum voltage drop over $\mathbf{R}_{BAT}$ is given by:

$$V_{DROPLP} = R_{BAT} * \left(I_{BAT} + I_{CC} + I_{RTL}\right) \quad \text{(eq. 4)}$$

Calculating with $\mathbf{R}_{BAT}$ = 1 kΩ the parameters from copied from the AMIS−41682/3 data sheets yields in:

$$V_{DROPN} = 1\ k\Omega * \left(60\ \mu A + 1.25\ mA\right) = 1.31\ V \quad \text{(Res.4)}$$

Conclusion

This shows that specifically in low power mode the voltage drop is relatively high due to the high output current on the RTL pin. For $\mathbf{R}_{BAT}$ = 1 kΩ the minimum operating battery voltage is increased with 1.31 V. For $\mathbf{R}_{BAT}$ = 2 kΩ this is almost an increase of 2.6 V leading to $\mathbf{V}_{BAT,min}$ = 7.6 V. If a very low minimum operating voltage is required, $\mathbf{R}_{BAT}$ can be eliminated. In all other cases $\mathbf{R}_{BAT}$ should be < 2 kΩ.

Table 5. MOST IMPORTANT PARAMETERS TO CALCULATE R_{BAT}

Symbol	Parameter	AMIS−41682/3
V_{BAT}	Minimum operating voltage at V_{BAT} supply pin	5 V
I_{BAT}	Max current in pin V_{BAT} (5 V to 36 V) in all modes of operation	230 μA
I_{BAT} + I_{CC}	Max current in pin V_{BAT} (5 V to 36 V) and V_{CC} in low power mode	60 μA
I_{RTL}	Maximum RTL current in low power modes	1.25 mA

V_{CC} Supply and Recommended Buffer Capacitance

Introduction

Two types of V_{CC} supply topologies can be recognized. For 5 V microcontrollers, in most cases, a common V_{CC} power supply is used for both the microcontroller and the AMIS−41682. (See Figure 1). In case of a 3.3 V microcontroller a separate V_{CC} supply is needed for the AMIS−41683 independently from the microcontroller. (See Figure 2).

Depending on the used topology the dimensioning of the buffer capacitor and the power dissipation in the voltage regulator will differ.

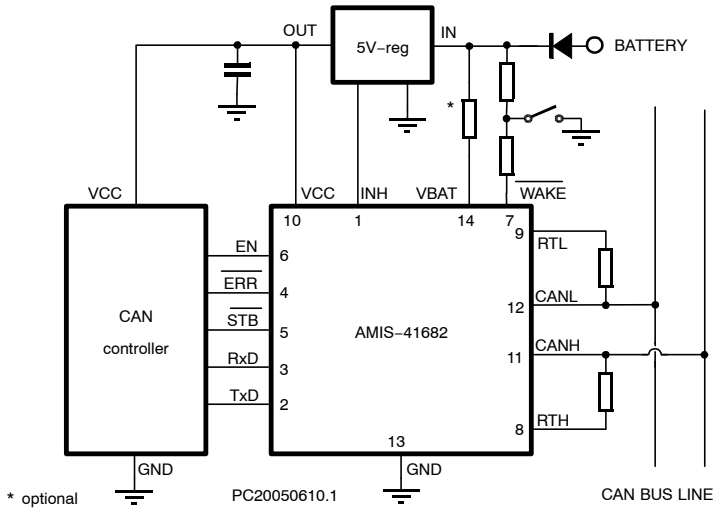


Figure 3. Single V_{CC} Topology for 5 V Microcontroller

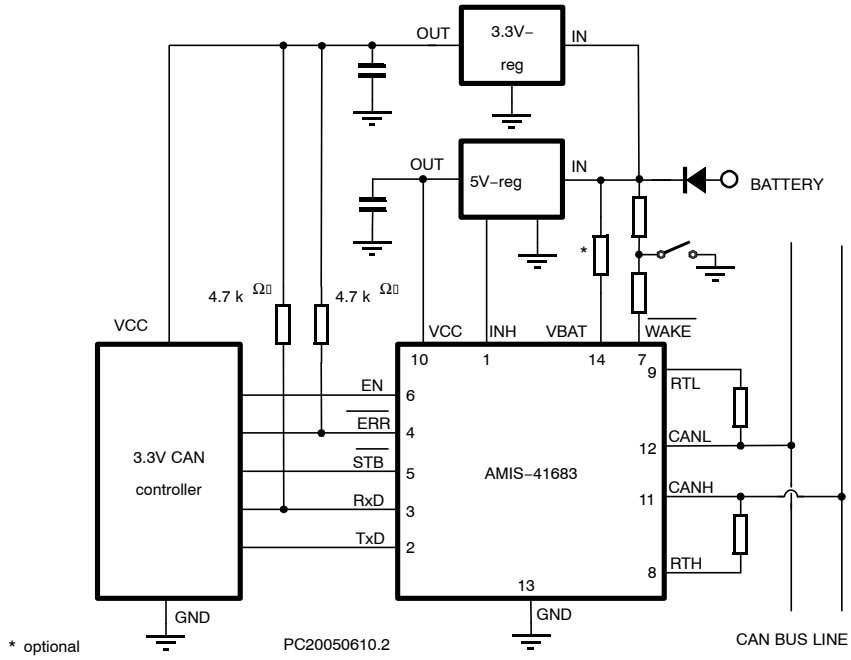


Figure 4. Dual V_{CC} Topology for 3.3 V Microcontroller

Calculation

For calculating the power dissipation in the voltage regulator the average current consumption is important. For dimensioning the buffer capacitor the peak current and the peak duration time is of importance. gives an overview of the calculated values discussed further in this document.

The average supply current is needed to calculate the thermal load of the required V_{CC} voltage regulator. The peak supply current may flow in case of certain bus failure conditions for a certain time and thus has an impact on the power supply buffering.

The V_{CC} supply of the transceiver is recommended to support the characteristics as follows:

Table 6. OVERVIEW OF THE CALCULATED V_{CC} SUPPLY CURRENTS

Symbol	Parameter	Condition	AMIS−41682/3
I_{CC,av_NF}	Average V_{CC} supply current	No bus failure	31.15 mA
I_{CC,av_SF}	Average V_{CC} supply current	Single bus failure	66.15 mA
I_{CC,pk_SF}	Peak V_{CC} supply current	Single bus failure	126 mA
t_{SINGLE}	Over current duration	Single bus failure	< 6 Tbit
I_{CC,pk_DF}	Peak V_{CC} supply current	Dual bus failure	127 mA
t_{DOUBLE}	Over current duration	Dual bus failure	< 17 Tbit

In the following, these two cases are discussed in more detail.

Calculating the Average Supply Current Without Bus Failure Condition

The average supply current is determined by the current consumption in the recessive state $\mathbf{I_{cc\_rec}}$ as listed in the datasheet and the current consumption in dominant state. The latter is the sum of the corresponding supply current $\mathbf{I_{cc0\_dom}}$, the bus current $\mathbf{I_{CANH\_dom}}$ and the current in the termination resistor $\mathbf{I_{CANH\_dom}}$.

The maximum dominant supply current (without bus wiring faults) is given by:

$$I_{CC\_dorm} = I_{CC0\_dom} + I_{CANH\_dom} + I_{RTL\_dom} \quad \text{(eq. 5)}$$

$$I_{RTL\_dom} = \frac{\left(V_{CC} - V_{CANL\_dom}\right)}{R_T} \quad \text{(eq. 6)}$$

Calculating with the given parameters in Table 7.

Table 7. MOST IMPORTANT PARAMETERS TO CALCULATE THE MAXIMUM I_{OC} IN DOMINANT STATE

Symbol	Parameter	AMIS−41682/3
I_{CC0_dom}	Max. V_{CC} supply current dominant, no load	12 mA
I_{CANH_dom}	Assumed CANH dominant current	40 mA
R_T	Assumed termination resistor	1 kΩ
V_{CANL_dom}	Assumed CANL dominant voltage	1 V

Yields in:

$$I_{CC\_dom} = 12\ mA + 40\ mA + \frac{\left(5\ V - 1\ V\right)}{1\ k\Omega} = 56\ mA\ max. \quad \text{(Res.5)}$$

The maximum recessive supply current (without bus wiring faults) is given by the parameters in Table 8:

Table 8. MAXIMUM I_{CC} IN RECESSIVE STATE

Symbol	Parameter	AMIS−41682/3
I_{CC_rec}	Maximum V_{CC} supply current recessive, no load	6.3 mA

For thermal considerations the average supply current at pin V_{CC} is relevant considering the transmit duty cycle. The worst case condition is a continuously transmitting node. With an assumed transmit duty cycle of 50% on pin TxD, the maximum average supply current is:

$$I_{CC\_nom\_avg} = 0.5 * \left(I_{CC\_rec} + I_{CC\_dom}\right) \quad \text{(eq. 7)}$$

Using the parameter in and result (Res 5) in Equation 7 yields in:

$$I_{CC\_nom\_avg} = 0.5 * \left(6.3\ mA + 56\ mA\right) = 31.15\ mA\ max. \quad \text{(Res.6)}$$

Supply Currents With Single Bus Failure Condition

Average Supply Current in Single Fault Condition

The average supply current is determined by the current consumption in the recessive state $\mathbf{I_{cc\_rec}}$ as listed in the datasheet and the worst case current consumption in dominant state. The latter is the sum of the corresponding supply current $\mathbf{I_{cc0\_dom}}$, the bus current when CANH is shorted to ground $\mathbf{I_{CANH\_\ sc1\_dom}}$ and the current in the termination resistor $\mathbf{I_{CANH\_dom}}$.

The maximum dominant supply current (with SINGLE bus wiring faults CANH shorted to GND) is given by:

$$I_{CC\_sc1\_dom} = I_{CC0\_dom} + I_{CANH\_sc1\_dom} + I_{RTL\_dom} \quad \text{(eq. 8)}$$

Calculating with the given parameters in Table 9:

Table 9. MAXIMUM DOMINANT CURRENT IN CASE OF A SHORT CIRCUIT IN THE CANH PIN

Symbol	Parameter	AMIS−41682/3
$I_{CANH\_sc1\_dom}$	CANH dominant current, short circuit	110 mA

Yields in:

$$I_{CC\_sc1\_dom} = 12\ mA + 110\ mA + \frac{(5\ V - 1\ V)}{1\ k\Omega} = 126\ mA\ max. \quad (Res.7)$$

For thermal considerations the average supply current at pin V_{CC} is relevant considering the transmit duty cycle. The worst case condition is a continuously transmitting node. With an assumed transmit duty cycle of 50% on pin TxD, the maximum average supply current is:

$$I_{CC\_sc1\_avg} = 0.5 * \left(I_{CC\_rec} + I_{CC\_sc1\_dom}\right) \quad (eq.\ 9)$$

Using the parameter from and and result (Res 7) in Equation 9 yields in:

$$I_{CC\_sc1\_avg} = 0.5 * (6.3\ mA + 126\ mA) = 66.15\ mA\ max. \quad (Res.8)$$

Extra Supply Current in Single Fault Condition

Compared to the quiescent current in recessive state the maximum **extra** supply current when the CANH driver is turned on with CANH shorted to GND is needed to calculate the required worst case V_{CC} buffer capacitance. This extra supply current has to be buffered for up to 6−bit times. This 6−bit time limitation is set by the CAN controller which is supposed to send an error flag within this timing window.

$$\Delta I_{CC\_sc1} = I_{CC\_sc1\_dom} - I_{CC\_rec,min} \quad (eq.\ 10)$$

The minimum recessive supply current is given by the parameter in Table 10.

Table 10. V_{CC} MINIMUM CURRENT CONSUMPTION IN RECESSIVE STATE

Symbol	Parameter	AMIS−41682/3
$I_{CC\_rec,min}$	Min. V_{CC} supply current recessive, no load	1 mA

Using the parameter in and result (Res 7) in Equation 10 yields in:

$$\Delta I_{CC\_sc1} = 126\ mA - 1\ mA = 125\ mA\ max. \quad (Res.9)$$

Worst−Case Max V_{CC} Supply at Presence of a Dual Short Circuit

The worst case maximum V_{CC} supply current is flowing in case of a **dual short−circuit** of the bus. In this case the bus−lines CAN_H and CAN_L are shorted to ground and no communication is possible. Nevertheless the application supply should be able to deliver a proper V_{CC} for the microcontroller in order to prevent erroneous operation. For the calculation of the buffer capacitor we need to distinguish between the two supply topologies:

If there is a **separate** voltage regulator available supplying the transceiver exclusively (see Figure 5), **no care** has to be taken on this dual short circuit condition. If the voltage regulator enters the over−current protection level and its output will drop to limit the internal power dissipation, this under−voltage condition will only affect the function of the transceiver. The microcontroller is still powered properly by its own supply.

In case of a **shared** voltage supply for transceiver and microcontroller, this dual fault condition is relevant to dimension the required buffer capacitor.

Max V_{CC} Supply Current in Worst−Case Dual Fault Condition

$$I_{CC\_sc2\_dom} = I_{CC0\_dom} + I_{CANH\_sc1\_dom} + I_{RTL\_sc\_dom} \quad (t < 17\ bit\ times) \quad (eq.\ 11)$$

$$I_{RTL\_sc\_dom} = \frac{V_{CC}}{2} \quad (eq.\ 12)$$

The 17−bit time−out limitation is determined by the CAN protocol. Due to the dual fault condition with CANH and CANL shorted to GND the RxD pin of the transceiver is continuously clamped recessive (CANL to GND forces CANH operation; CANH is clamped recessive).

The moment the CAN controller starts a transmission, this dominant start of frame bit is not fed back via RxD and thus forces an error flag due to the bit failure condition (TX error counter increment by 8). This first bit of the error flag again is not reflected at RxD and forces the next error flag (TX error counter + 8).

Latest after 17 bit times, depending on the TX error counter level before starting this transmission, the CAN controller reaches the error passive limit (128) and stops sending dominant bits. Now a sequence of 25 recessive bits follows (8 bit error delimiter + 3 bit intermission + 8 bit suspend transmission) and the V_{CC} current becomes reduced to the recessive one. From now on only single dominant bits (start of frame) followed by 25 recessive bits (passive error flag + intermission + suspend transmission) are output until the CAN controller enters the bus off state.

So, for dimensioning the V_{CC} voltage source in this worst case dual failure scenario, up to 17 bit times might have to be buffered by a buffer capacitor depending on the regulation capabilities of the used voltage supply.

Using the parameters from and in Equations 11 and 12 yields in:

$$I_{CC\_sc2\_dom} = 12\ mA + 110\ mA + 5\ V/1\ k\Omega = 127\ mA \quad (Res.10)$$

V_{CC} Extra Supply Current in Dual Fault Condition

Compared to the quiescent current in recessive state the maximum **extra** supply current when the CANH driver is

turned on in dual short−circuit condition is needed to calculate the required worst case V_{CC} buffer capacitance. This extra supply current has to be buffered for that time the applications voltage regulator needs to react.

$$\Delta I_{CC\_sc2} = I_{CC\_sc2\_dom} - I_{CC\_rec,min} \quad \text{(eq. 13)}$$

Using the parameter in and result (Res 10) in Equation (13) yields in:

$$\Delta I_{CC\_sc2} = 127\ mA - 1\ mA = 126\ mA\ max. \quad \text{(Res.11)}$$

Calculation of Worst−Case Buffer Capacitor

Depending on the power supply topology, the required worst−case buffer capacitor can be calculated.

In case of a **separate V_{CC}** supply for the transceiver only, the extra supply current **ΔI_{CC_sc1}** in case of the **single fault condition** has to be taken with a maximum of six dominant bit times.

$$C_{BUFF} = \Delta I_{CC\_sc1} * \frac{t_{dom\_max}}{\Delta V_{max}} \quad \text{(eq. 14)}$$

In case of a **shared V_{CC}** supply for transceiver and microcontroller, the extra supply current **ΔI_{CC_sc2}** in case of the **dual fault condition** has to be taken with a maximum of 17 dominant bit times.

$$C_{BUFF} = \Delta I_{CC\_sc2} * \frac{t_{dom\_max}}{\Delta V_{max}} \quad \text{(eq. 15)}$$

Important remarks:

- The buffer capacitor **C_{BUFF}** is calculated assuming the voltage regulator is **not** able to deliver any extra current within the maximum dominant output drive **t_{dom_max}** during the dual fault condition due to bandwidth limitations of the regulator.
- The voltage drop over the capacitor is assumed to be less than 5%. In the graphs also 7% and 9% are plotted.

C_{BUFF} Calculation for Separate Supplied Transceiver

In case of a separate transceiver supply the buffer capacitance has to be calculated based on the single fault condition with CANH shorted to GND. Here the dual fault is not relevant.

Assuming a communication speed of 100kBit/s gives:

$$t_{dom\_max} = 6 * 10\ \mu s = 60\ \mu s \quad \text{(Res.12)}$$

Maximum allowed V_{CC} voltage drop of 5% yields in:

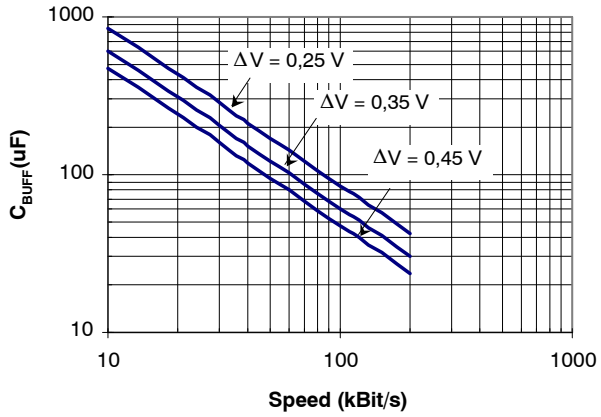
$$\Delta V_{max} = 0.25\ V \quad \text{(Res.13)}$$

Using the results (Res 9), (Res 12) and (Res 13) in Equation (14) yields in:

$$C_{BUFF} = 125\ mA * 60\ \mu s / 0.25\ V = 30\ \mu F \quad \text{(eq. 16)}$$

For different communication speeds and allowed voltage drop, **C_{BUFF}** can be looked up in the graph in Figure 5.

C_{BUFF} at double fault



C_{BUFF} at single fault

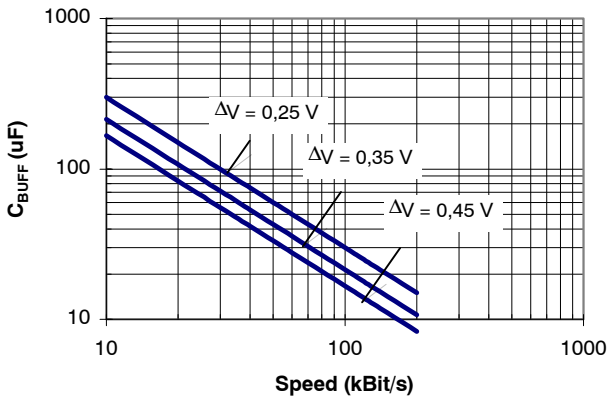


Figure 5. Needed V_{CC} Buffer Capacitor for Single and Double Bus Failure

C_{BUFF} Calculation for Shared Supply

In case of a shared supply concept the buffer capacitance has to be calculated based on the worst case dual fault condition in order to keep the micro−controller supply within the operating range:

Assuming a communication speed of 100 kBit/s gives:

$$t_{dom\_max} = 17 * 10\ \mu s = 170\ \mu s \quad \text{(Res.14)}$$

Maximum allowed V_{CC} voltage drop of 5% yields in:

$$\Delta V_{max} = 0.25\ V \quad \text{(Res.15)}$$

Using the results (Res 11), (Res 14) and (Res 15) in Equation 15 yields in:

$$C_{BUFF} = 126\ mA * 170\&\mu s / 0.25\ V = 85.7\ \mu F \quad \text{(Res.16)}$$

For different communication speeds and allowed voltage drop, **C_{BUFF}** can be looked up in the graphs plotted in Figure 5.

Calculation of Bus Termination Resistors and EMC Issues

How to Dimension the Bus Termination Resistor Values – Some Basic Rules

The termination is provided by connecting the CANL line to the R_{TL} pins of the transceiver devices and by connecting the CANH line to the R_{TH} pins. By connecting the termination pins the following requirements have to be considered:

- The overall network termination resistor of one line (all parallel resistors connected to RTL or RTH pins) shall be about 100 Ω, due to in circuit current limitations and CAN voltage definitions.
- A single resistor connected to an individual transceiver device shall not be below 500 Ω, due to in circuit current limitations.

It is recommended, that every node provides its own termination resistors. However this is not a strict requirement. A not well terminated node might be sensitive for false wake up signals, if a broken line error had occurred.

Depending on the number of nodes in the network the local termination resistors can be calculated as:

$$R_{TL} = n * 100\ \Omega \text{ and } R_{TH} = n * 100\ \Omega \quad \text{(eq. 17)}$$

Where n = number of nodes

If the number of nodes is smaller than five the network termination is limited to 500 Ω. This will lead to a non optimal line termination, but in small networks this is not considered as a problem.

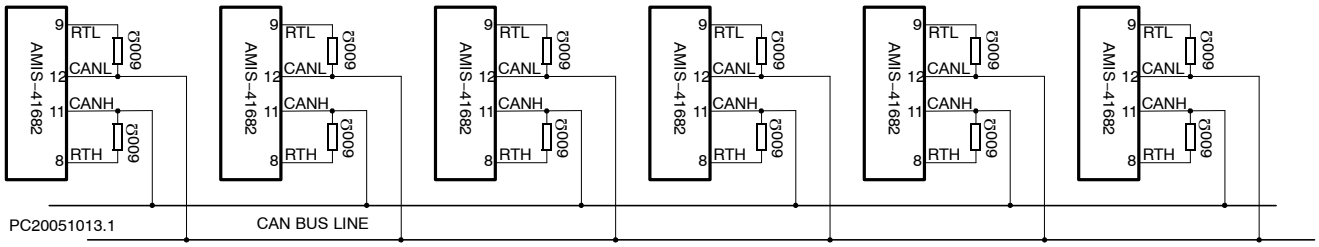


Figure 6. Example Network with Six Nodes, 600 Ω Termination at Each Node

Tolerances of Bus Termination Resistors – EMC Considerations

The symmetry of the termination resistors within a single node has a major impact to the systems electromagnetic emission (EME) behavior. Thus it is important to have well matched termination resistors within each control unit. This means that the $\mathbf{R}_{TH}$ resistor should have exactly the same value compared to the $\mathbf{R}_{TL}$ resistor within one control unit in order to get the same time constant on each bus wire during signal transitions. The tolerance between two different control units is absolutely insignificant.

The principle to achieve a good EME performance is that the differential signal on the bus wires eliminates any emission due to compensation effects if both CAN wires are carrying exactly the same signal, but with inverse polarities.

Here the transceiver can only provide a perfect symmetry for the dominant transitions by design. The recessive transitions are mainly driven by the termination resistors and the network cables itself. So not only the transceiver's output drivers have an impact to the EME performance but also the termination and the cable symmetry.

It is obvious that also the layout of printed circuit boards has a significant impact to the EMC behavior if the CAN lines have different capacitive loads due to different wire lengths.

It is recommended to provide a termination resistor accuracy ($\mathbf{R}_{TH}$ compared to $\mathbf{R}_{TL}$) within the same node of 1% or lower. Also the bus cable has to be at least a twisted pair cable in order to achieve a symmetrical capacitive load for both bus wires resulting in a good EMC performance.

Power Dissipation of Bus Termination Resistors R_T

Average Power Dissipation – No Bus Failures

To determine the average power dissipation of the termination resistors, the average time between dominant and recessive bits has to be taken into account. Additionally a worst case ground shift is contributing to additional dissipation.

The power dissipation in recessive state is $\mathbf{P_{rec}} = 0$ because there is no voltage drop across the termination resistor.

In dominant state the dissipation is given by:

$$P_{dom} = \frac{\left(V_{CC} + V_{GND}\right)^2}{R_T} \quad \text{(eq. 18)}$$

CAN frames are assumed to have a worst case ratio of dominant bits in the range of 0.75. This results in an average power dissipation calculated as follows:

$$P_{avg} = 0.25\, P_{rec} + 0.75\, P_{dom} = \frac{\left(0.75 * \left(V_{CC} + V_{GND}\right)\right)^2}{R_T} \quad \text{(eq. 19)}$$

Assuming R_T = 1 kΩ and a worst case ground shift of $\mathbf{V_{GND}}$ = 1.5 V yields in:

$$P_{avg} = \frac{(0.75 * (5\ V + 1.2\ V))^2}{1\ k\Omega} = 23.7\ mW \quad \text{(Res.17)}$$

Maximum Peak Power Dissipation

In case of a bus failure (CANH to V_{BAT}) a peak current will flow in the termination resistor. However the duration is limited because after the maximum Failure Detection Time the termination resistor will be disabled from the circuit. The peak power can be calculated as:

$$P_{peak} = \frac{V_{BAT,max}{}^2}{R_T} \left(\text{with duration } < t_{det}\right) \quad \text{(eq. 20)}$$

The maximum failure detection time is given by the parameter in Table 11:

Table 11. MAXIMUM FAILURE DETECTION TIME

Symbol	Parameter	AMIS−41682/3
t_{det}	Failure Detection time	80 ms

Calculating with data from , $\mathbf{R}_T$ = 1 kΩ and $\mathbf{V}_{BAT}$ = 27 V

$$P_{peak} = \frac{(27\ V)^2}{1\ k\Omega} = 730\ mW \text{ for less than } 8\ ms$$
$$E_{peak} = 5.84\ mJ \quad \text{(Res.18)}$$

Because the energy E_{peak} is very limited, this peak power dissipation can be neglected.

Table 12. GLOSSARY

Symbol	Description
I_{cc_dom}	Supply current at pin V_{CC} while driving a dominant bit **with** a certain load to the pins
I_{cc0_dom}	Supply current at pin V_{CC} while driving a dominant bit **without** any load to the pins
I_{CANH_dom}	Output current of pin CANH while driving a dominant bit with nominal bus load of 100 Ω in total
I_{RTL_dom}	Output current of pin RTL while driving a dominant bit with a certain load
I_{cc_rec}	Supply current at pin V_{CC} while driving a recessive bit
$I_{cc\_norm\_avg}$	Average supply current at pin V_{CC} assuming no bus failure and continuous sending
$I_{cc\_sc1\_dom}$	Supply current at pin V_{CC} driving a dominant bit while CANH is shorted to GND
$I_{CANH\_sc1\_dom}$	Output current of pin CANH driving a dominant bit while CANH is shorted to GND
$I_{cc\_sc1\_avg}$	Average supply current at pin V_{CC} assuming CANH shorted to GND and continuous sending
ΔI_{cc_sc1}	Supply current change at pin V_{CC} in case a dominant bit is driven while CANH is shorted to GND
$I_{cc\_sc2\_dom}$	Supply current at pin V_{CC} driving a dominant bit while CANH **and** CANL are shorted to GND
$I_{RTL\_sc\_dom}$	Output current of pin RTL while driving a dominant bit with CANL shorted to GND
ΔI_{cc_sc2}	Supply current change at pin V_{CC} in case a dominant bit is driven while CANH and CANL are shorted to GND
V_{CC}	Supply voltage at pin V_{CC}
V_{CANL_dom}	Voltage level on CANL while a dominant bit is driven
R_T	Termination resistor connected to pins RTL and RTH
t_{dom_max}	Maximum possible continuous dominant drive time
ΔV_{max}	Maximum allowed voltage change at pin V_{CC}
C_{BUFF}	Required buffer capacitance in case the voltage regulator does not deliver extra current within t_{dom_max}
$t_{PD(H)}$	Typical propagation delay TxD to RxD (High)
C_i	Input capacity seen from the open drain outputs
R_{PU}	Pull up resistor 3.3 V open drain output
$V_{OL,max}$	Maximum low level output voltage
I_{SINK}	Sink current in open drain output
R_{BAT}	Series resistor in V_{BAT} connection
V_{DROPN}	Voltage drop over V_{BAT} series resistor in Normal mode
V_{DROPLP}	Voltage drop over V_{BAT} series resistor in Low Power mode
V_{BAT}	Minimum operating voltage at V_{BAT} supply pin
I_{BAT}	Max current in pin V_{BAT} (5 to 36 V) in all modes of operation

Table 12. GLOSSARY

Symbol	Description
$I_{BAT} + I_{CC}$	Max current in pin V_{BAT} (5 to 36 V) and V_{CC} in low power mode
I_{RTL}	Maximum RTL current in low power modes
I_{CC,av_NF}	Average V_{CC} supply current
I_{CC,av_SF}	Average V_{CC} supply current
I_{CC,pk_SF}	Peak V_{CC} supply current
t_{SINGLE}	Overcurrent duration
I_{CC,pk_DF}	Peak V_{CC} supply current
t_{DOUBLE}	Over current duration
I_{CC,av_NF}	Average V_{CC} supply current
R_{TH} ,R_{TL}	CAN bus termination resistors
t_{det}	Failure detection time
P_{avg}	Average power dissipation in CAN bus termination resistors
P_{peak}	Peak power dissipation in CAN bus termination resistors
E_{peak}	Peak energy in CAN bus termination resistors

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

AND8366/D