AND8355/D

Characteristics of Interleaved PFC Stages

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APPLICATION NOTE

Overview

Interleaved PFC is an emerging solution that becomes particularly popular in applications where a strict form factor has to be met like for instance, in slim notebook adapters or in LCD TVs. This section will consider the interleaving of two (Frequency Clamped) Critical conduction Mode PFC stages that efficiently address wide mains applications above 200 W. Interleaving Continuous Conduction Mode (CCM) PFC stages is also possible. However this option should be devoted to much higher power applications (above 1 kW) and will not be detailed here.

The main goal of this paper is to give the main characteristics and merits of this approach. In particular, this application note focuses on the current ripple reduction when the interleaved stages are operated out-of-phase and on the design criteria when dimensioning the power components. This theoretical analysis matches the experimental data that can be obtained in a practical 300 W, universal line application as reported by NCP1631EVB [1].

Introduction

Interleaving consists in paralleling two “small” stages in lieu of a bigger one, which may be more difficult to design. Practically, two 150 W PFC stages are combined to form our 300 W PFC pre-regulator. This approach has several merits like the ease of implementation, the use of more but smaller components or a better heat distribution.

Also, Interleaving extends the power range of Critical Conduction Mode (CrM) that is an efficient and cost-effective technique (no need for low t_{rr} diodes). Even, as reported by NCP1631EVB [1], when associated to the Frequency Clamped Critical conduction Mode (FCCrM), this technique yields particularly high efficiency levels (above 95% over a large load range at 90 V_{rms} in a 300 W application).

Furthermore, if the two stages are operated out-of-phase, we will see that the current ripple is significantly reduced. In particular, the input current looks like that of a Continuous Conduction Mode (CCM) one and the rms current within the bulk capacitor is dramatically reduced.

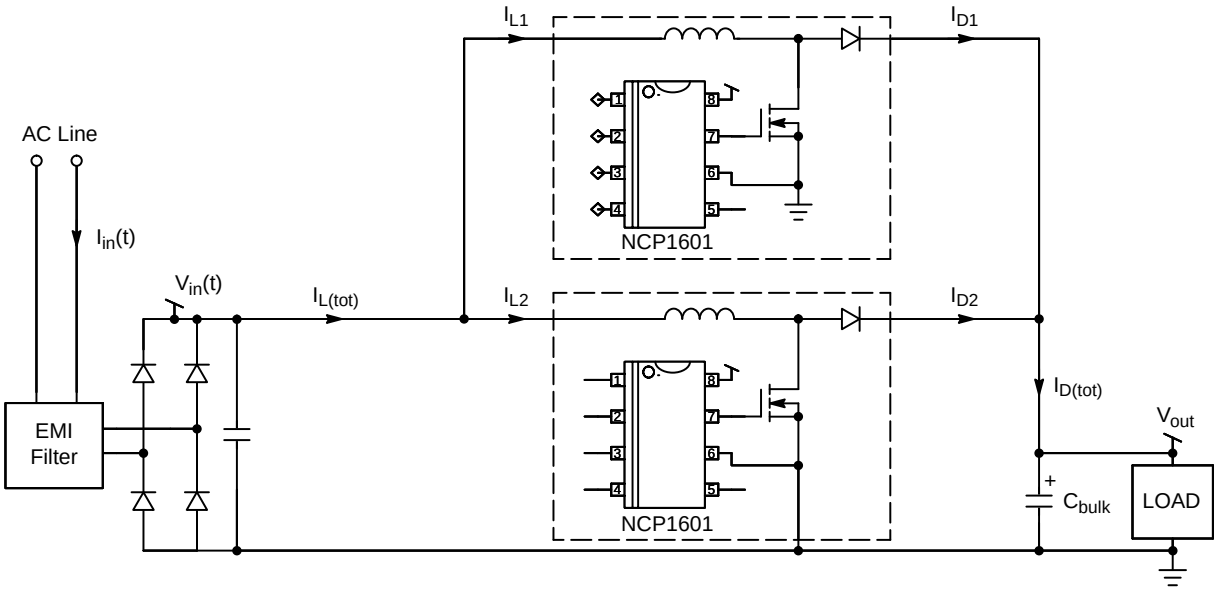

Figure 1. Schematic of an Interleaved PFC Driven by Two NCP1601

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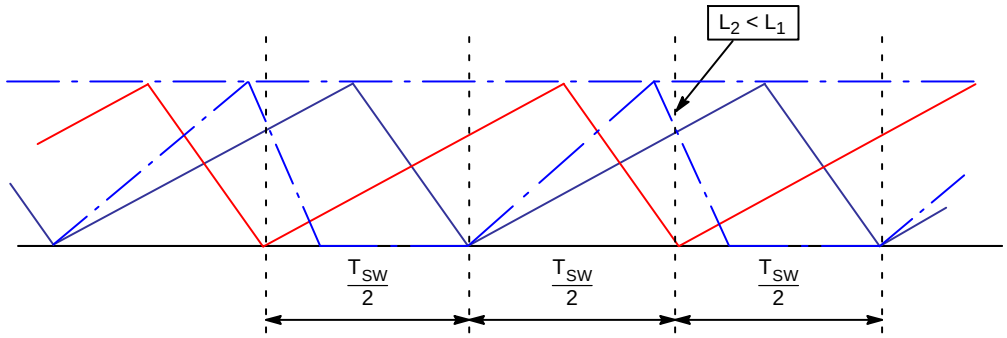
PRACTICAL IMPLEMENTATION

When controlling a CrM or FCCrM interleaved PFC, there is a main challenge: how get sure that both the two branches operate in CrM or FCCrM while running out-of-phase? The difficulty lies in the fact that the switching frequency is not fixed but varies versus the load and the line voltage. This is because in CrM or FCCrM, the MOSFET cannot turn on until the coil is fully demagnetized and even better until the very moment when the valley is detected. Hence, each phase should beat at its own rhythm and at the same time stay synchronized to the other branch.

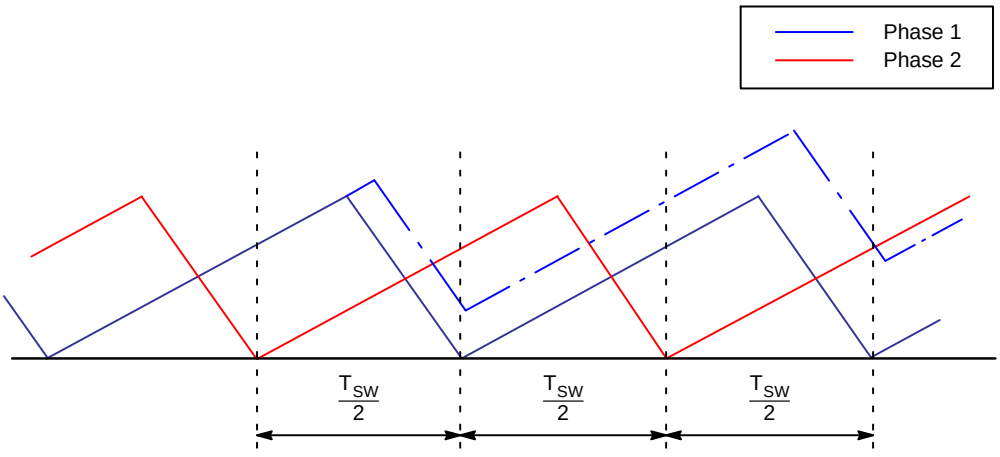
Two main approaches exist:

- The master/slave option where the master branch operates freely, the other one being controlled to follow out-of-phase. The challenge is to drive the slave branch so that it never enters CCM nor exhibits undesired dead-times. Figure 2 briefly portrays the type of difficulties that can be met when the slave is supposed to follow with the same switching period despite the effects of possible system defects:
  - An inductor imbalance that in current mode, may lead to a loss of the CrM operation within the slave stage (see Figure 2a).
  - A slight difference in the on-time of the two branches that may engender a similar issue in a voltage mode control (refer to Figure 2b).
- The interactive phases option where the two branches operate independently. Hence, each phase properly operates in CrM or FCCrM. The two branches however interact to set the proper 180° phase shift. Figure 3 illustrates one of the possible difficulties to overcome in a voltage mode solution: a perturbation in the conduction time of one branch engenders a loss of the phase shift.

For more information, refer to [4]. This paper gives a comprehensive analysis of the difficulties caused by each of the two approaches. In the rest of the paper, we will assume a perfect out-of-phase operation



a. Current Mode with Unbalanced Coils



b. Voltage Mode with On-Time Shift

Figure 2. Possible Issues in a Master/Slave Approach

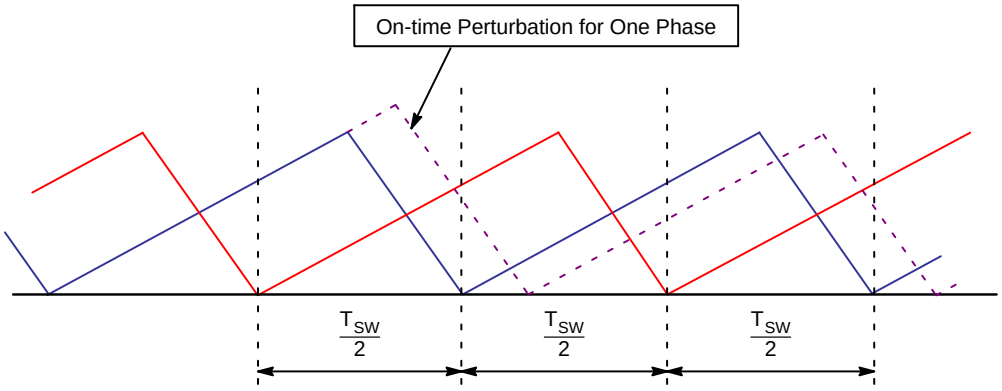


Figure 3. Possible Issues in the Independent Phases Approach

MAIN MERITS OF INTERLEAVED PFC

The Input Current Ripple is Minimized:

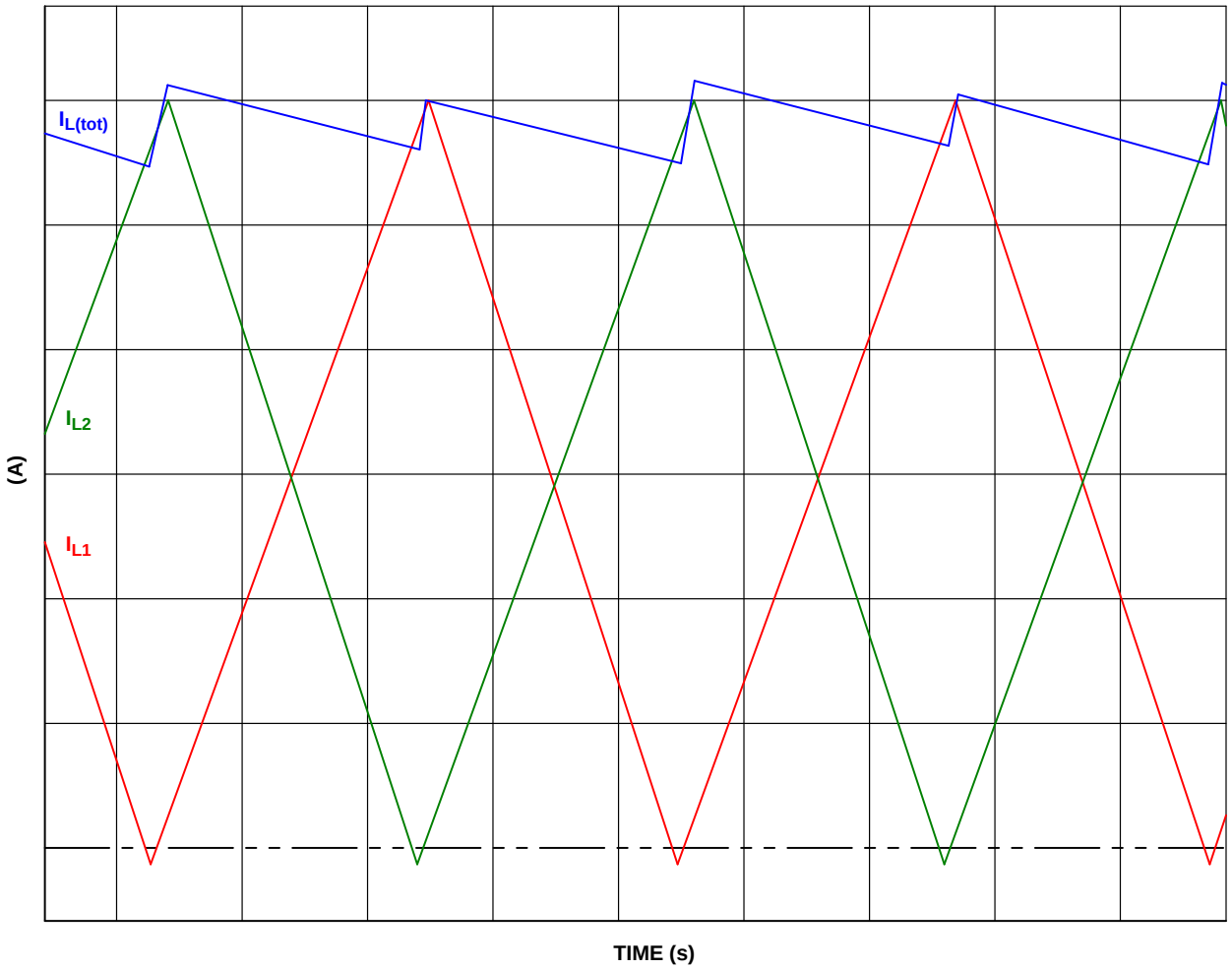
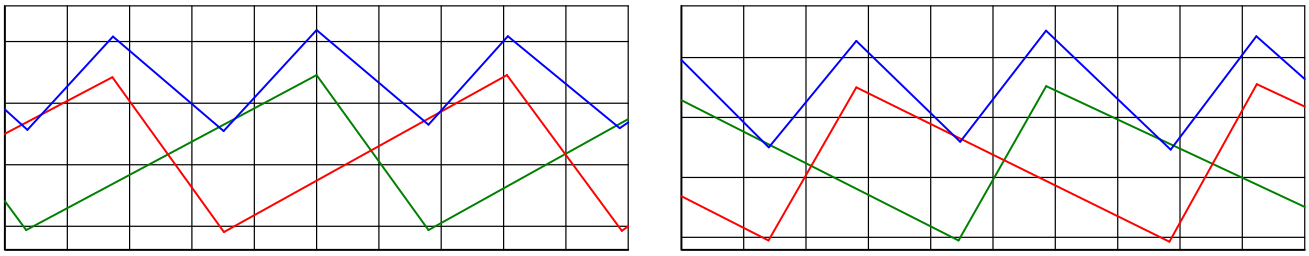


Figure 4. The Total Current Exhibits a Reduced Ripple

The coil current within each branch exhibits a large ripple (CrM operation) but as portrayed by Figure 4, out-of-phase operation results in a very small ripple on the global current drawn by the PFC stage.



Current Shape When $\left(V_{in} \le \frac{V_{out}}{2}\right)$ Current Shape When $\left(V_{in} \ge \frac{V_{out}}{2}\right)$

Figure 5. Current Shape

To compute the current ripple, we must notice that as portrayed by Figure 5, the global shape of the current differs according to the input voltage level:

- If ($V_{in} \le (V_{out}/2)$), the two branches operate with a duty cycle higher than 50%. Hence, the on-times of the two phases overlap;
- If ($V_{in} \ge (V_{out}/2)$), the duty cycle is below 50%. The demagnetization phase is the longest sequence within the switching period. The off-times of the two phases overlap.

Due to these differences, the computation of the total current requires to consider the two cases separately. For each of them, we can define periods of time when the two branches have their MOSFET on, when the two branches are in demagnetization phase, when one branch is in demagnetization phase and the other one has its MOSFET closed. Finally, for each period, we can add the current of the two branches.

Doing so, we can see that the total current:

- Always peaks when any of the branches enters a demagnetization phase;
- Is minimal at the very moment when a new on-time sequence starts in any of the branches.

More specifically, this computation enables to compute the total input current, its ripple, the “peak current envelop” that consists of its peak value levels and the “valley current envelop” that gives its valley value.

Figure 6 gives these magnitudes as a function (V_{in}/V_{out}).

	$V_{in}(t) \le \frac{V_{out}}{2}$	$V_{in}(t) \ge \frac{V_{out}}{2}$
Average Input Current (Line Current)	$I_{in}(t) = \left(I_{L(tot)}\right)T_{SW} = \frac{V_{in}}{R_{in}} = \frac{V_{in} \cdot P_{in(avg)}}{V_{in(rms)}^{2}}$	
Peak-to-Peak Ripple	$\left(\Delta I_{L(tot)}\right)_{PP} = I_{in} \cdot \left(1 - \frac{V_{in}}{V_{out} - V_{in}}\right)$	$\left(\Delta I_{L(tot)}\right)_{PP} = I_{in} \cdot \left(2 - \frac{V_{out}}{V_{in}}\right)$
Peak Current Envelop	$\left(I_{L(tot)}\right)_{pk} = 2 \cdot I_{in} \cdot \left(1 - \frac{V_{out}}{4 \cdot \left(V_{out} - V_{in}\right)}\right)$	$\left(I_{L(tot)}\right)_{pk} = 2 \cdot I_{in} \cdot \left(1 - \frac{V_{out}}{4 \cdot V_{in}}\right)$
Valley Current Envelop	$\left(I_{L(tot)}\right)_{V} = I_{in} \cdot \frac{V_{out}}{2 \cdot \left(V_{out} - V_{in}\right)}$	$\left(I_{L(tot)}\right)_{V} = \frac{P_{in(avg)} \cdot V_{out}}{2 \cdot V_{in(rms)}^{2}}$

Figure 6. Input Current Magnitude and Ripple

Figure 7 portrays the variation of the input current ripple as a function (V_{in}/V_{out}). One can note that the peak to peak ripple never exceeds 100% (±50%). This maximum value is obtained at ($V_{in} = 0$) and ($V_{in} = V_{out}$) that is at the limits of the input range. When the input voltage moves always from these extreme levels, the ripple reduces to totally cancel when ($V_{in} = (V_{out}/2)$).

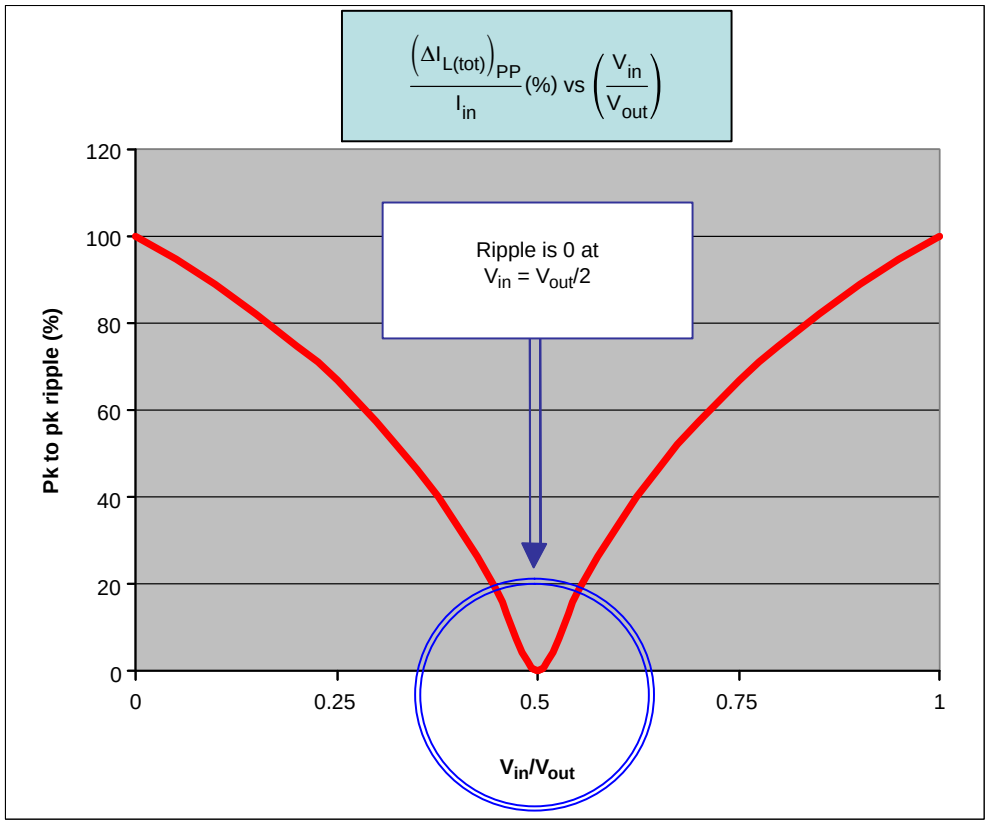


Figure 7. Input Current Ripple as a Function $\left(\frac{V_{in}}{V_{out}}\right)$

Figures 8 and 9 represent the input current at low and high line, respectively.

At low line, the input current looks that of a CCM PFC since its ripple is small. At the peak of the sinusoid, the ripple current is in the range ±28% @ 90 V_{rms}.

However, it is worth noting that the ripple does not really behave like that of a CCM PFC stage in the sense that, as testified by the equations of the Figure 7 table:

- The ripple does not depend on the chosen inductors;
- The ripple does not depend on the load.

At high line, the current envelop seems a bit more distorted. However, the ripple remains limited.

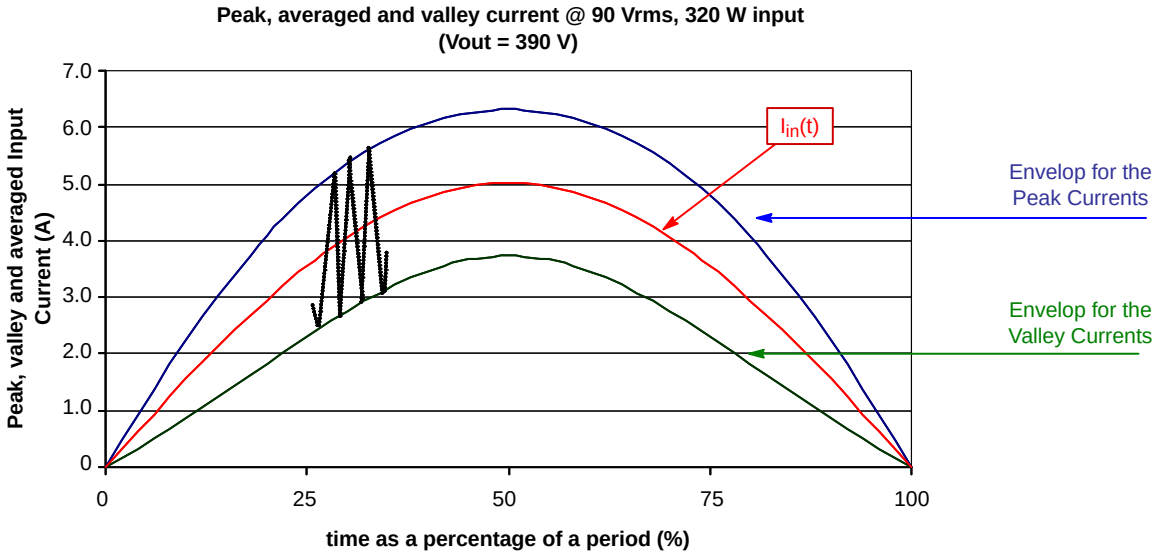


Figure 8. Typical Input Current at Low Line

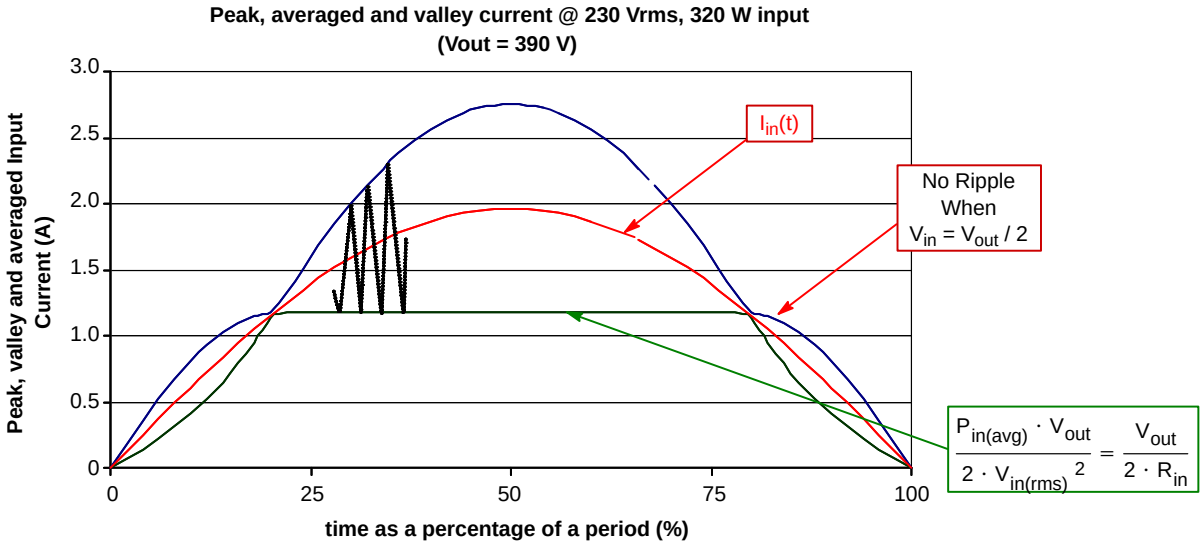


Figure 9. Typical Input Current at High Line

The Ripple of the Current that Feeds the Bulk and the Load is Minimized:

Figure 10 compares the refueling current (Note 1) that is obtained using different PFC converters.

In continuous conduction mode PFC, the boost diode conveys a quasi square wave current with a little ripple. If we ignore the ripple, the top of the diode current is (I_{in}) that is, the instantaneous line current. In Critical Conduction Mode, the refueling current has a triangular shape that like the coil current, peaks to ($2 \cdot I_{in}$). In interleaved PFC, each branch provides half the total power (assuming perfect current balancing). Hence, the coil current in each branch peaks to $\left(2 \cdot \left(\frac{I_{in}}{2}\right)\right)$ that is (I_{in}).

As shown by Figure 5, at low line in a wide mains application, there is no over-lap between the refueling phases of the two branches as a consequence of the 180° phase shift. More specifically, this is true when the conditions are the most severe when: $\left(V_{\leq} \frac{V_{out}}{2}\right)$

1. We call refueling current the current delivered by the PFC stage that feeds the bulk capacitor and the load. In a conventional 1-phase PFC, this is the output diode current. In a 2-phase interleaved PFC, it corresponds to the total current derived by the two output diodes.

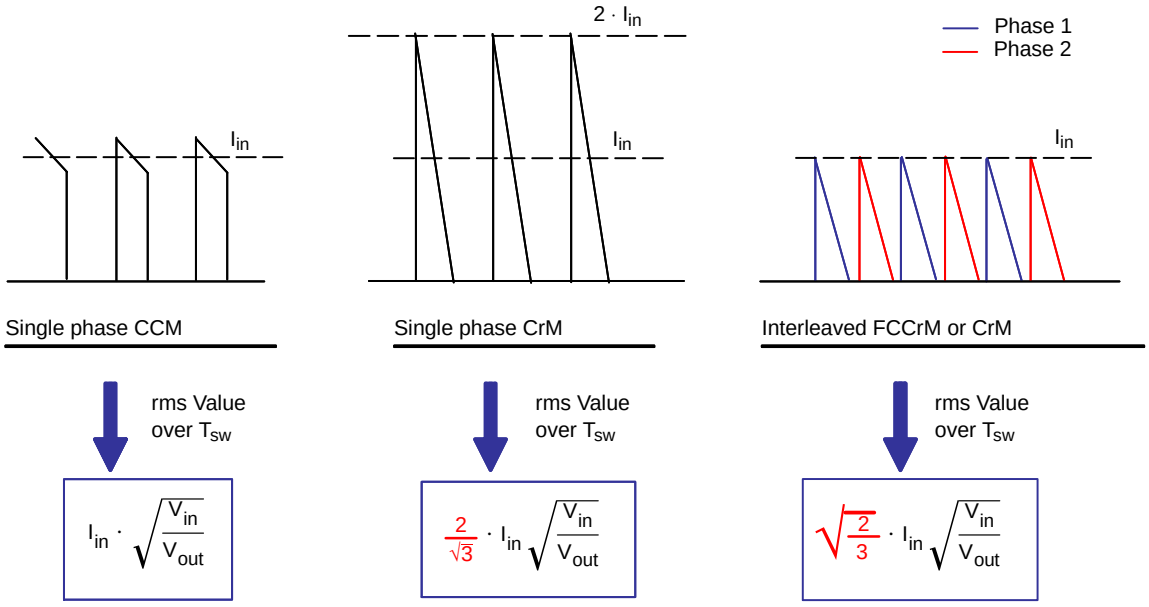


Figure 10. Shape and Magnitude of the Refueling Current

Figure 10 summarizes these characteristics and as a consequence of the current shape, gives the "rms current" computed over one switching period ($(I_{RMS})_{Tsw}$). $(I_{RMS})_{Tsw}$ must be viewed as the equivalent dc current that over the considered switching period, would dissipate the same energy as the refueling current across a resistor. To obtain the global rms current over a line period, we must average the square of $(I_{RMS})_{Tsw}$ over the line period and take the root-square of the result. In other words, we calculate the total power the refueling current dissipates across a 1 Ω resistor and deduct the dc current that would engender the same losses across the same 1 Ω resistor (see method detailed in AND8123/D).

Using this process, we can easily compute the refueling current in the three cases and deduce the rms capacitor current in the case of a resistive or constant current load.

Figure 11 gives the general equations. The table also consists of the practical values for a wide mains, 300 W application.

	Single Phase CCM PFC	**Single Phase CrM or FCCrm PFC**	**Interleaved CrM or FCCrM PFC**
Diodes(s) rms Current ($I_{D(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\frac{2}{\sqrt{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\sqrt{\frac{2}{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$
Capacitor rms Current ($I_{C(rms)}$)	$\sqrt{\frac{8\sqrt{2}\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{32\sqrt{2}\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{16\sqrt{2}\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$
300 W, V_{out} = 390 V, $V_{in(rms)}$ = 90 V	$I_{D(rms)}$ = 1.9 A $I_{C(rms)}$ = 1.7 A	$I_{D(rms)}$ = 2.2 A $I_{C(rms)}$ = 2.1 A	$I_{D(tot)(rms)}$ = 1.5 A $I_{C(rms)}$ = 1.3 A

Figure 11. Comparison of the Refueling and Capacitor Currents

DESIGN CONSIDERATIONS

This section does not intend to deeply deal with the design of an interleaved PFC. Simply, it will simply highlight some key points. For more details, you can refer to [5] that covers the design of a 300-W, wide mains application driven by the NCP1631 (controller optimized for interleaved PFC stages). [6] also illustrates this process in the case of a discrete solution based on two NCP1601 controllers.

Design of the Boost Inductor (for Each Branch)

The inductor must be designed for half the power. Compared to a conventional CrM PFC that would have to deliver the same power, the peak current is then halved. On the other hand, in CrM, the switching frequency directly depends on the current cycle duration that is imposed by the power, the inductor, the input and output voltages. If the current magnitude is halved, the coil inductance should be doubled to keep the same switching frequency range.

Finally, we can summarize the above statements as follows:

- $L_1 = L_2 = 2 \cdot L_{CrM}$
- $I_{pk1} = I_{pk1} = I_{pk(CrM)} / 2$

Where:

- L_1 and L_2 are the inductor of each branch, L_{CrM} the inductor of a CrM conventional PFC stage delivering the same total power.
- I_{pk1} and I_{pk2} are the peak current of each branch, $I_{pk(CrM)}$ the peak current of a CrM conventional PFC stage delivering the same total power.

So if we use the $(L \cdot I_{pk}^2)$ as a rough criterion to estimate the core size, we find that:

$$L_1 \cdot I_{pk1}^{\ 2} = L_2 \cdot I_{pk2}^{\ 2} = \frac{L_{CrM} \cdot I_{CrM}^{\ 2}}{2} \qquad \text{(eq. 1)}$$

Finally, an interleaved PFC stage requires two inductors whose core size is half that of a CrM conventional PFC stage for the same global power. Hence, both solutions require approximately the same global core size.

Power MOSFET

In a CrM PFC stage, the conduction losses are given by the following equation:

$$P_{M(CrM)(on)} = \frac{4}{3} \cdot R_{DS(on)} \cdot \frac{\left(\frac{P_{out}}{\eta}\right)^2}{V_{in(rms)}^{\ 2}} \cdot \left(1 - \frac{8 \cdot \sqrt{2} \cdot V_{in(rms)}}{3 \cdot \pi \cdot V_{out}}\right) \qquad \text{(eq. 2)}$$

Hence, in each branch of an interleaved PFC, still assuming a perfect balancing, the losses will be:

$$P_{M1(on)} = P_{M2(on)} = \frac{4}{3} \cdot R_{DS(on)} \cdot \frac{\left(\frac{P_{out}}{2 \cdot \eta}\right)^2}{V_{in(rms)}^{\ 2}} \cdot \left(1 - \frac{8 \cdot \sqrt{2} \cdot V_{in(rms)}}{3 \cdot \pi \cdot V_{out}}\right) \qquad \text{(eq. 3)}$$

Which simplifies as follows:

$$P_{M1(on)} = P_{M2(on)} = \frac{1}{3} \cdot R_{DS(on)} \cdot \frac{\left(\frac{P_{out}}{\eta}\right)^2}{V_{in(rms)}^{\ 2}} \cdot \left(1 - \frac{8 \cdot \sqrt{2} \cdot V_{in(rms)}}{3 \cdot \pi \cdot V_{out}}\right) = \frac{P_{M(CrM)(on)}}{4} \qquad \text{(eq. 4)}$$

So, the total losses are:

$$P_{M1(on)} + P_{M2(on)} = \frac{P_{M(CrM)(on)}}{2} \qquad \text{(eq. 5)}$$

So, if each branch of the interleaved PFC stage uses the same MOSFET as that of the equivalent CrM conventional PFC stage, the conduction losses are halved.

In practice, we may more likely implement “smaller” MOSFETs in each branch compared to the switch used in a conventional CrM PFC stage. For instance, in a 300 W application, we can implement one SPP11N60 (0.39 Ω @25°) per branch and 2 in parallel or a SPP20N60 (0.19 Ω @25°) in a 1-phase conventional PFC. Doing so, we obtain the same global conduction losses.

As for the switching losses, they are extremely hard to predict.

One can simply note that whether a traditional or interleaved PFC is used, the switching event occurs under the same voltage stress. The current is half for each phase of the interleaved PFC but we must consider two branches. So, the current stress can again be viewed as similar. Hence:

- If the same MOSFETs are used (one in a traditional PFC, 1 per branch in an interleaved one), the global switching losses must be the same in the two solutions
- If each branch uses a smaller MOSFET, the switching losses should be reduced due to the lower parasitic capacitances and higher transition speed.

Boost Diodes

Interleaved PFC requires two boost diodes (one per branch). However, when used in CrM or FCCrM, there are no reverse recovery issues to worry about. Simply, they must meet the correct voltage rating ($V_{out(max)}$+margin) and exhibit a low forward voltage drop. Supposing a perfect current sharing, the average diode current is half the load one $\left(I_{d1} = I_{d2} = \frac{I_{d(total)}}{2} = \frac{P_{out}}{2 \cdot V_{out}} \cong 0.39\ A \right)$. So, the losses are just $\left(\frac{I_{d(total)} \cdot V_f}{2} \right)$ per diode. For each phase, the peak current seen by the diode will be the same as the corresponding inductor peak current.

Summary

The following table summarizes the key characteristics of an interleaved PFC with respect to conventional FCCrM and CCM PFC for a 300 W, wide mains application.

Important Remark

Please note that due to its frequency clamp, FCCrM allows the use of smaller coils compared to CrM. CrM requires the use of relatively high inductances to limit the switching frequency to acceptable levels. The table is then valid for FCCrM conventional PFC and FCCrM interleaved PFC only.

For the sake of consistency, the CCM coil is chosen so that it exhibits the same input ripple as the interleaved PFC at low line, full load.

	Single FCCrM stage		Interleaved FCCrM stage		Single CCM stage	
	General	300-W, wide mains	General	300-W, wide mains	General	300-W, wide mains
$\Delta I_{in(max)}$ (A)	Independent on L	10.0 A	Independent on L	2.6 A	Depends on L	2.6 A (at 90 V_{rms}, full load if L = 250 µH)
Inductor	1 coil 	75 µH $I_{L,pk(max)}$ = 10 A $I_{L,rms(max)}$ = 4.1 A $L*I_{pk}^2$ = 7.5 mJ	2 coils 	150 µH $I_{L,pk(max)}$ = 5.0 A $I_{L,rms(max)}$ = 2.0 A $L*I_{pk}^2$ = 3.7 mJ	1 coil 	250 µH $I_{L,pk(max)}$ = 6.3 A $I_{L,rms(max)}$ = 3.5 A $L*I_{pk}^2$ = 9.9 mJ
Total MOSFET conduction losses (with below MOSFETs)	$\frac{4 \cdot R_{DS(on)}}{3} \left(\frac{P_{in(avg)}}{V_{in(rms)}} \right)^2 \left[1 + \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi \cdot V_{out}} \right) \right]$	4.6 W	$\frac{2 \cdot R_{DS(on)}}{3} \left(\frac{P_{in(avg)}}{V_{in(rms)}} \right)^2 \left[1 + \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi \cdot V_{out}} \right) \right]$	4.6 W	$R_{DS(on)} \left(\frac{P_{in(avg)}}{V_{in(rms)}} \right)^2 \left[1 + \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi \cdot V_{out}} \right) \right]$	3.5 W
MOSFETs		1 * SPP20N60 or 2* SPP11N60		2 * SPP11N60		1 * SPP20N60 or 2* SPP11N60
Diode	Ultrafast	MUR550 (TO220) 	2 * Ultrafast	2 * MUR550 (axial) 	Low t_{rr} diode	High speed diode (SiC..) 
$I_{C(rms)(max)}$ (A)	$\sqrt{\frac{32\sqrt{2}}{9\pi} \cdot \left(\frac{P_{out}}{\eta} \right)^2 \cdot \frac{1}{V_{in(min)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}} \right)^2}$	2.0	$\sqrt{\frac{16\sqrt{2}}{9\pi} \cdot \left(\frac{P_{out}}{\eta} \right)^2 \cdot \frac{1}{V_{in(min)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}} \right)^2}$	1.3	$\sqrt{\frac{8\sqrt{2}}{3\pi} \cdot \left(\frac{P_{out}}{\eta} \right)^2 \cdot \frac{1}{V_{in(min)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}} \right)^2}$	1.7
EMI complexity	DM: high CM: moderate		DM: moderate CM: moderate		DM: moderate CM: high	
Characteristics	Compact design		Low profile designs		Compact design	

Compared to CrM, FCCrM allows the use of smaller inductances (due to frequency clamp)
The inductance for the single and interleaved FCCrM stages is based on a 130 kHz frequency clamp (high frequency design).
The switching frequency is also supposed to be 130 kHz for the CCM stage.

Conclusions

This paper gives an overview of the interleaved PFC approach. This modular solution eases the heat distribution. It requires more components but they are smaller and hence, this approach can be particularly interesting when slim designs are required. For more details, refer to the below references. In particular, [1] and [2] give performance data in term of efficiency.

References

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[3] Joel Turchi, “Performance of a 300 W, wide mains interleaved PFC driven by the NCP1601”, Application Note AND8356/D, www.onsemi.com.

[4] L. Huber, B. T. Irving and M. M. Jovanovic, “Open-Loop Control Methods for Interleaved DCM/CCM Boundary Boost PFC Converters”, IEEE trans. Power Electron., vol. 23, no. 4, pp 1649-1657, July 2008.

[5] Joel Turchi, “Key Steps to Design an Interleaved PFC Stage Driven by the NCP1631”, Application Note AND8407/D, www.onsemi.com.

[6] Joel Turchi, “Designing a high efficiency, 300 W, wide mains interleaved PFC driven by the NCP1601”, Application Note AND8354/D, www.onsemi.com.

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