AND8346/D

A519HRT HART® Modem

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

Introduction

This application note describes a demonstration circuit that permits a user to implement a HART slave or master interface between a microprocessor and a process loop using the ON Semiconductor A5191HRT HART modem integrated circuit. The information in this Application Note is correct to the best of our knowledge. Development of a circuit suitable to the user's particular system and application environment is the responsibility of the user.

The HART (Highway Addressable Remote Transmitter) communication protocol provides digital communication for microprocessor−based process control instruments. HART uses the Bell−202 forward channel signaling frequencies and bit rate (1200 bits/second) as making it a subset of the Bell−202 standard. HART−speaking devices can use virtually any Bell−202 standard modem. However, the ON Semiconductor A5191HRT single−chip modem has been designed to meet the low power requirements of 2−wire process instruments.

The ON Semiconductor A5191HRT modem is designed to allow the user to easily implement a HART compliant Physical Layer design conforming to the HART FSK Physical Layer Specification[2]. The A5191HRT is intended to replace the 20C15 for all existing and future HART applications with no circuit topology changes. Only the values of four external resistors in the receive filter need to be adapted.

Features

- Same modem design as 20C15 from LSI Logic (formerly NCR and Symbios)
- Transmits a trapezoidal signal
- Internal oscillator cell
- Internal receive filter
- Carrier detect
- Available in 28−pin PLCC, 32−pin QFN and 32−pin LQFP Packages
- These Devices are Pb−Free and are RoHS Compliant

This application note shows how to interface the A5191HRT modem to the HART network, as well as other general advice on using the modem and on designing HART devices. A block diagram showing a typical application of the A5191HRT in a HART Slave is shown in Figure 1.

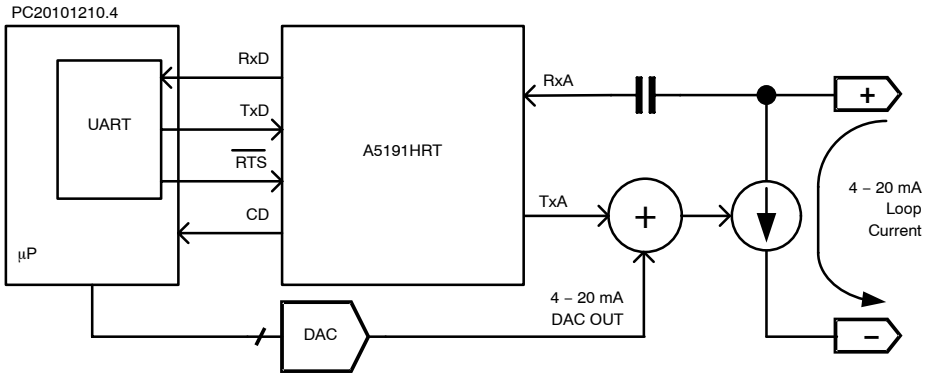


Figure 1. HART Slave Application Block Diagram

OVERVIEW OF HART COMMUNICATIONS

Analog Signaling

HART devices are connected in a conventional current loop arrangement shown in Figure 2. The HART Slave or Process Transmitter or Field Instrument (terminology used by HART specification) signals by varying the amount of current flowing through itself.

The HART Master or Controller (Primary Master) detects this current variation by measuring the DC voltage across the current sense resistor. The loop current varies from 4 to 20 mA at frequencies usually under 10 Hz.

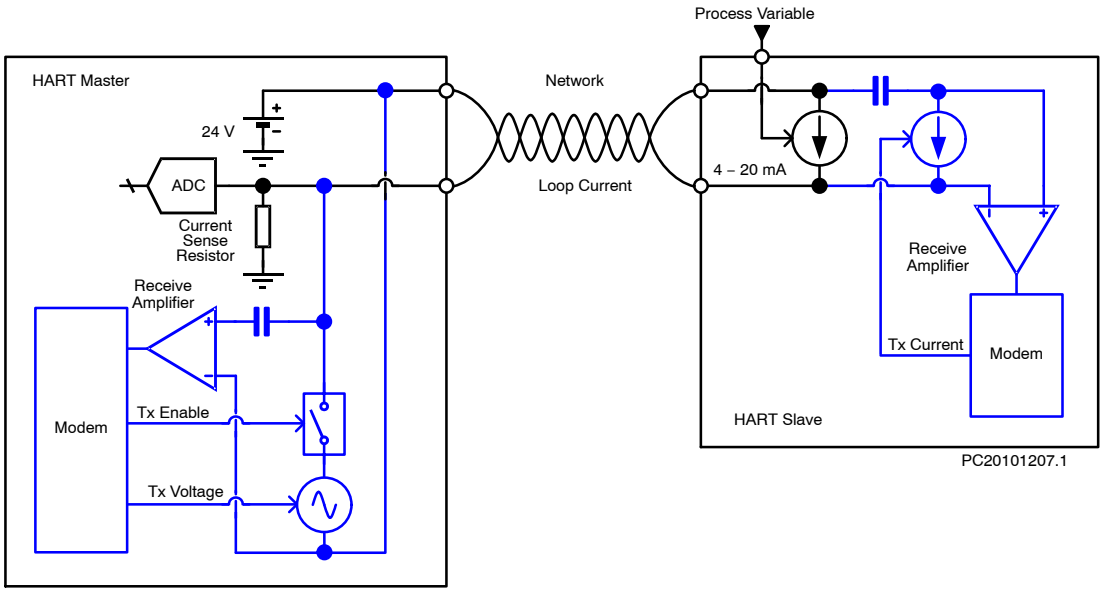


Figure 2. Current Loop with HART Signal Sources. Analog Signaling is Marked in Black. Digital Signaling is Marked in Blue.

Digital Signaling

The HART (digital) signal is superimposed on the 4−20 mA (analog) signal as shown in Figure 2 (marked in blue). The Master transmits HART signals by applying a voltage signal across the current sense resistor and it receives a voltage signal by detecting the HART current signal across the sense resistor. Conversely, the Slave transmits by modulating the loop current with HART signals and receives HART signals by demodulating the loop current.

HART Waveform

HART signals using phase−continuous frequency−shift−keying (FSK) at 1200 bit/s. Phase−continuous frequency−shift−keying requires the phase angle of the mark (1200 Hz) and the space (2200 Hz) to remain continuous at the 1200 bit/s bit boundaries. A HART Slave or Field Instrument transmits a HART signal by modulating a high−frequency carrier current of about 1 mA p−p onto its normal output current. This is illustrated in Figure 3 for a 6 mA analog signal.

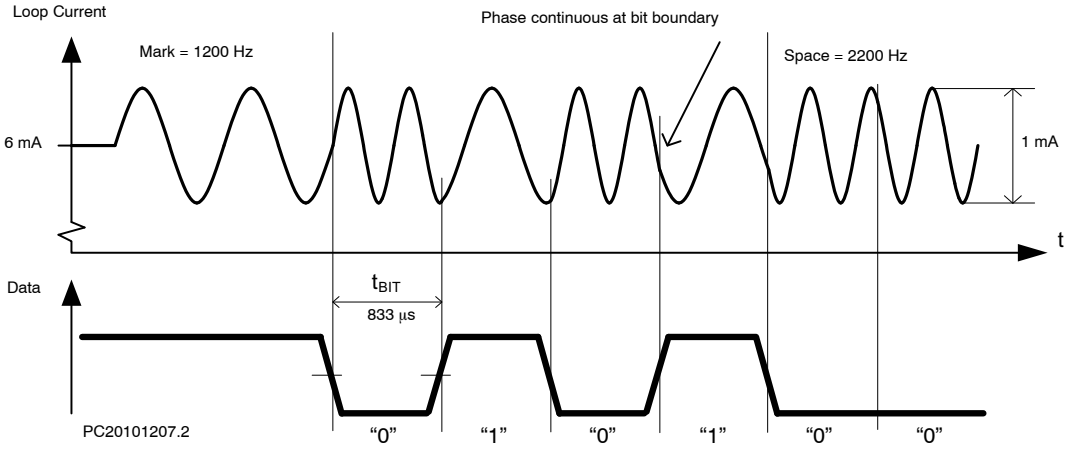


Figure 3. Field Instrument Current versus Time

HART Slave Device

HART Slaves transmit by modulating the process 4−20 mA DC loop current with a 1 mA p−p AC current signal as shown in Figure 3. Since the average value of the HART signal is zero, the DC value of the process loop remains unchanged. Receive circuits in a HART Slave device amplify, filter, and demodulate the current signal.

HART Multi−dropped Slave Devices

Some current loops (called networks in HART documents) use only digital signaling. The field instrument current is fixed at 4 mA or some other convenient value, and only digital communication occurs. Up to 15 such field instruments with unique addresses of 1 through 15 may be connected in parallel. More address space is available for devices compliant with HART specification rev. 5 or higher (up to 38 bits). A device that is not multi−dropped will usually have its address set to 0.

HART Master Device

HART Masters transmit by driving the loop with a low impedance voltage source as shown in Figure 2. Regardless whether a master or field device is transmitting, a signal voltage of about 500 mVp−p is developed across the conductors of the current loop (assuming a 500 Ω current sense resistor), and is seen by both devices. Receive circuits in each device filter and demodulate the signal voltage.

HART Primary Master

In general, a HART Primary Master is the device that provides the communications between the control system (DCS) and the remote process instruments with the intent to receive process information and perform maintenance operations. A HART network that has a HART Master interface integrated into the DCS will usually be configured as a Primary Master.

HART Secondary Master

In general, a second HART interface connected to a network that contains a Master will be a Secondary Master. An example of a Secondary Master is a hand−held communicator that would be connected directly across a HART. Such a network may have a Primary Master. A HART network can only have one Primary and one Secondary Master connected a time.

Multiplexing a HART Master

To reduce the design complexity of a multiple loop HART Master, the physical layer can be multiplexed to two or more process loops. This is usually done with analog switches that allow signals as high as 6 Vp−p to pass and exhibit an extremely low ‘on resistance’. The added impedance of the switch directly affects the output impedance of the Master device.

The multiplexer can switch only the HART signal or it can switch both the HART signal and the associated signal return. Switching the signal return insures the physical layer interface will be non−intrusive to the HART network if a failure were to occur. Typically, the analog switches connect to each process loop through a coupling capacitor (about 2.2 μF).

The greatest disadvantage of multiplexing HART signals is the reduction in communication throughput to each Slave device.

HART Cabling

Because of the relatively low HART frequencies, there is little cable attenuation and delay distortion. This results in very few restrictions on constructing networks. The complete topology requirements and electrical requirements for HART devices are given in the HART Physical Layer Specification[2].

In most applications, HART communications can be performed up to a distance of 1500 meter using existing field wiring for a 2−wire process instrument.

HART Data Link Layer

Normally, one HART device talks while others listen. Talking means that the device applies the modulated carrier to the network cable. A given device applies the carrier in one unbroken segment called a frame. Between frames the network is silent. Field instrument frames are usually responses to commands by a Master. Further information on network protocol is found in the HART Data Link Layer Specification[1].

A5191HRT FUNCTIONAL BLOCKS

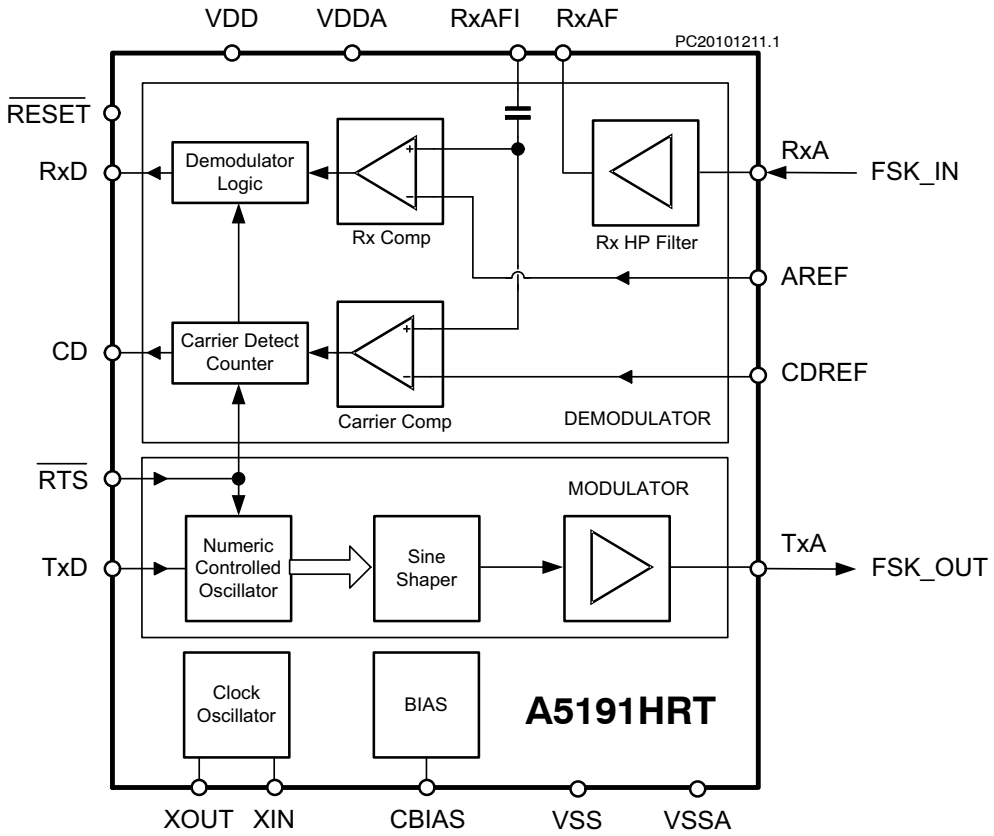


Figure 4. A5191HRT Block Diagram

HART MODEM

Demodulator

The demodulator accepts an FSK signal at its RxA input and reproduces the original modulating signal at its RxD output shown below:

The modem uses shift frequencies of nominally 1200 Hz (logical one, mark) and 2200 Hz (logical zero, space).

The bit rate is nominally 1200 bits/second. The output of the modulator RxD is qualified with the carrier detect signal CD. Therefore only RxA signals large enough to be detected (100 mVp−p typical) by the carrier detect function will produce demodulated output at RxD.

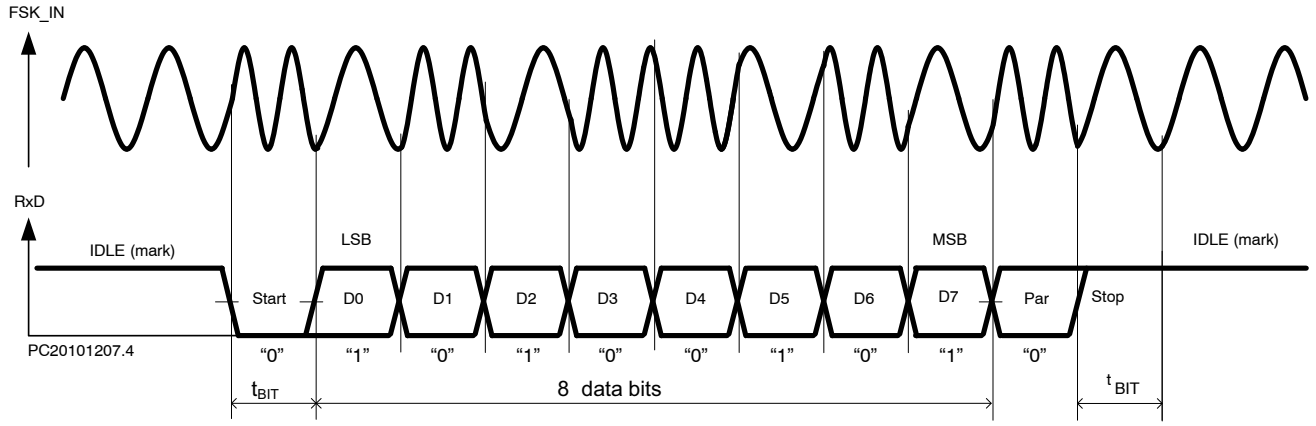


Figure 5. Demodulator Signal Timing

Modulator

The modulator accepts digital data in NRZ form at its TxD input and generates the FSK modulated signal at its TxA output. RTSB must be a logic low for the modulator to be active.

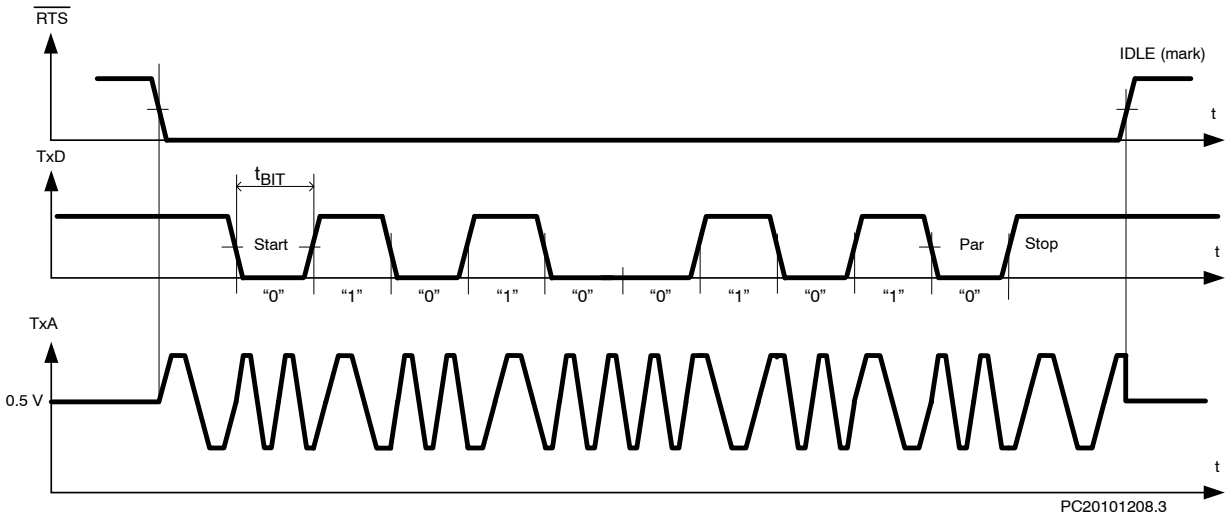


Figure 6. Modulator Signal Timing

Transmit Waveshaping

The A5191HRT generates a HART compliant trapezoidal FSK modulated signal at its TxA output. Shown in Figure 6 are actual transmit signals from a A5191HRT.

The amplitude of TxA is proportional to the analog reference voltage as follows:

$$V_{TxA,p-p} = V_{AREF} \times 0.417$$

For V_{AREF} = 1.235 V

V_{TxA} = 1.235 x 0.417 = 0.515 V p−p

The DC bias voltage of TxA is V_{TxA} = 0.5 V.

This means that when:

RTSB = “1” V_{TxA} = 0.5 V

RTSB = “0” V_{TxA} has a voltage swing from 0.16 V to 0.77 V.

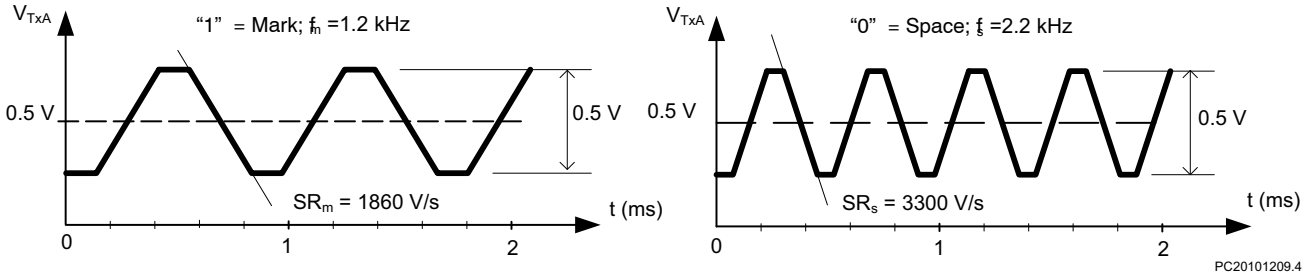


Figure 7. TxA Waveforms

Carrier Detect

Low HART input signal levels increases the risk for the generation of bit errors. If the received signal is below this 100 mV p−p level the demodulator is disabled.

NOTE: HART Physical Layer Specification specifies a signal level > 120 mVp−p as a valid carrier; signal level < 80 mVp−p as noise.

This level detection is done in the Carrier Detector. The output of the demodulator is qualified with the carrier detect signal (CD), therefore, only RxA signals large enough to be detected (100 mVp−p typically) by the carrier detect circuit produce received serial data at RxD.

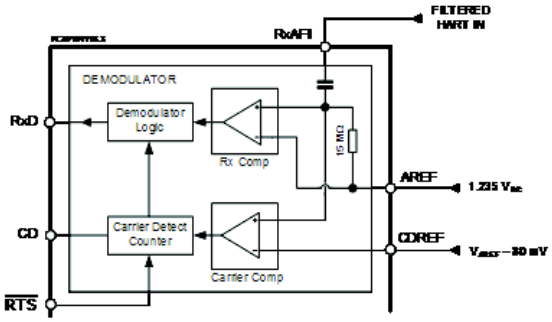


Figure 8. Demodulator Carrier and Signal Comparator

The carrier detect comparator shown in Figure 8 generates logic Low output if the RxAFI voltage is below CDREF. The comparator output is fed into a carrier detect block. The carrier detect block drives the carrier detect output pin CD high if nRTS is high and four consecutive pulses out of the comparator have arrived. CD stays high as long as nRTS is high and the next comparator pulse is received in less than 2.2 ms.

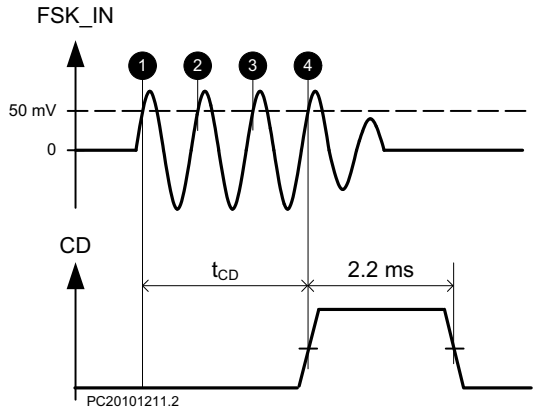


Figure 9. Carrier Detect Timing

Once CD goes inactive, it takes four consecutive pulses out of the comparator to assert CD again. Four consecutive pulses equals t_{CD} = 3.33 ms when the received signal is 1200 Hz and t_{CD} = 1.82 ms when the received signal is 2200 Hz.

Clock Oscillator

The A5191HRT requires a 460.8 kHz clock. This frequency is generated in the internal clock oscillator block, designed to use either a quartz crystal, ceramic resonator, or an external clock.

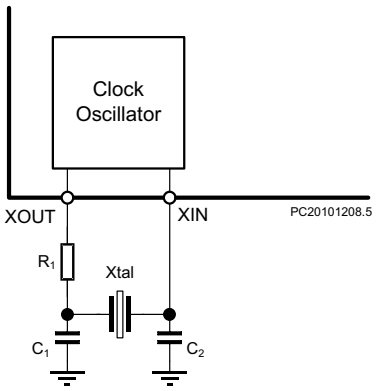


Figure 10. Oscillator Connection for Ceramic Resonator or Quartz Crystal

When using a crystal or resonator the accuracy should be at least 1%. The oscillator requires two external capacitors and one external resistor, which values varies depending on the used type. The specifications are listed in Table 4. Care should be taken to keep the circuit board traces between the A5191HRT and the external oscillator components as short as possible.

Ceramic Resonator Sources

Ceramic resonators are less expensive than quartz crystals, but are not as accurate. Unfortunately, ceramic resonators at the needed frequency require special ordering in very large quantities. Ceramic resonators that oscillate at 460.8 kHz are available from:
http://www.ecsxtal.com/store/dc-4-ecs-resonators.aspx
www.raltron.com/products/resonators/default.asp

Quartz crystals are available from:
www.aelcrystals.co.uk
www.statek.com/prod_thruholecrystals.php

Table 1. CERAMIC RESONATOR AND QUARTZ CRYSTAL VALUES

Description	Ceramic	Quartz	Unit
Type	ECS Crystal ZTB Series	Statek CX−1V Series	
Frequency	460.8	460.8	kHz
C_1	220	47	pF
C_2	220	22	pF
R_1	0	10	kΩ
Maximum ESR	N.A.	12	kΩ

External Clock

It may be desirable to use an external clock of 460.8 kHz rather than the internal oscillator cell because of the cost and availability of quartz crystals or ceramic resonators. In addition, the A5191HRT consumes less current when an external clock is used as shown in Figure 11. An external clock associated with the microprocessor (running at a frequency that is a multiple of 460.8 kHz) can be used as an input to the oscillator cell. Table 5 lists commonly available clock frequencies for crystals suited to this purpose. The interface between the microprocessor clock and the A5191HRT could be as simple as a direct connection or a single integrated circuit.

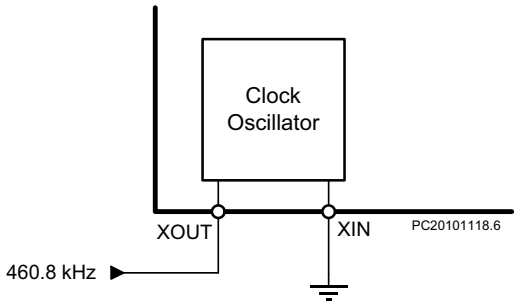


Figure 11. External Clock

NOTE: Output XOUT is driven by an external source

Table 2. COMMONLY AVAILABLE FREQUENCY MULTIPLES

Frequency	Multiple
1.8432 MHz	x4
3.6864 MHz	x8
7.3728 MHz	x16
14.7456 MHz	x32
29.4912 MHz	x64

Clock Skew

If one uses the same time base for both the modem and the UART, a 1% accurate time base may not be good enough. The problem is a combination of receive data jitter and clock skew between transmitting and receiving HART devices. If the transmit time base is at 99% of nominal and the receive time base in another device is at 101% of nominal, the receive data (at the receiving UART) will be skewed by roughly 21% of one bit time at the end of each 11−bit byte. This is shown in Figure 12. The skew time is measured from the initial falling edge of the start bit to the center of the 11th bit cell. This 21% skew by itself isn't bad. However, there is another error source for bit boundary jitter. The Phase Lock Loop demodulator in the A5191HRT produces jitter in the receive data that can be as large as 12% of a bit time. Therefore, a bit boundary can be shifted by as much as 24% of a bit time relative to its ideal location based on the start−bit transition. (The start−bit transition and a later transition can be shifted in opposite directions for a total of 24%.)

The clock skew and jitter added together is 45%, which is the amount that a bit boundary could be shifted from its expected position. UARTs that sample at mid−bit will not be affected. However, there are UARTs that take multiple samples during each bit to try to improve on error

performance. These UARTs may not be satisfactory, depending on how close the samples are to each other, and how samples are interpreted. A UART that takes a majority vote of 3 samples is acceptable.

Even if your own time base is perfect, you still must plan on a possible 35% shift in a bit boundary, since you don't have control over time bases in other HART devices.

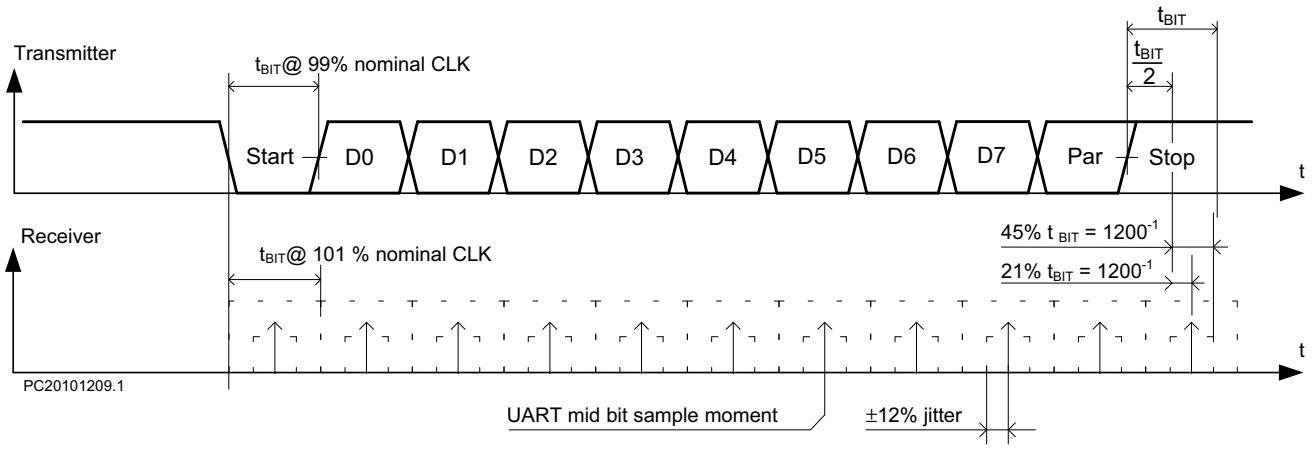


Figure 12. Clock Skew

RECEIVE ANALOG CIRCUITRY

Receive High−pass Filter

To remove the interfering analog signal, a high−pass filter is required in the HART signal receive path. The filter requirements are found as follows. From section 7.1 of the HART Physical Layer Specification[2], the interfering signal can be as high as 16 V p−p at 25 Hz.

NOTE: This is directly related to limits on analog signaling. The difference in specifications for analog interference as output versus analog interference as input is the result of the loads being different.

The interfering analog signal should be reduced to at least ten times smaller than the smallest HART signal, or under about 7.5 mV. Therefore, the high−pass filter should have an attenuation of 63 dB at 25 Hz. The HART signal band covers approximately 950 Hz to 2500 Hz, which means that the high−pass filter should begin rolling off somewhere below 950 Hz and be 63 dB down at 25 Hz. This is illustrated in Figure 13.

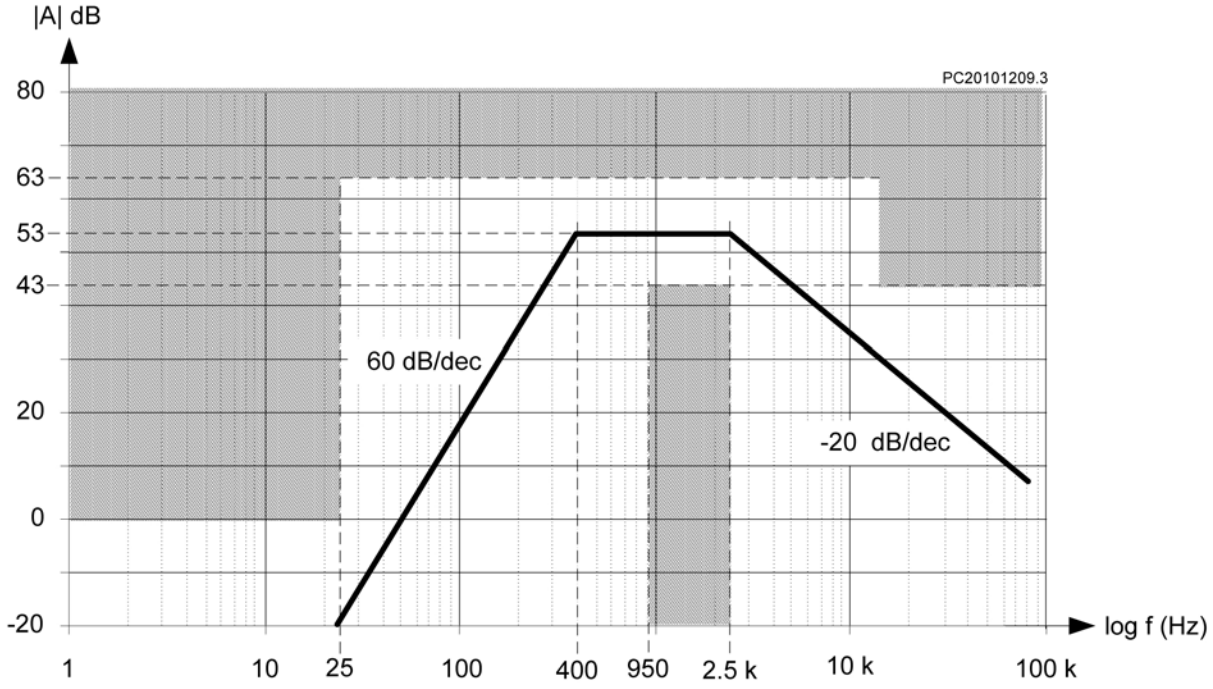


Figure 13. Receive Filter Bounds

The A5191HRT has an internal active filter to attenuate the frequencies outside the HART band. In addition to the internal active filter, an external passive filter is necessary to complete the filtering requirements. The external capacitors and resistor were too large in size to cost effectively integrate into the A5191HRT silicon.

The external components required for the receive filter is shown in Figure 14. All the external capacitors are ±5% and the resistors are ±1% components (except the 3 MΩ which is ±5%).

The external components on the receiver create a third order high pass filter with a pole at 624 Hz and a first order low pass filter with a pole at 2500 Hz. Internally, the A5191HRT has a high pass pole at 35 Hz and a low pass pole at 90 kHz, each of which can vary by as much as ±30 %. The input impedance to the entire filter is greater than 150 kΩ at frequencies less than 50 kHz.

A5191HRT is a pin to pin replacement for 20C15. Only the values of four resistors in the receiver need to be changed. (See Table 5 values marked in *italic*).The different resistor values change the shape of the lower pass band for the receive filter. It creates a more robust and noise immune receiver and as a results provides more margin in passing the out−of−band noise interference tests.

Table 3. RECEIVE FILTER VALUES FOR A5191HRT AND 20C15

Symbol	A5191HRT	20C15	Tolerance	Unit
R_1	215	*402*	1%	kΩ
R_2	215	*453*	1%	kΩ
R_3	499	*825*	1%	kΩ
R_4	787	787	1%	kΩ
R_5	422	*732*	1%	kΩ
R_6	215	215	1%	kΩ
R_7	3	3	5%	MΩ
C_1	470	470	5%	pF
C_2	1	1	5%	nF
C_3	1	1	5%	nF
C_4	220	220	5%	pF

The values shown for all external components in Figures 14 and Table 6 and all other circuits in this application note are those used in the circuitry which was used to pass the HART physical layer conformance test for the A5191HRT.

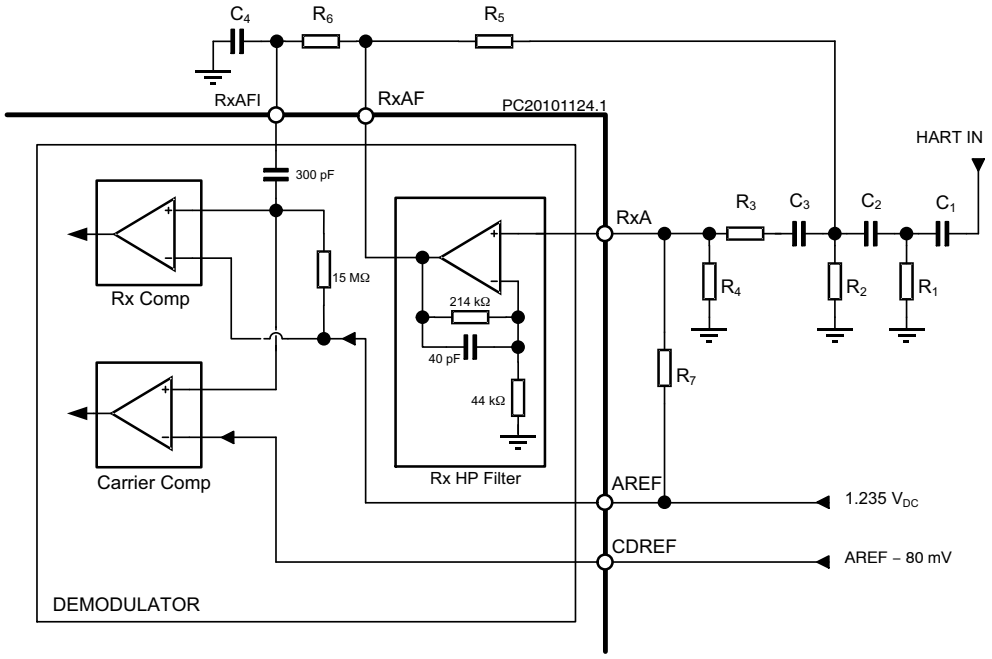


Figure 14. Receive Filter

Voltage References

The A5191HRT requires two voltage references, AREF and CDREF. AREF sets the DC operating point of the internal operational amplifiers and is the reference for the Rx comparator.

If A5191HRT operates at V_{DD} = 3.3 V the ON Semiconductor LM285D−1.2 1.235 V reference is recommended. In the case V_{DD} = 5 V, AREF is typically 2.5 VDC. LM285D−2.5 is recommended.

The level at which CD (Carrier Detect) becomes active is determined by the DC voltage difference (CDREF − AREF). Selecting a voltage difference of 80 mV will set the carrier detect to a nominal 100 mVp−p.

Analog Bias Resistor

The A5191HRT requires a bias current resistor R_{BIAS} to be connected between CBIAS and V_{SS}.

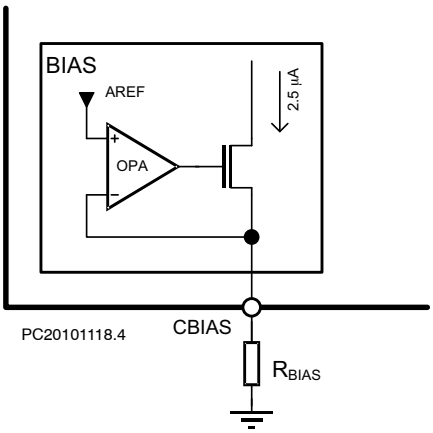


Figure 15. Bias Circuit

The bias current controls the operating parameters of the internal operational amplifiers and comparators and should be set to 2.5 μA.

The value of the bias current resistor is determined by the reference voltage AREF and the following formula:

$$R_{BIAS} = \frac{AREF}{2.5\ \mu A}$$

The recommended bias current resistor is 499 kΩ when AREF is equal to 1.235 V or 100 kΩ when AREF is 2.5 V.

Supply Current Budget and Transmitter Lift−Off Voltage

Current consumption of internal circuits is important in any 2−wire field instrument. It becomes critically important in a microprocessor− based field instrument featuring both analog and digital signaling. The available current is derived here and some techniques are examined for reducing current consumption.

The nominal HART signal transmitted by a field instrument is 0.5 mA peak. When this is superimposed upon a 4 mA analog signal, the terminal current must vary between 3.5 mA and 4.5 mA. During the peak of the HART waveform, the instrument has 4.5 mA available, but during the valley it has only 3.5 mA. Energy storage techniques can be used to allow the internal circuits to draw a steady 4 mA at all times. However, to be effective at HART frequencies, the storage capacitor should be quite large. A large capacitor (or any form of energy storage device) complicates the circuit design if intrinsic safety is required.

Therefore, the circuit is normally designed to run everything on 3.5 mA. Another 200 to 400 μA is often subtracted from this to allow some margin and to satisfy other conditions. Assuming a guard value of 200 μA, the

internal circuits of the 2−wire field instrument have to live on a diet of 3.3 mA during transmit. While receiving 3.8 mA is available.

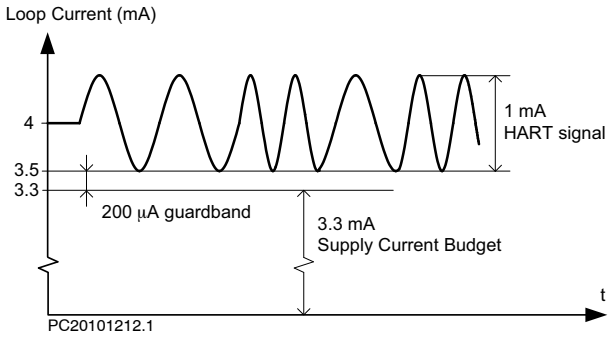


Figure 16. Supply Current Budget

A characteristic of the A5191HRT is that its current consumption is approximately 350 to 450 μA. This leads to the fortunate circumstance that the remaining (non−modem) circuits always have at least 2.85 mA available. Margins may be needed to cover current consumption over temperature. One way of reducing the A5191HRT current consumption is to operate it at reduced voltage. Since the A5191HRT is a CMOS part, current consumption is roughly proportional to supply voltage. Operation at V_{DD} = 3.3 V is common.

In applying the A5191HRT be careful not to let inputs float. The nRTS pin of the A5191HRT will often be driven by an I/O pin of a microprocessor. During power−up or after reset an I/O pin may be tri−stated, allowing it to float. This can cause the A5191HRT to draw excess current. In some cases the current may be large enough to prevent the field instrument from starting up properly. There should be a 1 MΩ pull−up resistor on RTSB.

The transmitter lift−off voltage is the minimum terminal voltage at which it is guaranteed to operate. When only analog signaling is involved, lift−off voltage is an unambiguous quantity. But when HART digital signaling is added, the available voltage can swing by as much as 0.75 V above and below the DC level. The minimum applied voltage is the DC level minus 0.75 volt. You should either design the field instrument to accommodate the dips in voltage, or else specify the lift−off voltage to include them.

INTERFACING TO THE HART NETWORK

Slave Device

The Slave interface to the network is typically a current regulator, as illustrated in simplified form in Figure 17. Its output current is controlled by varying a much smaller current into an op−amp summing junction. This junction is a convenient point at which to sum the analog and digital signals, thereby achieving superposition of the digital signal onto the analog. The digital transmit signal (TxA) is capacitively coupled into the summing junction, to preserve DC accuracy of the 4 − 20 mA analog signal. Also shown in Figure 17 is the receive path, consisting of a capacitor from the collector of the current regulator transistor to a high−impedance amplifier. Both the receive amplifier and the transmit current source should present a high impedance (greater than 100 kΩ) to the network.

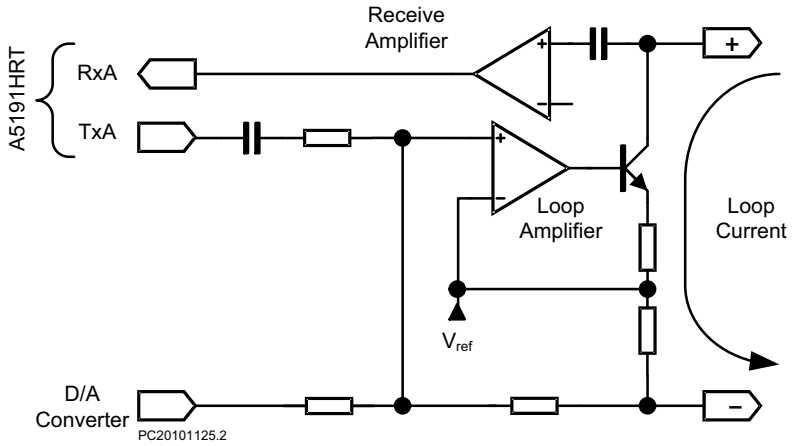


Figure 17. Simplified HART Slave Interface Circuit

Transmit Interface

The amplitude of TxA is nominally 500 mVp−p. The HART Physical Layer requires the Slave to modulate the loop with a 1 mA p−p signal. The amplitude of modulation of the loop current will have to be adjusted before the amplifier in the current loop regulator or at the regulator itself. It is recommended that the amplitude can be adjusted with voltage gain circuits. Using a small series capacitance to attenuate the signal may cause distortion of the transmitted signal.

Receive Interface

All HART receivers require non−disruptive coupling to the network current loop. This connection can be made with capacitive or inductive coupling without corruption of the process loop current. Typically a HART Slave uses a small value (1 nF) capacitor to couple an adequate signal level to the receive filter.

Master Device

The HART Master interfaces to the network as a voltage source, as illustrated in simplified form in Figure 18. The network is driven by a low output impedance (600 Ω or less) voltage amplifier circuit that can be switched to a high impedance state using RTSB. The output of the voltage amplifier needs to be high impedance while the HART Master receives, to insure a high input impedance for the receiver. Typically a HART Master uses a 2.2 μF coupling capacitor to insure the transmitter circuit meets the output impedance requirements specified in the HART Physical Layer Specification.

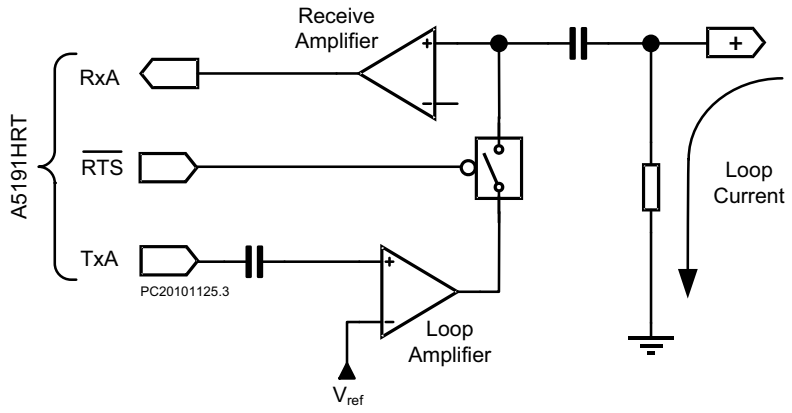


Figure 18. Simplified HART Master Interface Circuit

Transmit Interface

The amplitude of TxA is nominally 500 mVp−p. The 500 mVp−p meets the requirements for a HART Master. However, the A5191HRT is unable to source enough current to drive a HART network, therefore a low impedance voltage driver build around the Loop Amplifier is required between the A5191HRT and the network.

Transmit Switch

During a HART message transmission from the Master, the output impedance of the voltage source is quite low (0 − 600 Ω). However during reception of a HART message, the input impedance of the receive section must be quite high. Therefore, the transmitter section must be disabled when not active (nRTS = “High”).

Several methods can be used to achieve a high output impedance of the transmitter while nRTS is inactive. One method is choosing an op−amp with an “active low” current programming resistor that will basically “turn−off” the op−amp during receive operations. A second method can be implemented with a correctly biased discrete FET in series with the output stage. Lastly, a discrete solid−state relay with a characteristically low “on resistance” can be used.

All three above techniques will provide an adequate solution for the impedance requirements. However, only the third solution will allow proper circuit operation per the “bit−error−rate” requirements and does not need to be powered by a dual supply.

Under worse case conditions, a transmitter could dynamically change from 4 − 20 mA and a HART Master could have as much as 1 kΩ of loop resistance. This results in $(20 - 4)10^{-3} \times 1{\cdot}10^{3} = 16$ V p−p low frequency carrier with HART superimposed. The transmit switch must be designed to prevent this 16 V p−p signal from sinking current through the HART transmitter’s output stage. Any clipping of the 16 Vp−p signal through the HART transmitter or the use of transient suppressors will result in the clipping of the superimposed HART signal. The last solution will block and not clip the 16 Vp−p process signal and will not corrupt the input impedance. The third solution can be implemented easily as shown in Figure 18.

Receiving the HART Signal

HART Signal Coupling

All HART receivers require non−disruptive coupling to the network current loop. This connection can be made with capacitive or galvanic coupling without corruption of the process loop current. A receiver in a Master may use a single 2.2 μF capacitor to couple the HART signal in which the Master is always connected across a current sense resistor and share the same ground. Where ground isolation is required, another coupling capacitor may be necessary in the signal return connection.

To insure complete isolation from the network, galvanic isolation is the preferred method. Typically a transformer and a series capacitor are used to couple the HART signal. With this type of isolation, the master can be connected across the field instrument or the current sense resistor regardless of the polarity or grounding configuration.

Current Sense Resistor

The current sense resistor is considered an integral part of a HART Master. In operation, a HART message response from a Slave is superimposed on the 4−20 mA current loop. The Slave's 1 mA p−p HART signal is dropped across the Master's sense resistor. For a typical sense resistor of 250 Ω, one can expect 250 mVp−p signal extracted from a HART Slave device. A HART Master can have a sense resistor ranging from 230 Ω to 600 Ω.

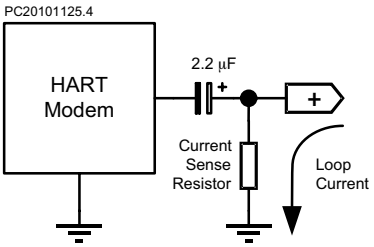
Master Connection to a HART Network

A HART Master must be able to receive voltage signals that are developed across the sense impedance. In addition, it must be able to apply a transmit signal across the current sense impedance. In some cases the Master will signal across the field device as well. In all cases, the presence of the HART Master must not disrupt the analog signaling of the process loop. Therefore, the HART signals must be non−intrusively coupled from the current sense resistor to the Master through one of the various coupling techniques listed below.

Coupling Techniques

Coupling to the network is most commonly done with capacitors and transformers. The simplest form of coupling is a single capacitor as shown in Figure 19.

This coupling technique will only work if one side of the Current Sense Resistor is connected to the analog ground.



This coupling technique will only work if one side of the Current Sense Resistor is connected to the analog ground.

Figure 19. Single Capacitive Coupling

Using two capacitors will allow a connection across a sense resistor or field device that does not have one of its connections at analog ground as show below in Figure 20.

When two coupling capacitors are used, lager values are required to meet the impedance requirements.

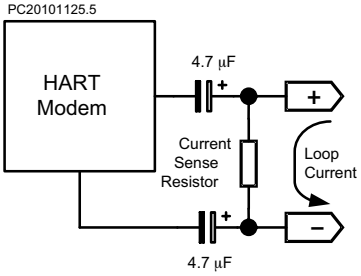


Figure 20. Dual Capacitive Coupling

Capacitive coupling can work well when Masters have their power isolated from ground. When the system power configuration is unknown, the use of transformer coupling will insure the elimination of ground effects. An example of transformer coupling is shown below in Figure 21.

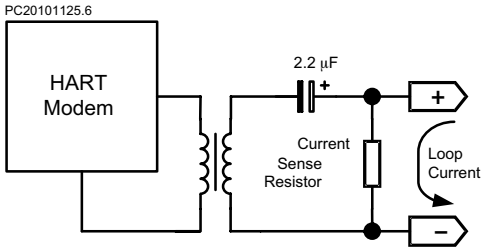


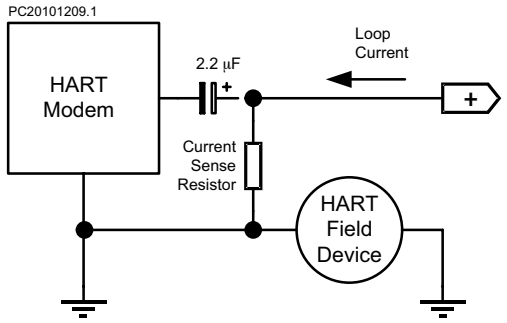
Figure 21. Transformer Coupling

Grounding Effects

With the use of capacitive coupling, AC and DC ground loops can be created if one is not aware of the grounding techniques of both the Master and the process loop. If the Master is powered from a battery or a galvanically isolated power source, then single capacitive coupling will work in any HART network.

If a Master (that does not have an isolated power source) with single capacitive coupling is connected to a sense resistor or field device that is not at ground potential, a DC ground loop will occur as shown in below:

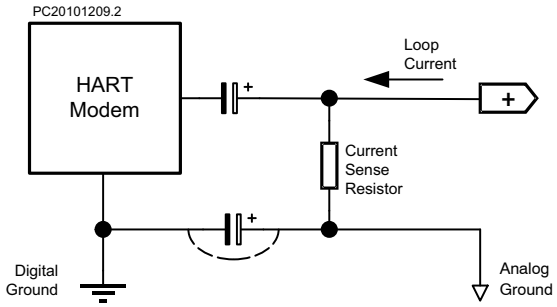
In this case the Field Device will have a direct short across it.



In this case the Field Device will have a direct short across it.

Figure 22. Single Capacitor Coupled DC Ground Loop

If the Master has a ground connection that is not at the ground potential as the analog ground from the process loop, it is possible to create AC ground loops. A noisy 240 VAC ground signal could be coupled directly unto the process loop ground (single capacitive coupling) or coupled unto the process loop (dual capacitive coupling) ground through the connection. The AC noise potentially could impede HART communications and corrupt the accuracy of the DCS measuring the analog current as shown in Figure 23.



The dashed line shows the ground loop when a single coupling capacitor is used..

Figure 23. Capacitor Coupled AC Ground Loop

Limiting the Analog Signal Frequency Bandwidth

Digital signaling can potentially interfere with analog signaling. A much worse problem is the analog signal interfering with digital signaling. This is due to the relative size of the two signals. For example, a change from 4 to 20 mA can produce a voltage change of as high as 16 V across the field instrument terminals, depending on the amount of resistance in the loop. At the same time, the instrument may be trying to detect a HART (digital) signal as low as 80 mVp−p.

Separating the two is usually done with a combination of low−pass filtering of the analog signal and high−pass filtering of the HART signal. The HART Physical Layer Specification[1] (section 7.2) limits the analog signal to 16 mA p−p at frequencies below 25 Hz and constrains the output above 25 Hz to fall within a −40 dB/decade slope, as illustrated in Figure 24. This means, for example, that a sinusoidal output at 25 Hz must have an amplitude into a 500 Ω test load of less than 8 Vp−p. It also means that a 25 Hz square wave of 8 Vp−p would not be acceptable, since its harmonics do not decrease at a −40 dB rate.

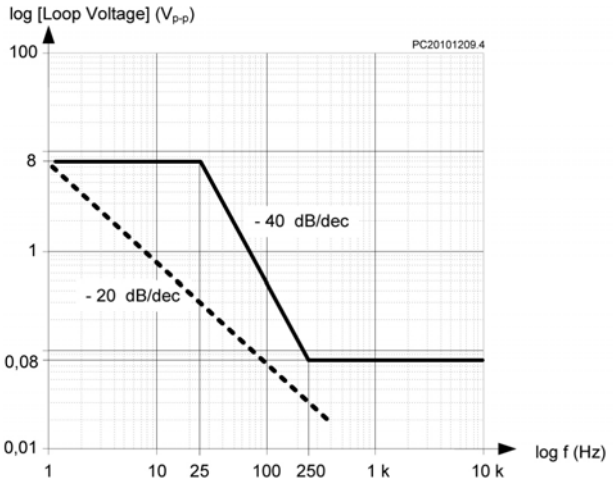
The required roll−off of the 4 – 20 mA analog signal can be achieved by various means, including:

- Analog filters.
- Digital filters (software).
- Inherent filtering in the instrument sensor.

Often it is a combination of these. Any convenient method may be used to insure that changes in instrument output current fall within the specification. If the field instrument uses a D/A converter (DAC) to generate its analog output, the output steps of the DAC must be sufficiently small or else the high−frequency content of the steps must be removed by filtering. When large changes in the DAC output occur due to calibration operations, caution must be used not to have these DAC changes active during a HART command or response. Any large and fast current changes that fall outside the HART specifications can cause unreliable communications with the HART Master or Slave.

The analog signaling of typical field instruments is usually band−limited to the range of 1 to 10 Hz, so that the roll−off starts well below the 25 Hz point of Figure 24. This can lead to simpler low− pass filtering. For example, a single−pole filter that begins rolling off at 1 Hz falls below the curve of Figure 24.

The dashed line illustrated the use of a simple first order filter with a pole at 1 Hz.



The dashed line illustrated the use of a simple first order filter with a pole at 1 Hz..

Figure 24. Analog Signal Bandwidth Limitation

Miscellaneous

Start of Frame

Because the HART carrier must be started and stopped, the receiving UART and processor must become synchronized to each HART frame. During the synchronization period at the beginning of the frame, it is normal for some transmitted bytes to be corrupted or lost. Various HART requirements have been devised to insure that synchronization will occur. They are:

- The transmitting device must send at least five preamble bytes (hex FF).
- The transmitting device must load the first preamble byte into the transmit UART within 5−bit times of starting carrier.
- The receiving device must recognize carrier within 30−bit times.

Correct start−up is based on the fact that, during the stream of preamble bytes, the start bits (applied to the UART) are the only 0 bits.

Everything else (stop, data, and parity bits), including idle time, is a 1. Although some extra 0 bits may be generated by the start−up transient, after a short time only valid start bits will remain and the device will be synchronized.

End of Frame

The UART can cause a possible problem at the end of frame. Normally, it is necessary to wait until the last bit of the last character of the frame has been sent until carrier is turned off. The UART usually tells you it is empty, which is an indication that you should turn carrier off. However, UARTs differ in when they indicate empty. Some indicate empty at the time of the last shift clock − that is, simultaneously with the stop bit being shifted out. But if carrier were to be turned off at that time, the modem would cease transmitting and the stop bit wouldn't be sent. Therefore, it is important to determine which kind of UART you have. If it behaves as described, then you should wait at least one bit time after the empty indication until you turn off carrier. Note that adding a 1 bit delay can't do any harm, even if it isn't needed.

Misuse of Carrier Detect

To maximize speed, a field instrument will often be designed to begin its response frame immediately after the Master's command frame. These frames are close enough together that there is not enough time for carrier detect to drop out. This brings out an important point regarding carrier detect: It sole purpose is to indicate the presence of carrier, so that receivers know that they have sufficient signal to work with. Carrier detect is not intended to reliably indicate the start or end of a particular frame. Start of frame detection is a Data Link Layer function and must occur through examination of the frame content.

More information

More information can be found under following weblinks:

Datasheets and Application notes of devices used above
http://www.onsemi.com

HART Standards:
http://www.hartcomm.org/

APPENDIX

HART Slave

The schematic in Figure 25 is a possible implementation of the HART Slave physical layer. The Loop Current Regulator Circuit build around the op amp is for information only. For detailed information on the Hart Physical Layer specification and requirements see the HART Physical Layer Specification[1].

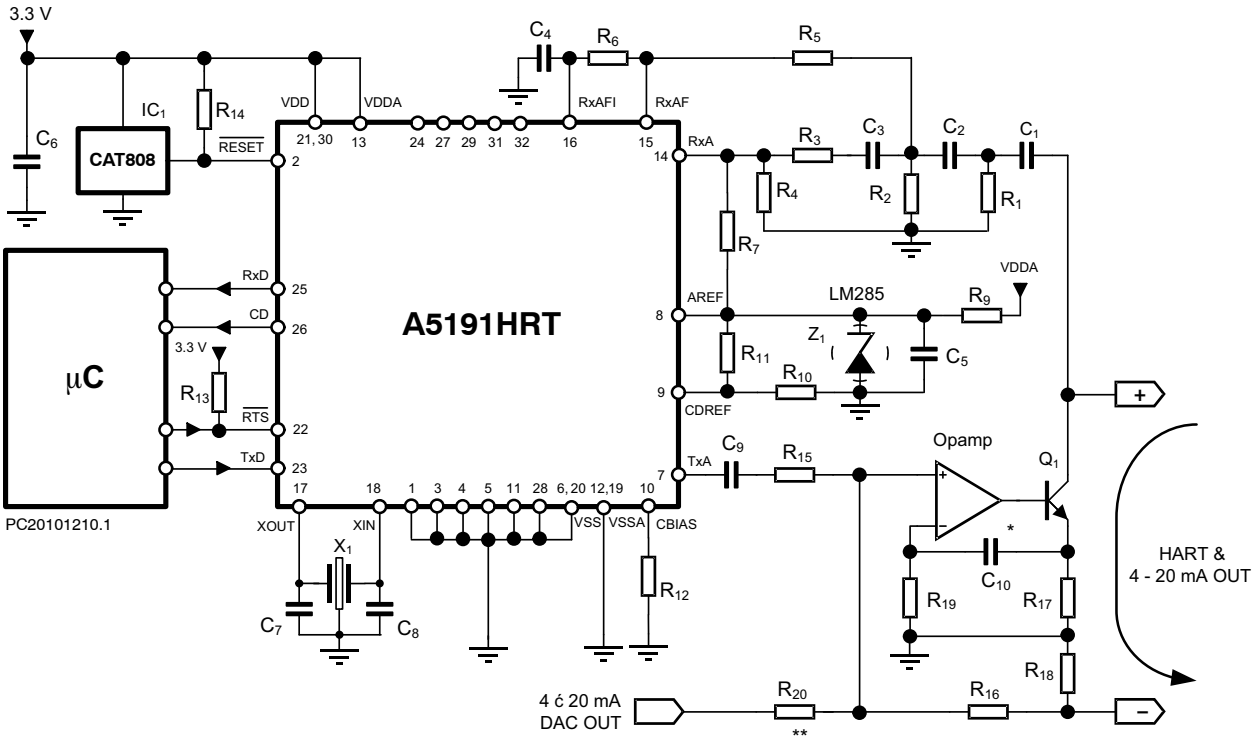


Figure 25. Possible Implementation for HART Slave Physical Layer

Table 4. COMPONENT LIST HART SLAVE IMPLEMENTATION

Symbol	Value	Tolerance	Units
R_1	215	1%	kΩ
R_2	215	1%	kΩ
R_3	499	1%	kΩ
R_4	787	1%	kΩ
R_5	422	1%	kΩ
R_6	215	1%	kΩ
R_7	3	5%	MΩ
R_8	470	5%	pF
R_9	10	1%	kΩ
R_{10}	200	1%	kΩ
R_{11}	14.7	1%	kΩ
R_{12}	499	1%	kΩ
R_{13}	1	5%	MΩ
R_{14}	100	5%	kΩ

*Value depends on used operational amplifier
**Value depends on V_{MSB} of DAC

Table 4. COMPONENT LIST HART SLAVE IMPLEMENTATION

Symbol	Value	Tolerance	Units
R_{15}	47	1%	kΩ
R_{16}	11.3	1%	kΩ
R_{17}	120	1%	Ω
R_{18}	120	1%	kΩ
R_{19}	3.6	5%	kΩ
R_{20}	6.2**	1%	kΩ
C_1	470	5%	pF
C_2	1	5%	nF
C_3	1	5%	nF
C_4	220	5%	pF
C_5	10	20%	nF
C_6	100	20%	nF
C_7	220	5%	pF
C_8	220	5%	pF
C_9	100	5%	nF
C_{10}	*		
Z1	LM285	http://www.onsemi.com/pub/Collateral/LM285−D.PDF	
Q1	BC547	http://www.onsemi.com/pub/Collateral/BC546−D.PDF	
IC1	CAT808	http://www.onsemi.com/pub/Collateral/CAT808−D.PDF	
X1	ZTBF−460.8−E	http://www.ecsxtal.com/store/pdf/ztb_ztbfr.pdf	

*Value depends on used operational amplifier
**Value depends on V_{MSB} of DAC

HART Master

The schematic in Figure 26 is a possible implementation of the HART Master physical layer. The HART signal coupling circuit build around the op amp is for information only. For detailed information on the Hart Physical Layer specification and requirements see HCF_SPEC−54.

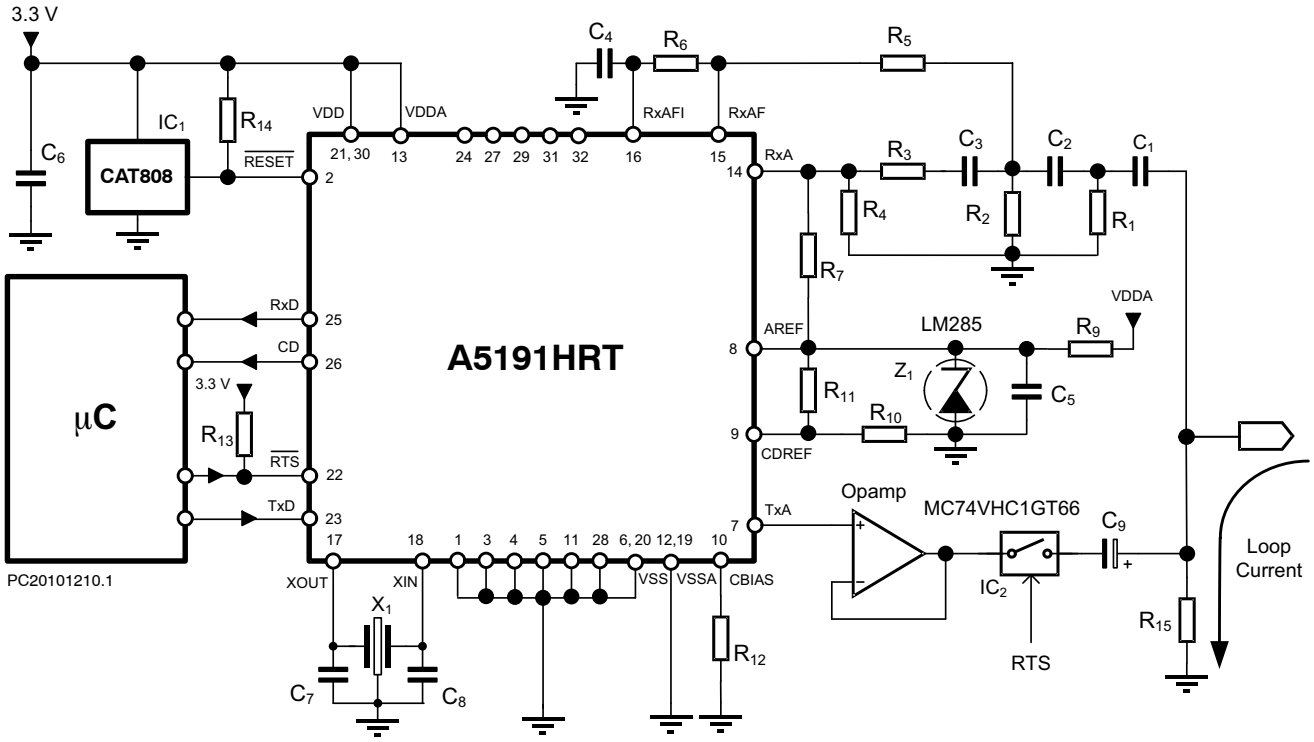


Figure 26. Possible Implementation for HART Master Physical Layer

Table 5. COMPONENT LIST HART MASTER IMPLEMENTATION

Symbol	Value	Tolerance	Unit
R_1	215	1%	kΩ
R_2	215	1%	kΩ
R_3	499	1%	kΩ
R_4	787	1%	kΩ
R_5	422	1 %	kΩ
R_6	215	1 %	kΩ
R_7	3	5 %	MΩ
R_8	470	5 %	pF
R_9	10	1 %	kΩ
R_{10}	200	1 %	kΩ
R_{11}	14.7	1 %	kΩ
R_{12}	499	1 %	kΩ
R_{13}	1	5 %	MΩ
R_{14}	100	5 %	kΩ
R_{15}	499*	1 %	Ω
C_1	470	5%	pF
C_2	1	5%	nF
C_3	1	5%	nF
C_4	220	5%	pF
C_5	10	20 %	nF

*Value depends on the required HART master Current Sense sensitivity

Table 5. COMPONENT LIST HART MASTER IMPLEMENTATION

Symbol	Value	Tolerance	Unit
C_6	100	20 %	nF
C_7	220	5 %	pF
C_8	220	5 %	pF
C_9	2,2	20 %	μF
Z1	LM285	http://www.onsemi.com/pub/Collateral/LM285−D.PDF	
Q1	BC547	http://www.onsemi.com/pub/Collateral/BC546−D.PDF	
IC1	CAT808	http://www.onsemi.com/pub/Collateral/CAT808−D.PDF	
IC2	1GT66	http://www.onsemi.com/pub/Collateral/MC74VHC1GT66−D.PDF	
X1	ZTBF−460.8−E	http://www.ecsxtal.com/store/pdf/ztb_ztbfr.pdf	

*Value depends on the required HART master Current Sense sensitivity

A5191HRT Current Consumption

The current consumption of the 15191HRT can be drastically reduced by reducing operating voltage and using an external clock. Table 6 lists typical current usage under different operating conditions. Other possibilities to reduce current consumption include shutting down the master during dead time, and careful design of reference voltage generation.

Table 6. CURRENT CONSUMPTION IN DIFFERENT CIRCUIT CIRCUMSTANCES

Operating Condition	Operating Voltage	Current Consumption
Idle, External oscillator	2.8 V	220 μA (Typ.)
Idle, External oscillator	3 V	240 μA (Typ.)
Normal Operation	3 V	350 μA (Typ.)
Absolute maximum current consumption	3 V	450 μA (Max.)

REFERENCES

1. HART Communication Foundation Document Number HCF_SPEC−13, HART FSK Communication Protocol Specification, Revision 7.3; 9390 Research Blvd., Suite I−350, Austin Texas, 78759.
2. HART Communication Foundation Document Number HCF_SPEC−54, HART FSK Physical Layer Specification, Revision 8.1; 9390 Research Blvd., Suite I−350, Austin Texas, 78759.
3. HART Communication Foundation Document Number HCF_TEST_2, HART FSK Physical Layer Test Specification, Revision 2.1; 9390 Research Blvd., Suite I−350, Austin Texas, 78759.

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