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AND8337/D

How to Apply High Frequency DC to DC Converters in Portable Designs

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APPLICATION NOTE

Introduction

Portable designs powered from one Li-Ion battery embed more and more regulators to supply digital integrated circuits. Complex power management are used in mobile phones but additional single output converters are often needed to supply additional phone features or many other applications like MP3 players, digital cameras, wireless and DSL modems or USB powered devices that cannot be powered by the main Power IC.

Popular core voltages have dropped to 1.8 V, 1.5 V, 1.3 V, and even 0.9 V, in the meantime typical I/O voltages have dropped from 3.3 V to 2.5 V or 1.8 V. Consequently, to maintain high efficiency with low output voltages, designers must select buck converter architecture instead of linear regulators.

This powerful solution seems easy to integrate; however, a specific attention has to be kept in design to get a very efficient solution with a fast switching frequency. External parts requirements and board layout recommendations will be tackled in this document.

Optimized The External L-C Filter

Handheld design engineers are always facing the space requirement challenge. So, the size of a step down solution is a key requirement in portable designs. To get a smaller application, we could reduce inductor size and thickness by decreasing inductor value. In return, switching frequency of converter must increase. For now, integrated circuit technologies limit this frequency to 3 MHz to maintain a high efficiency solution, another key parameter to save battery life in portable design.

NCP1522B is one of the highest frequency DC–DC step-down regulators at 3 MHz. It is working with a couple of passive parts formed by an inductor and a capacitor, generally called the L–C filter. External parts selection is a key parameter – at high frequency – to keep an efficient step down solution in DC and AC results, some of them are listed below:

- Efficiency: operating at high frequency allows us to reduce inductor's value which also means a reduction of parasitic serial resistor and associated losses.
  If a very small solution is needed, NCP1522B is available in µDFN 0.55 mm thickness. Low profiles inductors are available on the market but their serial resistor must be carefully checked to keep good overall efficiency.

- Maximum Output Current: make sure your inductor can support the maximum current needed by the application according to inductor DC maximum current rating.

- Load Transients: in DC–DC converters, the function of output capacitance is to store energy. For some high load transient's requirements, the output capacitance is doubled to provide satisfactory load transient response.

- Loop Stability: to optimize solution size and facilitate device implementation, the compensation has been integrated. Using and implementing this kind of part is very easy, but the engineer has to follow rules to select external L–C filter. At 3 MHz, the integrated compensation is internally fixed and optimized for tank frequency of 50 kHz – in the case of NCP1522B – any inductor/capacitor couple that can fulfill Equation 1 requirement can be used:

$$f_t = \frac{1}{2\pi \sqrt{L \times C_{OUT}}} = 50 \text{ kHz} \qquad \text{(eq. 1)}$$

Table 1. NCP1522B µDFN, OUTPUT L–C FILTER RECOMMENDED

Inductance (L)	Output Capacitor (C_{out})
2.2 µH	4.7 µF
1.0 µH	10 µF

- Ripple Voltage; it depends on inductor and output capacitor selected values. Evaluate output ripple suppose to know inductor current flowing the inductance first, according to Equation 2 and Equation 3:

$$\Delta I_L = \frac{V_{OUT}}{L \times f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \qquad \text{(eq. 2)}$$

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{4 \times f_{SW} \times C_{OUT}} + ESR \right) \qquad \text{(eq. 3)}$$

Where:

ΔV_{OUT} – Output Voltage Ripple in PWM Mode

ΔI_L – Peak-to-peak Inductor Ripple Current

L – Inductor Value

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1

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C_{OUT} – Output Capacitor
ESR   – Output Capacitor Serial Resistor
f_{SW} – Switching Frequency

Both Equations 2 & 3 demonstrate that a fast DC to DC converter is a main advantage concerning ripple. Furthermore, ceramic capacitors with low ESR values will have the lowest output ripple voltage and are strongly recommended.

Smallest portable design must integrate a high switching frequency DC–DC converter. A good compromise must be done by designers between size, price and solution performance to configure the output L–C filter.

Configure The Output Voltage

For proper operation, a 4.7 μF decoupling capacitor and an external resistor bridge are also required for the application and gets the total part count to five. Although even if some common output voltages are internally fixed,

to propose several output voltages over wider range, DC–DC converters are typically adjustable by an external resistor bridge.

NCP1522B is adjustable in the 0.9 V to 3.3 V range. In this case, the feedback voltage (FB) is compared to a voltage reference internally set to 0.6 V. Below formula gives V_{OUT} value according to R1 & R2 choice:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \qquad \text{(eq. 4)}$$

V_{OUT} – Output Voltage (Volts)
V_{FB} – Feedback Voltage = 0.6 V
R1   – Feedback Resistor from V_{OUT} to FB
R2   – Feedback Resistor from FB to GND

For low power consumption and noise immunity, the resistor from FB to GND (R2) should be in the [100–600 kΩ] range. If R2 is 300 kΩ, the current through the divider will be 2.0 μA.
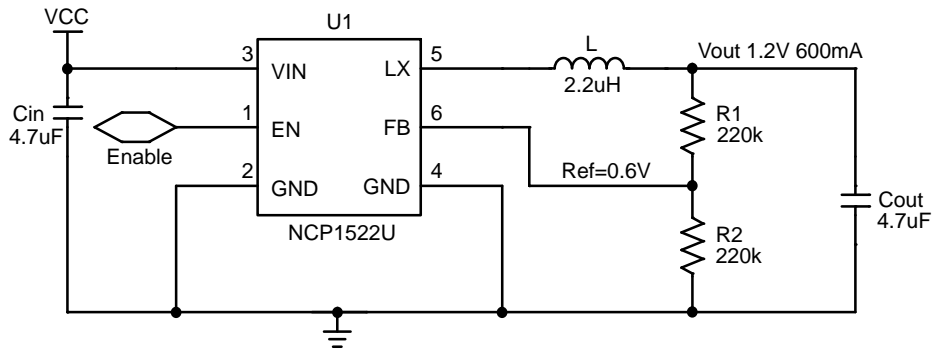

Figure 1. NCP1522B μDFN–6, Output Voltage Setting at 1.2 V

By selecting a symmetrical resistor bridge R1 = 220 kΩ and R2 = 220 kΩ, the output voltage is configured to 1.2 V. For better voltage accuracy, 1% or better resistors values are recommended.

Using Dynamic Voltage Management

Increased functionality and performance demands require better methods to extend battery life in portable application. Current techniques such as PFM mode to provide a low quiescent current keep saving battery life; however in order to reduce power consumption during processing time, most of the digital IC that are supplied by DC–DC converters can support dynamic power management. This is implemented by two ways: Dynamic Clock Management and Dynamic Voltage Management. A straightforward way to dynamically adjust the output voltage is to modify the resistor network value.

Figure 2 shows a simple way to switch between 1.2 V and 1.5 V on NCP1522B.

Q1 will switch R3 and so adjust the divider network value between 1.2 V and 1.5 V from the digital signal "Select". A low signal will turn ON Q1 and set the output voltage to 1.5 V while a high signal will turn OFF Q1 and set the output voltage to 1.2 V. Additional inverter U2 is only necessary if the Select voltage I/O is not powerful enough to switch Q1. For proper operation and to avoid over voltage or large under voltage during high to low and low to high voltage transition, Q1 turn on/turn off edge has been slowed down by adding R4/C4 network. This network can be adjusted and the final components value should be selected according to the end application requirements.
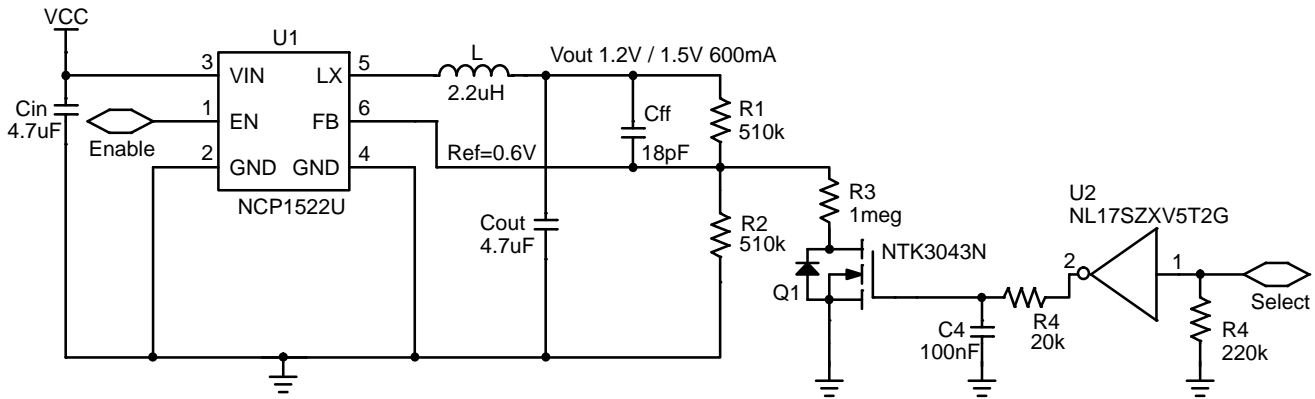
Figure 2. NCP1522B μDFN−6, 1.2 V to 1.5 V Dynamic Voltage Management

We can get output voltage by replacing R2 by REQ in formula (1), where

REQ = FB to GND Equivalent Resistor

Using Equation 1: R1 and REQ calculation for each voltage is straightforward. By using standard resistor in the range [100 kΩ, 600 kΩ], REQ will be:
- REQ = 510 kΩ for Vout = 1.2 V
- REQ = 330 kΩ for Vout = 1.5 V

Given these values, we will select R2 = 510 kΩ. R3 calculation is also straightforward. Knowing REQ = 330 kΩ and R2 = 510 kΩ, R3 will be R3 = 1 MΩ.

To optimize output voltage accuracy, we recommend selecting 1% or better resistors value.

Board Layout Recommendation

Implementing a high frequency DC−DC converter requires respect of some rules.

Good layout is key to prevent switching regulators to generate noise to application and to themselves. Like for any close loop systems, feed back pin protection against any external parasitic signal coupling requires special care. As portable digital circuits consume a large amount of current, the loop formed by high current path from the battery to the ground plane and so called the current loop must be particularly checked by designers from the input to the output of the device.

A four layer PCB with a ground plane and a power plane or more is generally implemented on mobile phone application. However others applications which also embed these circuits can not meet these recommendations. In this case, a specific attention must be paid to the board layout:

- Prefer having a power plane and a ground plane and always think about the parasitic
- Use single point grounding
- Keep input capacitor close to the IC with low inductance traces
- Always avoid vias on current loop. They have high inductance and resistance. If vias are necessary always use more than one in parallel to decrease parasitic
- For high di/dt signals (V_{IN} & V_{OUT}): keep traces short, wide and closely spaced. This will reduce stray inductance and decrease the current loop area to prevent from EMI
- For high dv/dt signals (SW): keep copper to a minimum to prevent making unintentional parallel plate capacitors with other traces or to ground plane. Best to route signal and return on same plane
- Keep trace from switching node pin to inductor short
- Use short and large traces when large amount of current is flowing
- Output voltage feedback sampling must be taken right at output capacitor and shielded
- Isolate analog signal paths from power paths
- Do not use auto-router
- Think about thermal

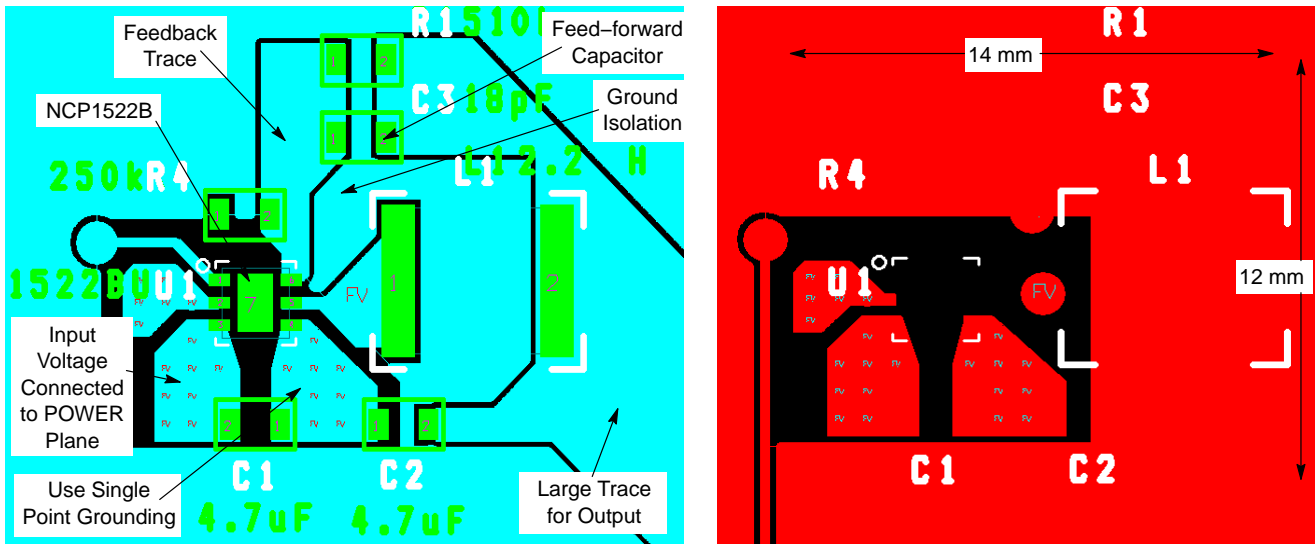Figure 3 shows recommended layout implemented on NCP1522B μDFN−6 four-layer demonstration board.

Figure 3. NCP1522B μDFN–6, Top & Bottom Layout Routing

These figures show the integration of five components around the NCP1522B, a 3 MHz switching regulator. A smaller solution can be achieved with a smaller inductor (down to 1 μH).