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AND8332/D

Calculating External Components

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APPLICATION NOTE

Scope

This document describes how to calculate external component values for the NCP1080, NCP1081, NCP1082 and NCP1083 integrated PoE−PD and DC−DC converter controller and elaborates on implementation details, without delving into theoretical details. Examples are illustrated with the use of the supplied calculation scripts.

Introduction

The NCP108x are robust, flexible and highly integrated solutions targeting demanding medium− and high−power Ethernet terminals. The combination of an enhanced PoE−PD fully compliant with the IEEE 802.3af and IEEE 802.3at specifications for the NCP1081 with a highly efficient SMPS, in a single device, offer new opportunities for the design of products directly supplied over Ethernet lines. Elimination of the need for any local power adaptor or power supply drastically reduces the overall installation and maintenance cost.

ON Semiconductor's unique process and design enhancements allow the NCP1081 to power PoE systems with up to 40 W. The NCP1080 is designed to support power levels up to 15.4 W, according to the IEEE 802.3af specification.

The hot swap PD switch and programmable current limit are designed for high power applications. The handshaking for power requirements for the IEEE 802.3at standard supports Type 1 and Type 2 classification with Layer 1 single and dual events as well as Layer 2 classification. Additional proprietary handshaking is implemented as a fifth class to program with an external resistor.

The ON Semiconductor vertical N−channel DMOS device is inherently robust for fast transients. This results in cable ESD levels of 2 kV (on the RJ45 connector) and HBM ESD levels of 2 kV.

The PWM controller facilitates single−ended SMPS power supply topologies such as fly−back and forward converters. The control scheme is based on peak current control. This control allows line feed−forward, cycle−by−cycle current limitation and simple feedback compensation.

The inrush current limit, operational current limit, operating frequency and soft start time are programmable, depending on the requirements of the application.

This application note attempts to give a step−by−step approach to the implementation of a stable power supply. All aspects of the process from converter architecture to the PCB layout guidelines are explained, while trying to minimize the mathematics necessary to perform the steps. Converter transfer functions are not deduced as literature on these topics is widely available.

An isolated fly−back topology is described in this document. Other topologies are discussed in separate application notes.

Although the document mostly references the NCP1081, the discussed principles and calculations for the external components are equally valid for the NCP1080, NCP1082 and NCP1083.

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CURRENT MODE CONTROL, ISOLATED FLY−BACK CONVERTER

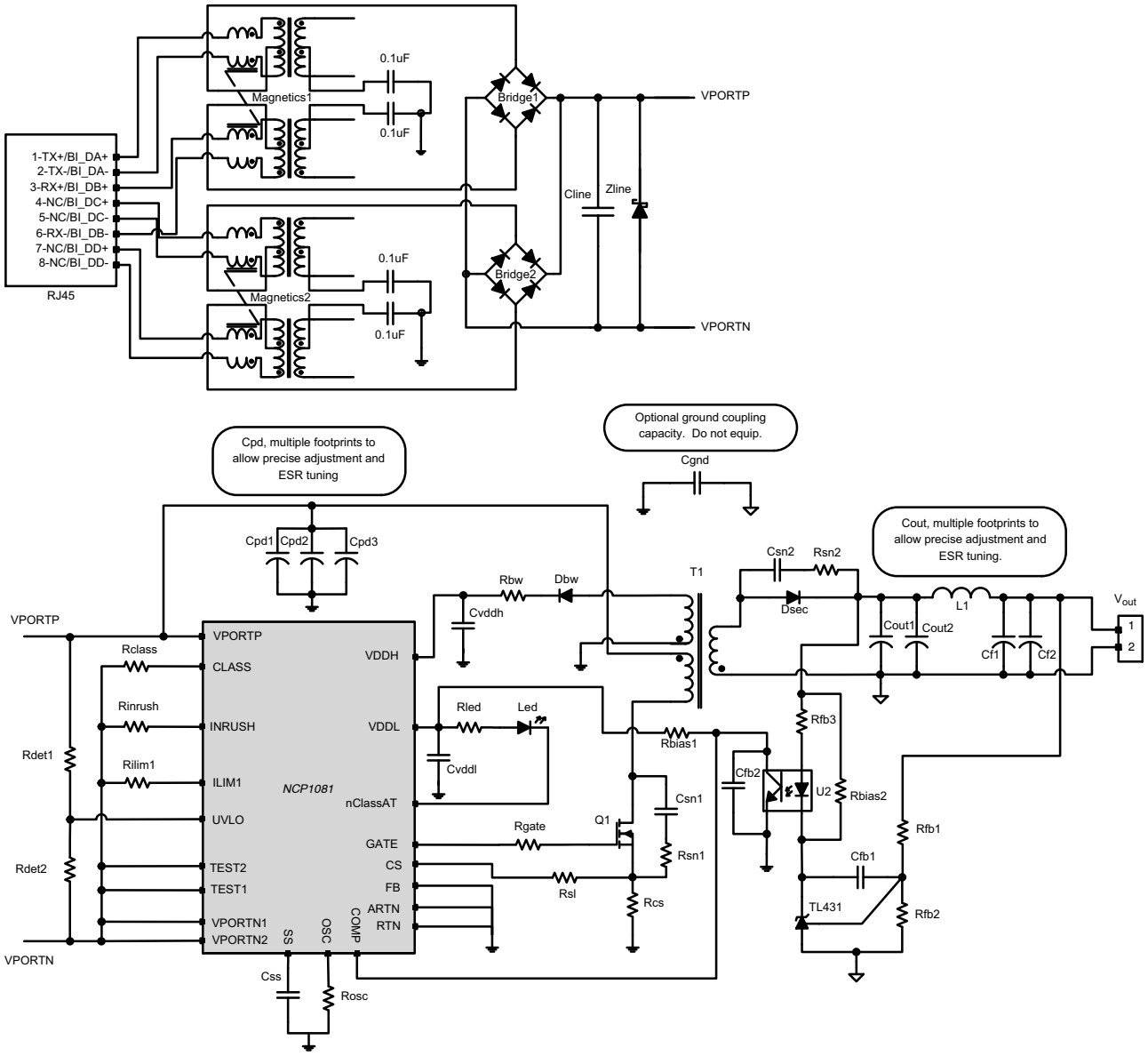

Figure 1. Isolated Fly−back Converter with Bias Winding and Diode Bridge

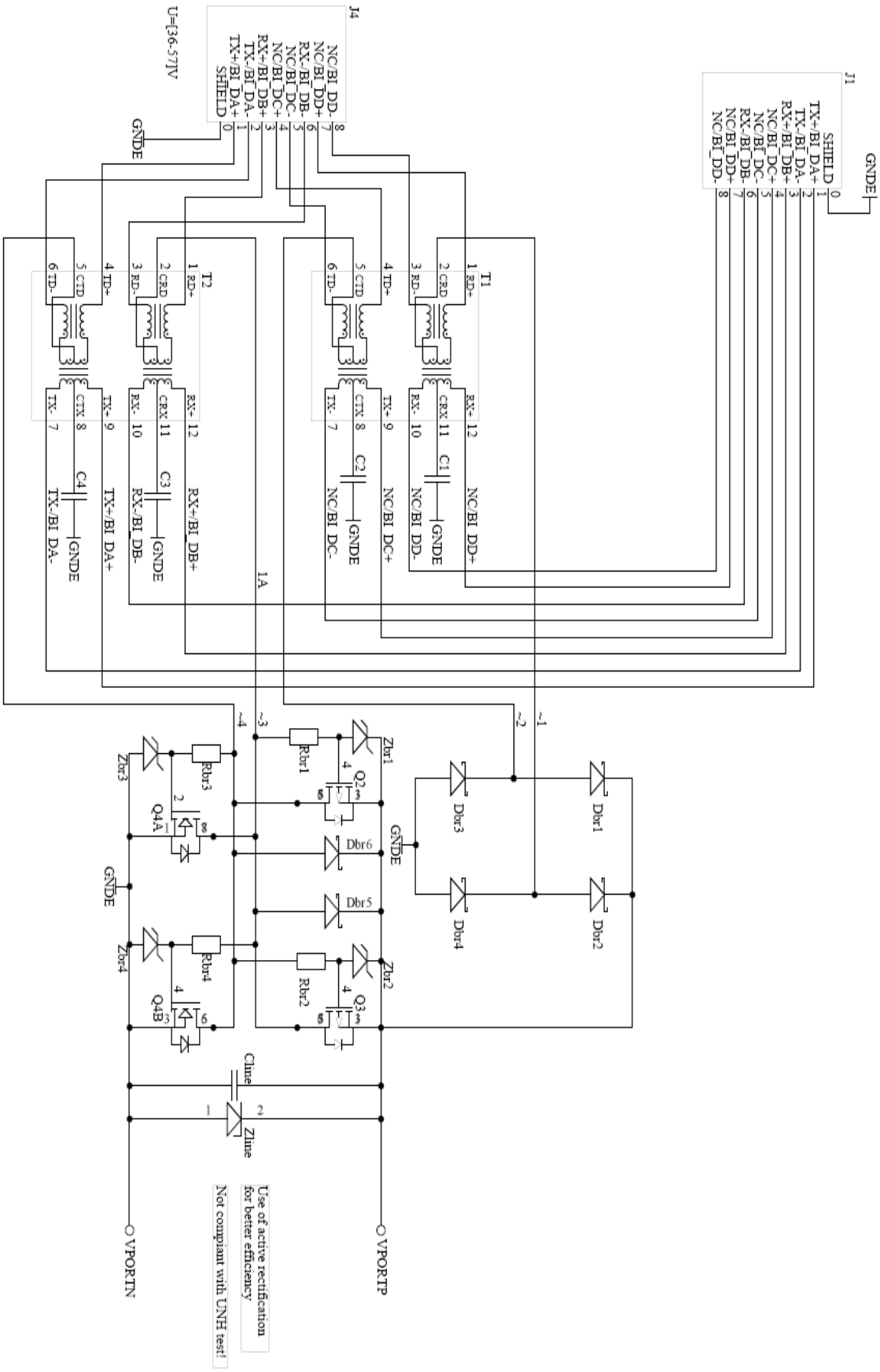

Figure 2. Primary Circuitry of the Flyback Converter Using Active Rectification for Better Overall Efficiency

The Isolated Fly−back Converter with Bias Winding and diode bridge is shown in Figure 1. The primary circuitry can use also the active rectification bridge for better overall converter efficiency(Figure 2).

We will calculate or decide on the values for the components listed in Table 1.

Table 1. LIST OF COMPONENTS

Name	Description
$C_{out1,2}$	DC−DC output capacitor
$C_{pd1,2,3}$	DC−DC input capacitor
R_{cs}	Resistor for current sensing
R_{sl}	Resistor for extra slope compensation (optional)
R_{class}	Resistor setting the classification current level
R_{inrush}	Resistor setting the inrush current limitation level
R_{ilim1}	Resistor setting the operational current limit level
C_{line}	Input line capacitor
Z_{line}	Tranzorb (transient voltage suppression diode)
R_{det1}	Detection signature and external UVLO programmable resistor 1
R_{det2}	Detection signature and external UVLO programmable resistor 2
C_{sn1}	Snubber capacitor for the switching transistor
R_{sn1}	Snubber resistor for the switching transistor
C_{sn2}	Snubber capacitor for the power diode
R_{sn2}	Snubber resistor for the power diode
R_{fb1}	Resistor for the voltage feedback system
R_{fb2}	Resistor for the voltage feedback system
R_{fb3}	Resistor for the voltage feedback system
R_{bias1}	Resistor for extra biasing current in the opto−coupler (optional)
R_{bias2}	Resistor for extra biasing current in the TL431 shunt regulator (optional)
C_{fb1}	Capacitor for the voltage feedback system
C_{fb2}	Capacitor for the voltage feedback system
R_{bw}	Current limiting resistor for bias winding usage
R_{led}	Current limiting resistor for nCLASS_AT LED
$C_{1..4}$	Capacitors for noise reduction on the Ethernet magnetics
C_{vddl}	Decoupling capacitor for VDDL low voltage regulator
C_{vddh}	Decoupling capacitor for VDDH high voltage regulator
R_{osc}	Resistor setting the PWM switching frequency

PoE−PD SIDE DESIGN

Detection and UVLO Setting

During the detection phase the input impedance of the PD device is measured by the PSE and should, according to IEEE 802.3af/at, be included between 23.75 kΩ and 26.25 kΩ. The NCP108x can either use its internal under voltage lockout setting of 37.5 V, or an external resistor divider can be used to tune the UVLO. The NCP108x will not allow operation of the power converter unless the sensed line voltage is above the UVLO pin limit (internal or external). R_{det} or the sum of R_{det1} and R_{det2} should hence be 25.5 kΩ. The UVLO limit, $V_{uvlo\_on,}$ should be configured to the low−line design parameter of the converter. In most cases this will be 36 V. Use Equation 1 to calculate R_{det1} and R_{det2}.

$$R_{det2} = \frac{V_{uvlo\_ref}}{V_{uvlo\_on}} = 25.5\ k\Omega \qquad \text{(eq. 1)}$$

and

$$R_{det2} + R_{det1} = 25.5\ k\Omega$$

where V_{uvlo_ref} = 1.2 V

Classification

IEEE 802.3af/at specifies five power classes (0 − 4). During classification the PSE equipment will sense the current that flows through R_{class} to determine what power consumption class the PD equipment belongs to. Table 2 indicates what resistor value to use for R_{class} for the different classes. Note that a fifth non−standard high−power class is defined to enable the NCP1081 high power capabilities.

Table 2. IEEE 802.3AF/AT POWER CLASSES

R_{class} (Ω)	Power Class
10k	Class 0: 15.4 W
130	Class 1: 4 W
69.8	Class 2: 7 W
44.2	Class 3: 15.4 W
30.9	Class 4: IEEE 802.3at device class
22.1	Class 5: NCP1081 class, power levels exceeding IEEE 802.3at levels

The IEEE 802.3at specification describes a second classification event to let the application know if higher power (higher than IEEE 802.3af power levels) can be switched on. This second classification is either supported by hardware (NCP1081, not NCP1080) or by software on a network processor, powered by the NCP1081. The PSE

decides which classification will be executed. When the hardware classification is complete the nClassAT pin is low. When the hardware classification is not executed, meaning that either the PSE is IEEE 802.3af compliant or that the high power capabilities will be exchanged by the network protocols, the nClassAT will remain high. The LED connected to nClassAT will only light when the second event hardware classification has completed.

Programmable Current Limitation

Inrush Current Limit

Table 3 lists the typical values for R_{inrush}.

Table 3. PROGRAMMABLE INRUSH CURRENT

R_{inrush} (kΩ)	Min	Typ	Max	Unit
150	95	125	155	mA
57.6	260	310	360	mA

Operational Current Limit

Table 4 lists the typical values for R_{ilim1}.

Table 4. USEFUL VALUES FOR R_{ilim1}

R_{ilim1} (kΩ)	Min	Typ	Max	Unit
84.5	450	510	570	mA
66.5	600	645	690	mA
56.0	720	770	820	mA
36.5	970	1100	1230	mA

Note that non−standard compliant current can be achieved by lowering Rilim1. Keep in mind that the absolute maximum rating for the current through the NCP1081 is 1.23 A. Note that the board layout should allow proper thermal conductivity to avoid exceeding the maximum junction temperature.

Diode Bridge and C_{line}

C_{line} should be a 100nF ceramic with low ESR (< 0.1 Ω) and 20% tolerance. The diode bridge should be dimensioned to allow the maximum current that is chosen for the design.

Power Stage Design

Decide on the System Parameters and Transformer to Use

Table 5. INPUT PARAMETERS

Parameter	Description
V_{in}	Ethernet input voltage. Take into account the drop over the diode bridge.
V_{out}	The desired output voltage
L_{prim}	The inductance of the primary of the transformer
N	The transformer turns ratio
P_{out}	The desired output power
V_{ripple}	The desired output ripple
f_s	The desired PWM switching frequency

The switching frequency (f_s) supported by the NCP108x ranges up to 500 kHz. Higher frequencies reduce the size of the transformer but may have adverse effects on other parameters such as switching loss. The designer will have to find an optimum between power consumption and material cost.

Note that this entire design guideline is focused on the implementation of a current measurement feedback loop on top of voltage feedback.

Configure the Switching Frequency

The PWM switching frequency is configured by an external resistor R_{osc}. R_{osc} is calculated using Equation 2, below.

$$R_{osc} = \frac{38600}{f_s} k\Omega \qquad \text{(eq. 2)}$$

Where f_s (kHz) the desired switching frequency

Continuos Conduction Mode (CCM) or Discontinuos Conduction Mode (DCM)

Note that the NCP108x is designed to operate in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Pros and cons exist for both modes of operation. In CCM, the ripple current is smaller and possibly a smaller output capacitance can be used. In DCM, the conduction losses are higher (because the currents are higher) but the switching loss is smaller (due to current being zero when switch opens). Also in DCM, a smaller inductor or transformer can be used, leading to lower leakage inductance. On the other hand, the AC losses in the DCM transformer may become dominant. Due to the higher currents in DCM, the DCM converter creates more EMI.

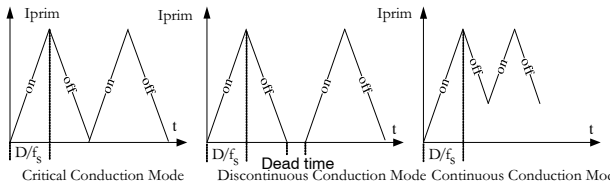

Figure 3. CCM/DCM

Switching frequency, transformer induction and load are parameters that make the converter run in one or the other mode. The transition from one to the other mode depends on these three values. The point where the system transitions from DCM to CCM is called the critical conduction mode. Correspondingly, we can define the critical load, frequency and induction.

$$R_C = \frac{2 \cdot L_c \cdot f_s \cdot n^2}{(1 - D)^2} \qquad L_C = \frac{R_c \cdot (1 - D)^2}{2 \cdot f_s \cdot n^2}$$
$$F_C = \frac{R_C (1 - D)^2}{2 \cdot L_C \cdot n} \qquad \text{(eq. 3)}$$

The design procedure described in the following sections focuses on CCM operation. Equation 3 can be used to find out how far the design is from running in one or the other mode.

Calculate the Duty Cycle

First calculate the converter duty−cycle D from the assumption that in one full cycle the secondary voltage should be zero and thus equal the shaded areas of Figure 4 where T is the period.

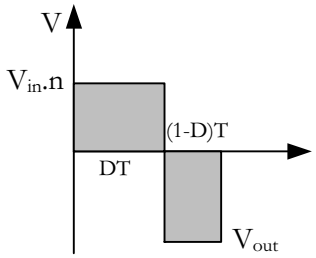

Figure 4. Determining the Duty−Cycle

$$\frac{V_{out}}{V_{in}} = n\frac{D}{1 - D} \qquad \text{(eq. 4)}$$

or

$$D = \frac{V_{out}}{V_{out} + nV_{in}}$$

The NCP108x supports duty cycles up to 0.80. Use Equations 5 and 6 and the data of the chosen transformer to calculate whether or not the maximum duty cycle can be met. Note that the duty cycle is at a maximum when the input voltage is at its lowest (low line), therefore we use V_{in_min}.

Also take into account the forward voltage drop of the diode (typically 0.5 V).

$$V_{in} T_{on} N_1 = V_{out} T_{off} N_2$$
$$\Rightarrow \frac{N_1}{N_2} = \frac{D_{max}}{1 - D_{max}} \frac{V_{in\_min}}{V_{out}} \qquad \text{(eq. 5)}$$
$$\Rightarrow D_{max} = \frac{\frac{N_1}{N_2}}{\frac{N_1}{N_2} + \frac{V_{in\_min}}{V_{out}}} \qquad \text{(eq. 6)}$$

Calculate the Various Currents

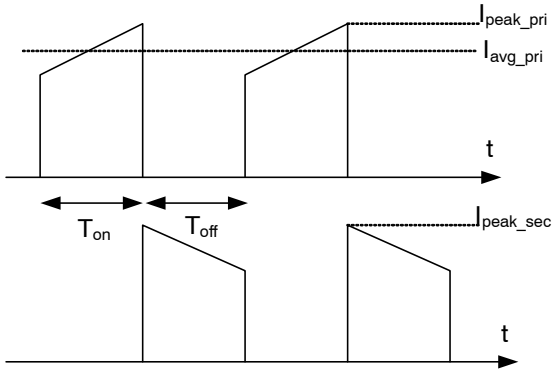

Figure 5. Primary and Secondary Currents (ccm)

Average currents, during T_{on}:

$$I_{avg\_pri} = \frac{P_{out}}{V_{in} \cdot D \cdot \eta_{transformer}}$$
$$I_{avg\_sec} = \frac{P_{out}}{V_{out} \cdot (1 - D)} \qquad \text{(eq. 7)}$$

Magnetizing currents:

$$I_{mag\_pri} = \frac{V_{in} \cdot D}{L_{pri} \cdot f_s}$$
$$I_{mag\_sec} = \frac{(V_{out} + V_{diode}) \cdot (1 - D)}{L_{sec} \cdot f_s} \qquad \text{(eq. 8)}$$

Peak currents:

$$I_{peak\_pri} = I_{avg\_pri} + \frac{I_{mag\_pri}}{2}$$
$$I_{peak\_sec} = I_{avg\_sec} + \frac{I_{mag\_pri}}{2} \qquad \text{(eq. 9)}$$

RMS currents:

$$I_{rms\_pri} = \frac{P_{out}}{V_{in} \cdot \sqrt{D} \cdot \eta_{transformer}} \quad \text{(eq. 10)}$$

$$I_{avg\_sec} = \frac{P_{out}}{V_{out} \cdot \sqrt{(1 - D)}}$$

Output Capacitance and Filter

Use the duty−cycle D to obtain a value for C_{out}.

$$C_{out} = \frac{P_{out}}{V_{out}} \frac{2D}{f_s V_{ripple}} \quad \text{(eq. 11)}$$

The parasitic effective series resistance (R_{esr}) of the capacitor C_{out} affects the output voltage ripple the most. The ripple caused by R_{esr} is an order of magnitude larger than the ripple caused by having a small output capacitance. The required output ripple specification will not be met by using an output capacitor only.

Take the closest standard value for the capacitor with the lowest R_{esr}. It is better to deviate from the calculated capacitance value when there's another capacitor value with lower ESR. Equally important is to measure the chosen capacitor or parallel capacitors on an impedance analyzer to make sure the ESR is correct.

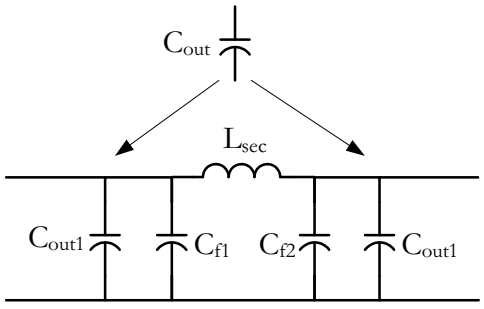

Figure 6. Adding an Additional Ripple Filter

An additional L−C filter should be added to meet the ripple specification. A large capacitor should remain at the side of the load to cope with load changes and to make sure no stability issues arise from capacitive loading (due to shift of the filter resonance frequency). Therefore, split the output capacitance in two, or take an additional one (depending on the ESR which should not increase) and place an inductor in between to create an L−C filter.

The damping of the L−C filter is given by Equation 12. This equation can be rewritten into Equation 13 which gives the product of L and C.

$$\frac{V_{ripple}}{V_{ripple\_esr}} = \frac{Z_C}{Z_C + Z_L} \quad \text{(eq. 12)}$$

with

$$Z_C = \frac{1}{2\pi f_s C}$$

and

$$Z_L = 2\pi f_s L$$

or

$$LC = \frac{V_{ripple\_esr} - V_{ripple}}{V_{ripple}(2\pi f_s)^2} \quad \text{(eq. 13)}$$

V_{ripple} is the desired output voltage ripple and V_{ripple_esr} is the voltage ripple that is generated over the ESR of the output capacitor. The approximate current that flows through the ESR resistor is the secondary peak current of the converter, leading to Equation 14.

$$V_{ripple} = I_{peak\_sec} R_{esr} \quad \text{(eq. 14)}$$

Choose a value for L and calculate the value for C. Next, make sure the resonance frequency (Equation 15) is at least two or three times higher than the cross−over frequency of the closed loop converter (to make sure the resonant peak stays well below 0 dB), but still lower than the switching frequency of the regulator (to make sure switching noise is filtered).

$$f_{LC} = \frac{1}{\pi\sqrt{L2C}} \quad \text{(eq. 15)}$$

Stability Analysis of the Converter in CCM

Equation 16 shows the transfer function of the fly−back converter in current controlled mode of operation. Note that adding current measurement in the feedback loop has advantages on top of implementing only voltage measurement feedback:

- The feedback is immediate, current can be limited in the same cycle,
- The order of the transfer function is reduced, leading to a system that is easier to stabilize,
- The phase margin is better.

$$T_{power\_ccm}(s) = K\frac{\left(1 + \frac{s}{\omega_{zesr}}\right) \cdot \left(1 - \frac{s}{\omega_{zrhp}}\right)}{1 + \frac{s}{\omega_p}} \quad \text{(eq. 16)}$$

where

$$\omega_{zesr} = \frac{1}{R_{esr} \cdot C_{out}} \quad \text{(eq. 17)}$$

ω_{zesr} is a zero originating from the output capacitor and its equivalent series resistor.

$$\omega_{zrhp} = \frac{R_{load} \cdot (1 - D)^2}{DL_{pri}n^2} \quad \text{(eq. 18)}$$

ω_{zrhp} is a right half plane zero can be explained by the phenomenon that when there's a sudden load increase, the duty cycle will increase instantaneously, building up higher current but the voltage will drop temporarily until the required current is present. Since this zero is located in the

right half plane, this leads to a gain boost and a phase lag (which is not desirable and can lead to an unstable system).

$$\omega_p = \frac{1 + D}{R_{load}C_{out}} \quad \text{(eq. 19)}$$

ω_p , a dominant pole originates from the load and output capacitor.

$$K = \frac{R_{load}(1 - D)}{nR_{cs}A_V(1 + D)} \quad \text{(eq. 20)}$$

where A_v = 2 for NCP108x

To investigate and improve the stability of the DC−DC converter, the technique of frequency response compensation is used.

This technique is based on the fact that any linear system in steady state will show at its output a sine wave with amplitude and phase when it is excited at its input with a sine wave of given frequency, amplitude and phase. The amplitude and phase of the output signal may be different than those of the input signal, however the input and output frequency will be the same.

This technique uses a Bode plot to assess the stability criteria. A Bode plot consists of two drawings. One drawing plots the magnitude of the output signal over the input signal, using logarithmic scale. The other drawing plots the phase of the output minus the phase of the input, using logarithmic scale.

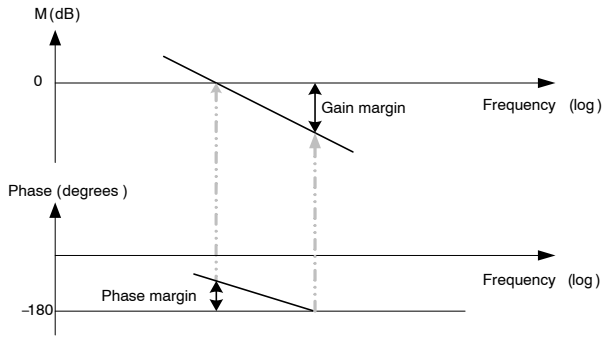

Figure 7. Phase and Gain Margin

A closed loop system is stable if the open loop frequency response shows a gain of less than 0 dB at the frequency where the phase shift is 180°. Gain margin is the value by which the gain of the system can be increased, while keeping the phase at −180° (Note 1), before the system becomes unstable. Phase margin is the value by which the phase of the system can be increased, keeping the gain at 1, before the system becomes unstable.

A bigger phase margin lowers the peaking on transitions and a higher system bandwidth increases the speed of the system. The DC error (or static, or steady state error) is reduced when the low frequency gain is increased.

Use Equation 16 to plot a Bode diagram and inspect where stability issues may arise.

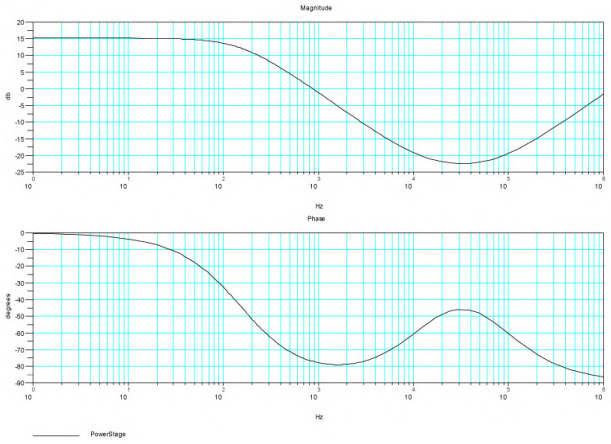

Figure 8. Bode Plot of the Power Sate of a 30 W 3.3 V Fly−back Converter (note the poor gain at DC)

DC Gain Boosting and Phase Margin Insurance

When we translate the stability requirements to our fly−back converter design, we should have a system with high phase margin (around 60°), high bandwidth (unity gain or cross−over frequency as high as possible but still far enough from the switching frequency), a high gain at DC, and a high attenuation at high frequency.

This is achieved by adding a control and compensation network which uses an opto−coupler for isolation, introduces an extra zero, two poles (one at DC) and has following transfer function:

$$T_{comp}(s) = \frac{CTR \cdot \left(5K//R_{bias1}\right)}{R_{fb3}} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{R_{fb1} \cdot C_{fb1} \cdot s \cdot \left(1 + \frac{s}{\omega_p}\right)} \quad \text{(eq. 21)}$$

The goal of the compensation network is to set the gain criteria while affecting the phase margin as least as possible. (Proportional−integral (PI) plus high−frequency pole compensation)

1. Note that the systems discussed here, all have negative feedback like most feedback systems, hence the −180° of the negative feedback together with an additional 180° shift would yield 360° overall shift, a positive feedback, unstable system.

Step 1: Define the Compensation Circuit Cross−Over Frequency

Rule of thumb: The converter should have a cross−over frequency

$$f_{cross} < \min\left(\frac{f_{zrhp}}{3}, \frac{f_s}{5}, f_{zesr}, f_{optocoupler}\right) \quad \text{(eq. 22)}$$

where:

- f_{zrhp} is the frequency of the right hand plan zero of the open loop fly−back converter derived from Equation 18
- f_s is the converter's switching frequency
- f_{zesr} is the frequency of the zero introduced by the output capacitor's series resistance, given by Equation 17
- $f_{optocoupler}$ is the frequency indicating the bandwidth of the chosen opto−coupler

Step 2: Phase Margin Insurance, Define the Pole and Zero Frequency of the Compensation Circuit

Instead of using a Type II or Type III compensation network with operational amplifier, often an equivalent but cheaper network with TL431 voltage reference is used as an error amplifier in combination with an opto−coupler for isolation.

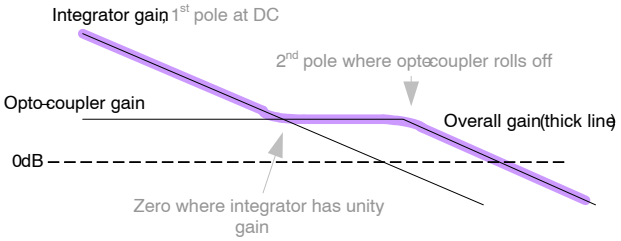

Figure 9. Compensation Network Gain Approximation

At low frequencies C_{fb1} and R_{fb1} act like an integrator. The overall gain of the integrator is the product of the integrator gain and the opto−coupler gain. The compensation zero is located at the point where the integrator crosses over.

At mid−range frequencies, the opto−coupler becomes dominant because the integrator with the TL431 has crossed unity gain. The gain is determined by the opto−coupler gain, R_{fb3} and the NCP108x 5 kΩ internal pull−up in parallel with R_{bias1}.

At high frequencies the pole of the opto−coupler becomes dominant. Make sure that the bandwidth of the opto−coupler is as high as possible. R_{bias1} in parallel with the 5 kΩ internal resistor should be tuned such that the opto−coupler is sufficiently biased. We want to configure a known compensation pole by inserting C_{fb2}.

We make sure that between the zero and the pole of the compensation network we have a unity gain of the closed loop system with the desired phase margin. Use the Bode plot of the open loop system to find the phase margin at the cross−over frequency. The pole of the compensation network needs to be K times larger and its zero needs to be K times smaller than the cross−over frequency. With K given by:

$$K = \tan\left(\frac{boost}{2} + 45\right) \quad \text{(eq. 23)}$$

boost = desired phase margin − actual phase margin + 90

Now, choose a value for R_{fb1} and use Equations 24 and 25 to calculate C_{fb1} and C_{fb2}.

$$f_z = \frac{1}{2\pi \cdot R_{fb1} \cdot C_{fb1}} \quad \Rightarrow C_{fb1} = \frac{1}{2\pi R_{fb1} f_z} \quad \text{(eq. 24)}$$

$$f_p = \frac{1}{2\pi \cdot \left(5K // R_{bias1}\right) \cdot C_{fb2}}$$

$$\Rightarrow C_{fb2} = \frac{1}{2\pi\left(5K // R_{bias1}\right) f_p} \quad \text{(eq. 25)}$$

Step 3: Gain Adjustment

First we need to find out, using the Bode plot, what the gain (A_0) is of the open loop system at f_{cross}. The gain of the compensation network is given by:

$$CTR \cdot \frac{5K // R_{bias1}}{R_{fb3}} \quad \text{(eq. 26)}$$

where CTR is equal to the current transfer ratio of the opto−coupler. The Rbias2 and Rfb3 resistors connected to the opto−coupler and the TL431 shunt regulator should be carefully tuned to guarantee a sufficient operating current for the TL431 (typical TL431 require minimum 1 mA as bias current). The gain of this network needs to be sufficiently high to react abruptly on reaching the output voltage. It is good practice to measure the performance of this network prior to switching on the NCP1081.

Now equalize the compensation network gain to the inverse of the open loop gain at cross−over frequency and calculate R_{fb3}.

$$CTR \cdot \frac{5\ k\Omega // R_{bias1}}{R_{fb3}} = \frac{1}{A_0} = A_{comp} \quad \text{(eq. 27)}$$

Step 4: Set the TL431 DC Regulation Voltage

The shunt regulator compares the output voltage divider to an internal V_{tl431} reference and generates an error voltage which is applied to the cathode of the opto−coupler. The output resistor divider made of R_{fb1} and R_{fb2} should be calculated to provide exactly V_{tl431} to the reference pin of the TL431 when the power converter output voltage equals the desired regulated Vout1 voltage. Since R_{fb1} was already chosen before, R_{fb2} can be calculated easily.

$$R_{fb2} = \frac{V_{tl431} \cdot R_{fb1}}{V_{out} - V_{tl431}} \quad \text{(eq. 28)}$$

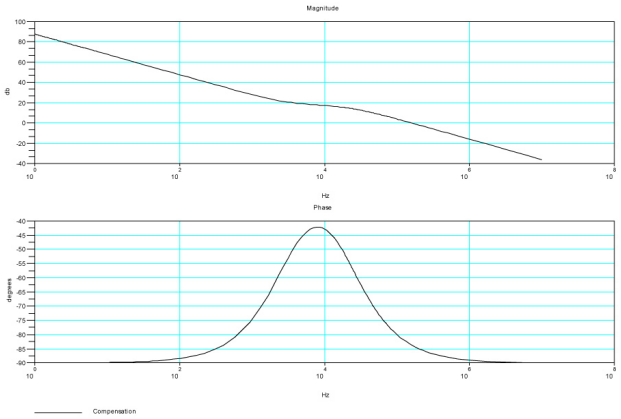

Figure 10. Bode Plot for a 30 W 3.3 V Converter Compensation Network

Step 5: Check the Compensation Network Performance

The theoretically derived component values need to be checked on the real design. Two separate measurement techniques are proposed to measure the frequency response of the entire loop and that of the converter without the compensation network. Most probably, more than one iteration will be required to get it right.

Measure the Full Loop Frequency Response, Including the Compensation Network

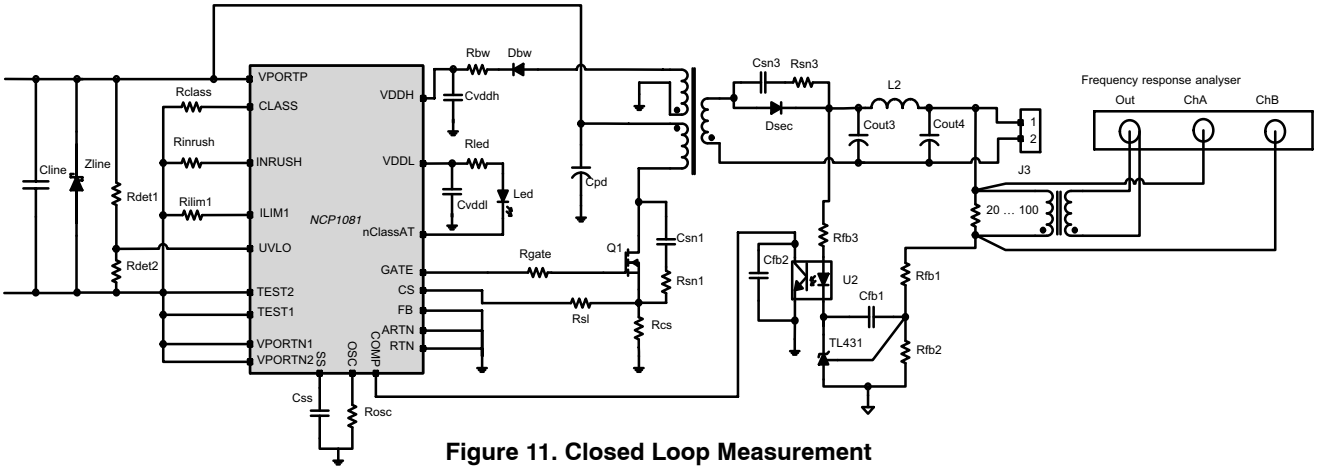

Figure 11. Closed Loop Measurement

The proposed technique measures the entire loop frequency response without breaking the loop. The standard way of measuring this would be to break the loop and inject and measure the signal at impedance matched cutting points.

Measure the Frequency Response of the Power Converter Only, Without the Compensation Network

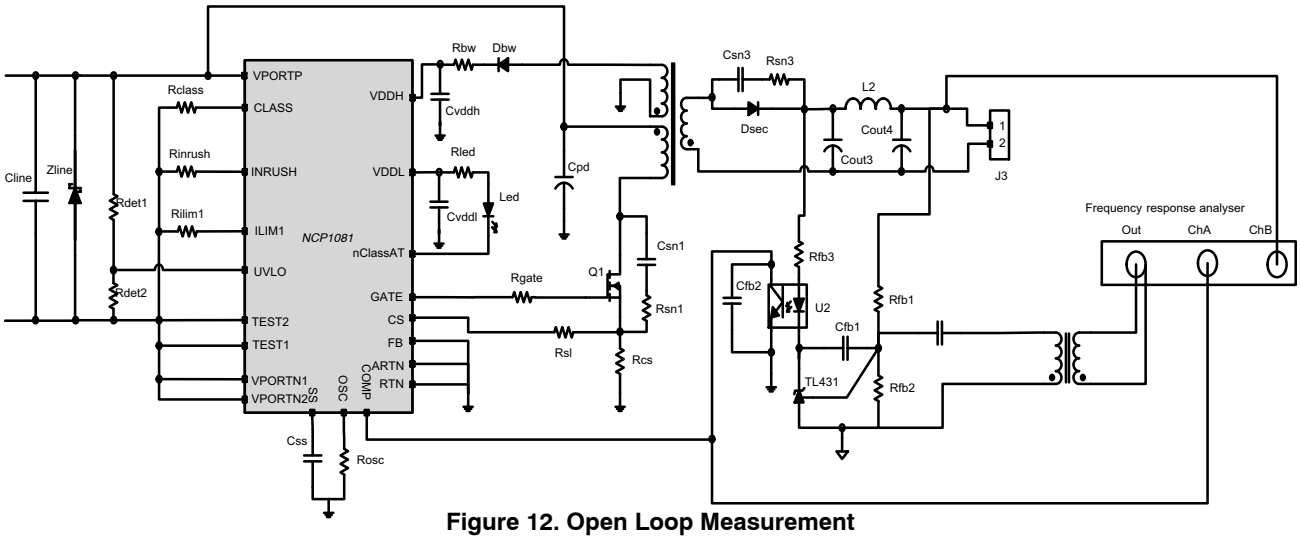

Figure 12. Open Loop Measurement

This measurement technique measures the loop without having to break it, but at the same time, the network between measurement point A and B is eliminated. In this case we measure the frequency response of the power converter, without the compensation network.

Slope Compensation

To overcome sub−harmonic oscillations and instability problems that exist with constant frequency current mode control converters running in continuous conduction mode (CCM) and when the duty cycle is close or above 50%, the NCP108x integrates a current slope compensation circuit.

This sub−harmonic oscillation phenomenon can be understood by looking at Figure 13. The current in the primary transformer is illustrated for two different duty cycle cases, assuming a current mode PWM controller without slope compensation. When D > 0.5, a small disturbance on the primary current causes a duty cycle asymmetry between consecutive pulse cycles. This error increases with every cycle (due to the fixed frequency operation) and will lead to oscillation in the regulation loop at f_s / 2. When D < 0.5 this disturbance diminishes cycle by cycle.

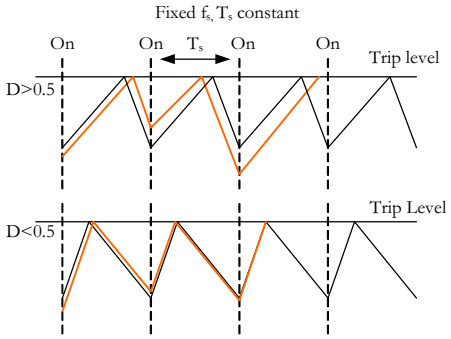

Figure 13. Current Control Instability at D > 0.5, for PWM Controller not using Slope Compensation

These possible oscillations are modeled by another transfer function which will be multiplied with the transfer function of the power stage, listed in Equation 16.

$$T_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n{}^2}} \qquad \text{(eq. 29)}$$

where

$$\omega_n = \pi \cdot f_s \qquad Q_p = \frac{1}{\pi(m_c(1 - D) - 0.5)}$$

$$m_c = 1 + \frac{s_e}{s_n} \qquad s_e = \frac{V_{slope-pp}}{T_s} \qquad s_n = \frac{V_{on}}{L} A_{sense}$$

S_e is the compensation ramp slope, given by the compensation voltage over the switching period.

S_n is the slope of the sensed current waveform, given by the voltage over the coil when the switch is on, times the current measurement gain, divided by the inductance. When only the current sense resistor is used, $A_{sense} = R_{cs}$.

The transfer function shows a peak at $f_s/2$. This peaking could cause the gain to go above 0 dB again, even after we've done all the compensation (setting the cross−over frequency and phase margin improvement), rendering the system unstable once more. The height of the peak is determined by Q_p. The lower Q_p, the bigger the damping is and the lower the peak is.

This damping is achieved by adding a slope to the comparator trip level. Figure 15 shows that, now even with D > 0.5, the error reduces every cycle.

The necessary Slope compensation can be calculated using the following formula:

$$dV_{slope} = nR_{cs}\frac{V_{out}}{2L_{pri}n^2}dt \qquad \text{(eq. 30)}$$

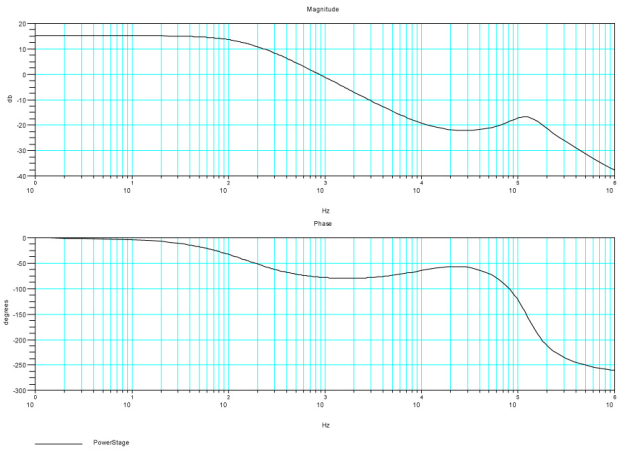

Figure 14. Same Converter as in Figure 7, but Now Including the High Frequency Effect of Current Control

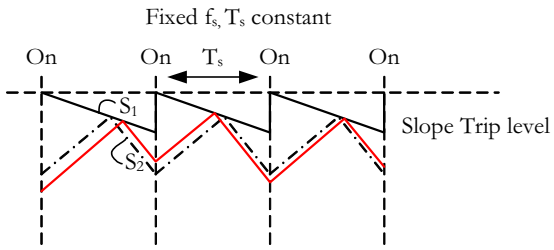

Figure 15. How Slope Compensation Helps

where

$$dt = \frac{1}{f_s} \quad \text{(eq. 31)}$$

and

$$R_{cs} = \frac{0.36}{I_{PriPeak} 1.2}$$

where

$$I_{PriPeak} = \frac{V_{in}}{L_{pri}} \frac{D}{f_s}$$

0.36 V Is the threshold voltage of the current comparator, factor 1.2 adds margin to the measurable current. This margin is required because there's an additional voltage drop over R_{sl}.

Since the NCP1081 integrated a slope compensation of 110 mV over 1 period, the remaining necessary slope can be obtained by adding an external Rsl resistor between the CS pin and Rcs resistor.

$$R_{sl} = \frac{dV_{slope} - 110\ mV}{10\ \mu A} \quad \text{(eq. 32)}$$

(10 μA corresponds to the internal sawtooth current amplitude)

To make sure the damping of the peak at f_s / 2 in the frequency response is not an issue (gain at f_s / 2 < 0), the overall Bode plot needs to be drawn. The closed loop transfer function is given by Equation 33, product of Equations 16, 21 and 29.

$$T_{closedLoop} = T_{power\_ccm}(s) \cdot T_{comp} \cdot (s)T_h(s) \quad \text{(eq. 33)}$$

Stability Analysis in Discontinuous Conduction Mode (DCM)

We use the values of the components as they were designed for CCM operation in the equation of the transfer function of the converter running in DCM mode. We check by drawing a Bode diagram if the stability requirements are met for the closed loop system, including the compensation network and the high frequency effect of the current mode control.

Note that if one started the design procedure for a power converter in DCM mode, a similar approach can be used to check the stability in CCM mode.

Step 1: Calculate the Duty Cycle, D, Based on the Voltage Transformation Ratio

$$\frac{V_{out}}{V_{in}} = D\sqrt{\frac{R}{2L_{pri}f_s}} \Rightarrow D = \frac{V_{out}}{V_{in}}\sqrt{\frac{2L_{pri}f_s}{R}} \quad \text{(eq. 34)}$$

Step 2: Frequency Response Analysis

The transfer function of the power stage in DCM is given by Equation 35.

$$T_{power\_dem}(s) = K\frac{1 + \frac{s}{\omega_{zesr}}}{1 + \frac{s}{\omega_p}}$$

where

$$K = nD\sqrt{\frac{R_{load}}{2L_{sec}f_{sw}}} = \frac{V_{out}}{V_{in}} \quad \text{(eq. 35)}$$

$$\omega_{zesr} = \frac{1}{R_{esr} \cdot C_{out}} \Rightarrow f_{zesr} = \frac{1}{2\pi R_{esr} \cdot C_{out}} \quad \text{(eq. 36)}$$

$$\omega_p = \frac{2}{R_{load}C_{out}} \Rightarrow f_p = \frac{2}{2\pi R_{load}C_{out}} \quad \text{(eq. 37)}$$

Plot the total closed loop frequency response (Equation 38) and check the stability requirements.

$$T_{closedLoop} = T_{power\_dcm}(s) \cdot T_{comp} \cdot (s)T_h(s) \quad \text{(eq. 38)}$$

Switch Drain−Source Voltage Considerations

Special attention to the switch drain−source reverse voltage is required since in fly−back design, this voltage will be the sum of the input voltage and the weighted output voltage, as indicated in Equation 39.

$$V_{DS} = V_{in} + \frac{N_1}{N_2}V_{out} \quad \text{(eq. 39)}$$

Note the forward diode drop needs to be taken into account. Also note the leakage inductance will add a voltage spike. Sufficient margin needs to be built in when choosing the switch transistor.

Snubber Design

To avoid destruction of the switching transistor due to the voltage spikes originating from the leakage inductance, these transient spikes at the drain of the power switch need to be reduced. To size the snubber, measure the ringing frequency and calculate R_{sn} and C_{sn}.

$$R_{sn1} = 2\pi f_{ring} L_{leak} \quad \text{(eq. 40)}$$

$$C_{sn1} = \frac{1}{2\pi f_{ring} R_{sn1}} \quad \text{(eq. 41)}$$

The snubber design for the diode at the secondary side of the transformer is handled in the same way.

To measure the oscillation frequency in a safe way, use a low V_{in} and do not apply any load to the converter to make sure that the peak voltage is not exceeding the switching transistor V_{DS} rating.

Soft Start

To eliminate possible voltage overshoots on the output during start up, the NCP1081 provides a soft start function which increases progressively the duty cycle limit during the soft start time. This soft start is programmable by Css and defined by Equation 42.

$$T_{softstart}[ms] = 0.23 C_{ss}[nF] \quad \text{(eq. 42)}$$

VDDL and VDDH

C_{vvdl} and C_{vddh} are noise decoupling capacitors (20%) with low ESR (< 0.1 Ω). C_{vddl} may range from 330 to 470 nF. C_{vddh} may range from 1 to 2.2 μF. For application using the auxiliary bias winding to supply the VDDH regulator, the designer has to make sure that the bias winding does not force VDDH above 16 V for the maximum load condition. Use 50 Ω for R_{bw} as initial value.

Converter Efficiency

The overall efficiency of the flyback power converter is given by Equation 43.

$$\eta = \frac{P_{out}}{P_{out} + P_{MOSdynamic} + P_{MOSstatic} + P_{diode} + P_{esr} + P_{MagConductive} + P_{core} + P_{NCP108x}} \quad \text{(eq. 43)}$$

Each of the power losses in Equation 43 are calculated in following sections.

Dynamic Power Switch Losses

Dynamic switch losses are created during the toggling of the switch. Parasitic capacitances in the switch are charged and discharged.

$$P_{MOSdynamic} = V_{dsmax} \cdot I_{peak\_pri} \cdot f_s \cdot t_{sw} + \frac{C_{swout} \cdot V_{dsmax} \cdot f_s}{2} + f_s \cdot Q_{gtot} \cdot V_{gatedrive} \quad \text{(eq. 44)}$$

where

$$V_{dsmax} = 1.15 \cdot \left(V_{in} + \frac{\left(V_{out} + V_{diode}\right)}{2} \right) \quad \text{(eq. 45)}$$

the maximum drain−source voltage.

$$t_{sw} = \frac{Q_{gd} \cdot R_{gatedrive}}{V_{gatedrive} \cdot V_{GSth}}, \text{ the switch−on time} \quad \text{(eq. 46)}$$

V_{GSth} is the gate to source threshold voltage from the data sheet
Q_{gd} is the gate to drain Miller charge from the data sheet
Q_{gtot} is the total gate charge from the switch data sheet
$I_{peakpri}$ is the peak current at the primary
$V_{gatedrive}$ is the gate drive voltage of the NCP1081, or 9 V
V_{diode} is the forward voltage drop of the diode at secondary side
C_{swout} is the switching transistor output capacitance

Static Power Switch Losses

Static losses are the conductive losses of the power switch and calculated using the R_{dson} resistance coming from the data sheet and the RMS current.

$$P_{MOSstatic} = \left(R_{DS(on)} + R_{CS}\right) \cdot I_{rms\_pri}{}^2 \cdot D \quad \text{(eq. 47)}$$

With $R_{DS(on)}$ the on resistance of the switch, from the data sheet and R_{cs} is the calculated current sense resistance.

Secondary Diode Losses

The secondary diode has a forward voltage drop, affecting the overall efficiency.

$$P_{diode} = \frac{P_{out}}{V_{out}} \cdot V_{diode} \quad \text{(eq. 48)}$$

Capacitor Losses

One of the biggest loss contributors is the parasitic equivalent series resistor of the output smoothing and the input bulk capacitors.

$$P_{esr} = R_{esr\_cout} \cdot I^2_{rms\_sec} + R_{esr\_cpd} \cdot I^2_{rms\_pri} \quad \text{(eq. 49)}$$

It is important to use low ESR capacitors.

Conductive Losses in Magnetics

Conductive losses are those originating from the DC and AC resistance of the transformer wire. DC resistance of primary and secondary windings are listed by the transformer manufacturer. When the switching frequency

increases, additional phenomena such as skin effect and proximity effect increase the losses even further.

$$P_{MagConductive} = R_{dc\_pri} \cdot I^2_{rms\_pri} + R_{dc\_sec} \cdot I^2_{rms\_sec} \quad \text{(eq. 50)}$$

To make calculations simpler, we discard the AC resistance of the copper wire. But note that the AC losses become substantial with high switching frequencies.

Core losses originate from the energy that is dissipated in the core of the transformer and can be found from graphs for the specific core material used and the physical dimensions of the core.

NCP1081 Losses

First calculate the current consumed on the VPORTP pin in Power Mode:

$$I_{VportP}\,(mA) = I_{Quiescent}\,(mA) + I_{PortDriver}\,(mA) + I_{PWM}\,(mA) \quad \text{(eq. 51)}$$

With

$$I_{Quiescent}\,(mA) = 1.4 \quad \text{(eq. 52)}$$

Core Losses

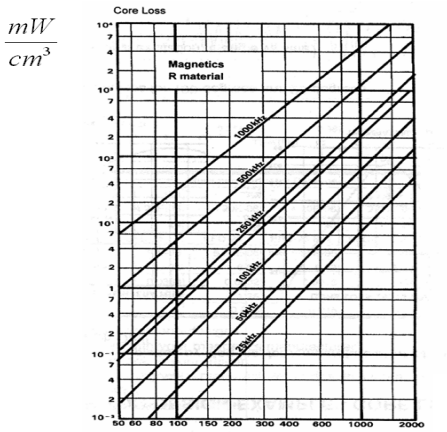

Figure 16. Core Losses

$$I_{PortDriver}(mA) = 0.1 + I_{PassSwitch}\,(mA) \times \left[\frac{1}{385} + \frac{1}{2300}\right] \quad \text{(eq. 53)}$$

$$I_{PWM}(mA) = 1.175 + \frac{f_s(kHz)}{250} \times \left[0.725 + 4.35 \times \frac{C_{gate}(nF)}{2}\right] \quad \text{(eq. 54)}$$

With C_{gate} the equivalent input capacitance of the external switching MOSFET

Then calculate the internal power dissipation.

$$P_{NCP108x}(mW) = P_{Quiescent}(mW) + P_{PortDriver}(mW) + P_{PWM}(mW) \quad \text{(eq. 55)}$$

With

$$P_{Quiescent}(mW) = I_{Quiescent}(mA) \times V_{portP}(V) \quad \text{(eq. 56)}$$

$$P_{PortDriver}(mW) = I_{PortDriver}(mA) \times V_{portP}(V) + I_{PortDriver}{}^2(mA) \times R_{on\_PassSwitch} \quad \text{(eq. 57)}$$

$$P_{PWM}(mW) = I_{PWM}(mA) \times V_{portP}(V) \quad \text{(eq. 58)}$$

if the auxiliary winding of transformer is not used, or

$$P_{PWM}(mW) = I_{PWM}(mA) \times V_{DDH}(V) \quad \text{(eq. 59)}$$

if VDDH is supplied by the auxiliary winding of transformer

The internal junction temperature can be evaluated.

$$T_J(degC) = T_{ambient}(degC) + P_{DissTotal}(mW) \times \frac{R_{th}(W/\deg C)}{1000} \quad \text{(eq. 60)}$$

With Rth the junction to ambient thermal resistance

Secondary Diode Maximum Rating

A rule of thumb for the maximum reverse voltage of the secondary rectifying diode is

$$V_{reverse} = \frac{V_{in\_max} * N_s}{N_p} \quad \text{(eq. 61)}$$

The maximum current through the diode is given by Equation 9.

Design Example 1: 30 W Single Output 12 V Supply

A Microsoft Excel® file (NCP108X DESIGN TOOL FLYBACK CCM.xls) with calculation sheets is provided by ON Semiconductor, with the presented expressions incorporated to design a stable and reliable flyback converter. In Figure 17 all the input data needed for the design is shown. As a result, the output calculated data is shown in Figure 18.

The frequency and phase response of the system as well as the poles and zeroes are calculated by the Excel VBA macros and shown in logarithmic charts for the power stage, compensation and close loop networks in Figure 20.

The Excel VBA script calculates also the efficiency for various output power, gives the final summary of all the designed components, according to a certain scematics(shown in Figure 1). In addition there is a convenient tool to calculate the output divider resistor values, when the output voltage and the reference voltage of the shunt feedback regulator are given.

Frequency response plots	
Minimum frequency(Hz)	1.00E+02
Maximum frequency(Hz)	1.00E+06
DC/DC system parameters	
Pout(W)	30
Vout(V)	12
Vin(V)	48
Vdrop_d(V)	0.5
Vripple(V)	0.1
Shunt regulator reference voltage(V)	2.5
Rbias1(Ohm)	5.10E+03
Rfb1(Ohm)	1.80E+04
Desired phase margin(Deg)	7.00E+01
T_softstart(s)	1.00E-02
T_rendement	8.00E-01
Optocoupler parameters	
Fopto(Hz)	8.00E+03
Optocoupler CTR	2.50E-02
Transformer parameters(from datasheet)	
Lpri(H)	1.27E-04
N	2.90E-01
DCR_pri(Ohm)	4.50E-01
DCR_sec(Ohm)	5.00E-02
MOSFET parameters(from datasheet)	
Rdson(Ohm)	4.60E-01
Cswout(F)	9.20E-11
Qswgtot(C)	1.20E-08
Qswmill(C)	1.20E-08
Vswgsth(V)	2.90E+00
NCP108x parameters	
Av	2.00E+00
Fs(Hz)	1.00E+05
Vgatedrive(V)	9.00E+00
Rgate(Ohm)	1.80E+01

Figure 17. Input Data for the Flyback Design Excel Calculation Sheet

Rdet1(Ohm)	2.37E+04
Rdet2(Ohm)	1.78E+03
Estimated efficiency(%)	85.17232143

Figure 18. Output Data Calculated by the Flyback Design Excel Calculation Sheet – Values of the Detection Signature Resistors and the Maximum Power Estimated Efficiency

Outputs:	
Fcross(Hz)	8.00E+03
T_power_stage gain at Fcross(dB)	5.01E+00
D	4.63E-01
Parameter extraction:	
Rfb2(Ohm)	4.75E+03
Rfb3(Ohm)	1.13E+02
Rbias2(Ohm)	1.00E+12
Rload(Ohm)	4.70E+00
Resr(Ohm)	1.07E-02
Rosc(Ohm)	3.83E+05
Rsl(Ohm)	8.06E+03
Rcs(Ohm)	1.17E-01
Cfb1(F)	1.00E-08
Cfb2(F)	8.20E-10
Cout(F)	2.20E-04
Css(F)	4.70E-08
Lsec(H)	1.07E-05

Figure 19. Output Data Calculated by the Flyback Design Excel Calculation Sheet – Parameter Extraction of the External Components Values According to Figure 1

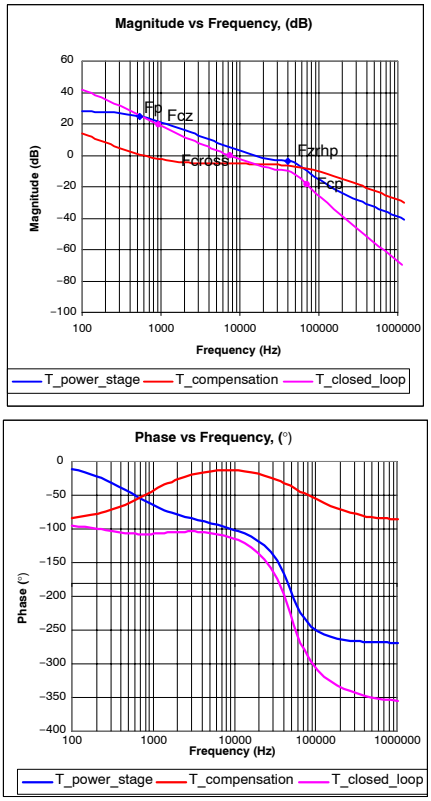

Figure 20. Output Data Calculated by the Flyback Design Excel Calculation Sheet – Frequency and Phase Response of the Designed Flyback Converter

Design Example 2: 20W Single Output 3.3V Supply

Scilab scripts are also provided to aid the design calculation. Scilab is an open−source numeric computation program that is available free of charge at www.scilab.org. The input data is shown in Table 6.

Table 6. DESIGN PARAMETERS

Parameter	Value
V_{in}	36 V (minimal PD input voltage)
V_{out}	3.3 V
L_{prim}	42 μH, according to Coilcraft POE300F−33L data sheet
N	0.09, according to Coilcraft POE300F−33L data sheet
P_{out}	20W
V_{ripple}	33 mV
f_s	250 kHz

The output of the Scilab script summarizes the design parameters and the closest standard values of the calculated component values for the feedback loop.

The Bode plot of the converter without compensator network and with compensator network is plotted in Figure 21.

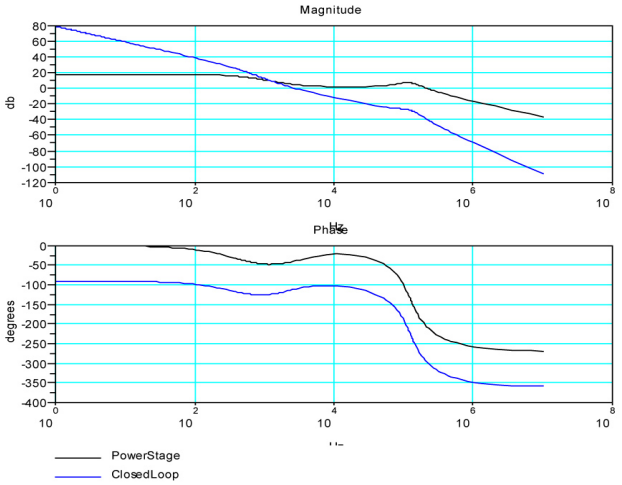

Figure 21. Gain and Phase Plot of the Compensated Converter

Note: *If Scilab or Excel software is not available, using asymptotic approximation to generate a Bode plot and computing the values manually will lead to similar results.*

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