Compensation of a PFC Stage Driven by the NCP1654

AND8321/D

Circuits for power factor correction have to shape the line current that is a low frequency signal. Hence, they are in essence extremely slow systems. That is why, the compensation of the PFC loop is generally not considered as a critical step when designing a power supply: “wildly shrink your bandwidth, that’s it!”. Still however, a PFC stage must be compensated and this unavoidable step should be properly performed for an optimized operation of the downstream converter and a satisfactory power factor.

This application note shows how a NCP1654−driven PFC can be compensated by the means of a systematic method. Reusable for other circuits, this process is practically illustrated through a wide mains, 300 W application.

Introduction

The NCP1654 is an upgraded version of the NCP1653.

With “its father”, it shares the control scheme that led to a major leap towards implementation of PFC boost converters operating in continuous conduction mode. Practically, like the NCP1653, it directly controls the power switch conduction time (PWM) as a function of the coil current. Housed in a SO8 package and available in 3 frequency versions (65, 133 and 200 kHz) the NCP1654 integrates all the features for a compact and rugged PFC stage. Ultimately, as well as the NCP1653, it leads to an eased and compact PFC implementation.

It is worth noting that it has also inherited the NCP1653 current sensing technique and its associated merits. More specifically, this function can be associated to very low impedance current sense resistors for reduced losses and a significant improvement of the efficiency. Compared to traditional solutions, the efficiency increase can be as high as almost 1%.

Finally, with respect to the NCP1653, the NCP1654 further incorporates a brown−out detection block to disable the PFC stage when the line magnitude is too low. Also, the voltage regulation is made more accurate and a dynamic response enhancer dramatically minimizes the large deviation of the output voltage that a sharp line/load step would otherwise produce.

The NCP1654 pinout is intended to ease the replacement of industry existing circuits.

PFC Stage Control to Output Transfer Function

First, we have to compute the control to output transfer function ($V_{out}/V_{control}$), where V_{out} is the output voltage of the PFC stage and $V_{control}$, the output of the error amplifier (that is, our control signal)

To do so, we need to:

1. Derive a large signal model of our system. Such a representation takes into account the dc and ac components of the signals. The result is a non linear representation in particular due to the multiplication of time varying signals.
2. Linearize this system and for this, to consider little variations of each signal around the dc values (obtained in steady state) to derive the small signal model. Practically it models the system response to a perturbation applied to the two input signals ($V_{in,RMS}$ and $V_{control}$) or to the output (V_{out}). This is exactly what our compensation will have to control.

In PFC applications, a good way to build the large−signal model, is probably to inspire of the “loss−free network” method developed by Dr Robert Erickson [1] and:

1. Derive an equation of the power delivered by the PFC stage as a function as the parameters that modulate it, practically, the line magnitude and $V_{control}$. To do so, this power will be averaged over a line period. (Note 1)
2. Represent our system as a current source that under V_{out} provides the computed power.

1. This approximation (constant power while it has actually a squared sinusoidal characteristics) is acceptable since the PFC regulation bandwidth is below the line frequency.

The average power delivered by the NCP1654 is given by the following formula (refer to the data sheet):

$$P_{in,avg} = \frac{K \cdot (V_{control} - V_{control(min)}) \cdot V_{in,RMS}}{V_{out}} \text{ with: } K = \frac{2\pi R_{CS} \cdot (R_{boU} + R_{boL}) \cdot V_{REF}}{\sqrt{2} \cdot R_M \cdot R_{boL} \cdot R_{SENSE}} \quad \text{(eq. 1)}$$

Where:

- $V_{in,RMS}$ is the RMS line voltage
- $V_{control}$ is the output voltage of the NCP1654 error amplifier
- $V_{control(min)}$ is the minimum output voltage of the error amplifier.
- V_{out} is the PFC output voltage
- V_{REF} is the internal 2.5 V reference voltage
- R_{SENSE} is the current sense resistor
- R_{CS} is the resistor that sets the current limitation
- R_M is the V_m pin resistor
- R_{boU}, R_{boL} are the upper and lower brown−out sensing resistors respectively. Please note that R_{boU} is practically spit into two or several resistors for safety reasons (due to its connection to the input high voltage rail) (See Figure 7).

Our system can then be represented by a current source ($I_{out} = P_{in,avg}/V_{out}$) that charges the bulk capacitor C which is loaded by a resistor R that simulates the load. This leads to the following large−signal model:

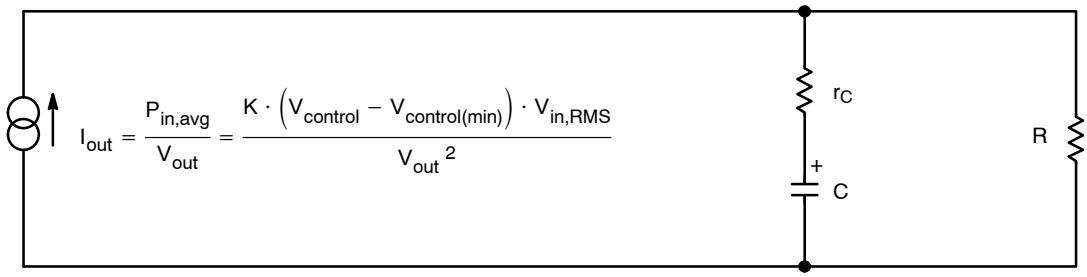

Figure 1. Large signal model of the PFC stage
(R is the Load Equivalent Resistance and C and r_C are Respectively the Capacitance and the Series Resistor of the PFC Output Capacitor)

Considering small variations for $V_{control}$, $V_{in,RMS}$ and V_{out}, one can derive the following small−signal equivalent schematic:

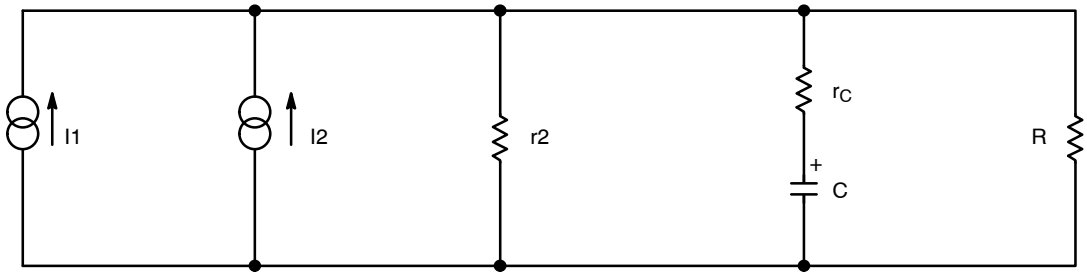

Figure 2. Small Signal Model of the PFC Stage
(R is the Load Equivalent Resistance and C is the PFC Output Capacitor − Bulk Capacitor)

In Figure 2:

- I1 is a current source that models the I_{out} variation produced by a small $V_{control}$ variation $\hat{v}_{control}$.

$$I1 = \frac{\partial I_{out}}{\partial V_{control}} \cdot \hat{v}_{control} = \frac{K \cdot V_{in,RMS}}{V_{out}^{\,2}} \cdot \hat{v}_{control} \quad \text{(eq. 2)}$$

- I2 models the I_{out} variation that results from a small variation of $V_{in,RMS}$.

$$I2 = \frac{\partial I_{out}}{\partial V_{in,RMS}} \cdot \hat{v}_{in,RMS} = \frac{K \cdot \left(V_{control} - V_{control(min)}\right)}{V_{out}^{\,2}} \cdot \hat{v}_{in,RMS} \quad \text{(eq. 3)}$$

- r2 models the I_{out} variation that results from a small variation of V_{out} (Note 2).

$$r2 = \frac{V_{out}^{\,2}}{2 \cdot P_{in,avg}} = \frac{R}{2} \quad \text{(eq. 4)}$$

Here, we do not consider the input voltage variations. Hence, ($\hat{V}_{in,RMS} = 0$) and the current source I2 cancels. If in addition, we note that R/3 is the resistance equivalent to that of R wired in parallel with R/2, Figure 2 simplifies as follows:

Figure 3. Small Signal Model Where the Line Variations are Not Taken Into Account

The bulk capacitor (including the series resistor "r_C") in parallel to the load ("R") leads to the following impedance:

$$Z = (C + r_c) \parallel \frac{R}{3} = \frac{R}{3} \cdot \frac{1 + (s \cdot r_c \cdot C)}{1 + \left(s \cdot \left(r_c + \frac{R}{3}\right) \cdot C\right)} \quad \text{(eq. 5)}$$

As the capacitor series resistor ("r_C") is small compared to R, the precedent formula simplifies as follows:

$$Z \cong \frac{R}{3} \cdot \frac{1 + (s \cdot r_C \cdot C)}{1 + \frac{s \cdot R \cdot C}{3}} \quad \text{(eq. 6)}$$

Hence, the transfer function is:

$$\frac{V_{out}}{V_{control}} = Z \cdot I1 = \frac{K \cdot R \cdot V_{in,RMS}}{3 \cdot V_{out}^{\,2}} \cdot \frac{1 + (s \cdot r_C \cdot C)}{1 + \frac{s \cdot R \cdot C}{3}} \quad \text{(eq. 7)}$$

Thus, we have:

- The following pole:

$$f_{RC} = \frac{3}{2\pi \cdot R \cdot C}$$

- A zero due to the series resistor of the bulk capacitor:

$$f_{ESR} = \frac{1}{2\pi \cdot r_C \cdot C}$$

- A static gain that is dependent on the line and load levels:

$$(G_0)_{dB} = 20 \cdot \log\left(\frac{K \cdot R \cdot V_{in,RMS}}{3 \cdot V_{out}^{\,2}}\right)$$

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2. When we compute:

$$I3 = \frac{\partial I_{out}}{\partial V_{out}} \cdot \hat{v}_{out} = \frac{-2K \cdot (V_{control} - V_{control(min)})}{V_{out}^{\,3}} \cdot \hat{v}_{out} = -\frac{2 \cdot I_{out}}{V_{out}} \cdot \hat{v}_{out} = -\frac{2 \cdot \hat{v}_{out}}{R}$$

we note that I3 is the current absorbed by a resistor (R/2) placed across ($\hat{V}_{out}$). That is why a resistor r2 = (R/2) simulates the impact of V_{out} variations on the bulk capacitor charge current.

Output to Control Transfer Function

The NCP1654 embeds a transconductance error amplifier (OTA).
Hence, the OTA output current ($I_{control}$) is:

$$I_{control} = G_{EA} \cdot \left[\frac{R_{fbL} \cdot V_{out}}{R_{fbL} + R_{fbU}} - V_{REF} \right] = G_{EA} \cdot \frac{R_{fbL} \cdot \left[V_{out} - V_{out,nom} \right]}{R_{fbL} + R_{fbU}} \quad \text{(eq. 8)}$$

Where:

- R_{fbU} is the feed−back upper resistor. Please note that R_{fbU} is practically spit into two or several resistors for safety reasons (due to its connection to a high voltage rail) (See Figure 7).
- R_{fbL} is the feed−back lower resistor.
- $V_{out,nom}$ is the regulation level of the output voltage.
- G_{EA} is the trans−conductance gain of the error amplifier (200 μS typically)

The precedent section shows that the power stage exhibits one pole and one zero that we have to compensate. A type 2 compensator that brings two poles and one zero (as portrayed by Figure 4) is the recommended solution.

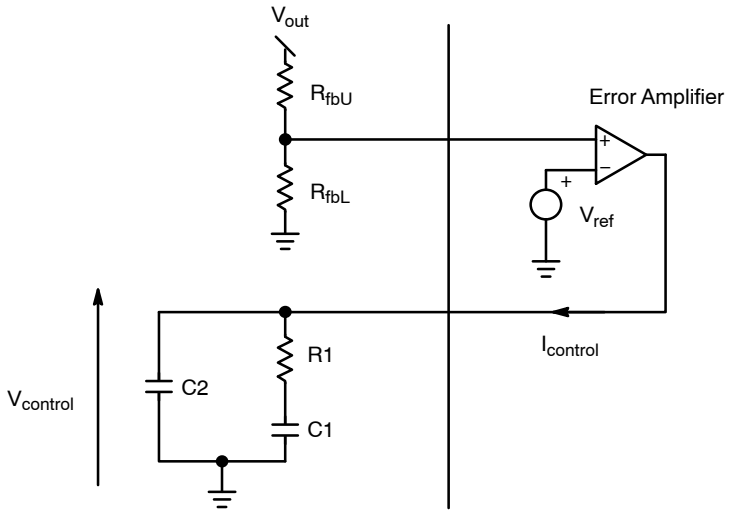


Figure 4. Type 2 Compensation

One can calculate the control function of our type 2 compensator:

$$\frac{V_{control}}{I_{control}} = \frac{1 + s \cdot R1 \cdot C1}{s(C1 + C2) \cdot \left(1 + s \cdot \frac{R1 \cdot C1 \cdot C2}{C1 + C2}\right)} \quad \text{(eq. 9)}$$

Hence, substitution of the $I_{control}$ expression into the precedent equation leads to:

$$\frac{V_{control}}{V_{out}} = \frac{R_{fbL}}{R_{fbL} + R_{fbU}} \cdot \frac{1 + s \cdot R1 \cdot C1}{s\frac{(C1 + C2)}{G_{EA}} \cdot \left(1 + s \cdot \frac{R1 \cdot C1 \cdot C2}{C1 + C2}\right)} \quad \text{(eq. 10)}$$

R_{fbL} and R_{fbU} are the feedback resistors that scale down the output voltage for regulation. Hence, in steady state:

$$V_{REF} = \frac{R_{fbL}}{R_{fbL} + R_{fbU}} \cdot V_{out,nom} \quad \text{(eq. 11)}$$

Where:

- V_{REF} is the NCP1654 internal reference voltage (2.5 V).
- $V_{out,nom}$ is the output regulation level.

Finally, if C2 << C1, Equation 10 simplifies as follows:

$$\frac{V_{control}}{V_{out}} = \frac{1 + \left(s \cdot 2\pi \cdot f_{z1}\right)}{s \cdot 2\pi \cdot f_{p0} \cdot \left(1 + s \cdot 2\pi \cdot f_{p1}\right)}$$

Where:

$$f_{z1} = \frac{1}{2\pi \cdot R_1 \cdot C_1}$$

$$f_{p1} = \frac{1}{2\pi \cdot R_1 \cdot C_2}$$

$$f_{p0} = \frac{1}{2\pi \cdot R_0 \cdot C_2}$$

$$R_0 = \frac{V_{out,nom}}{V_{REF} \cdot G_{EA}}$$

Closing the Loop

We need then to position the poles and zeroes of the compensator so that the open loop gain crosses zero dB at the crossover frequency f_c with a (−1) slope and the wished phase margin.

We have the choice between several techniques to define our compensation network like the “k factor” method from Dean Venable or the manual placement presented in Christophe Basso book [5]. Here, we propose to simply compensate our PFC stage by systematically forcing a (−1) slope for the open loop gain up to the crossover frequency. It can be done as follows:

1. Select the crossover frequency f_c, that is, the frequency at which the open loop gain drops to 0 dB. It is generally admitted that it should be in the range of half the line frequency at high line (we will see that the crossover frequency peaks at high line). Actually f_c must be as low as possible to obtain a near unity power factor. This is because any ripple on the error amplifier output generates some distortion of the line current. On the other hand, a low crossover frequency leads to a slow response to load or line variations. So, if your power factor specification is not very stringent, it is wise to increase f_c with the benefit of better dynamic performance. Generally speaking, f_c equal to half the line frequency at high line is a good starting point.
2. Position the zero of your compensation at the frequency of the pole: ($f_{z1} = f_{RC}$) so that they cancel each other.
3. Place f_{p1} so that it cancels the zero produced by the ESR of the bulk capacitor: ($f_{p1} = f_{ESR}$). If (f_{ESR}) is a very high frequency zero, you should clamp (f_{p1}) to half the switching frequency for a good filtering of the switching noise. This pole filters the high frequency noise:

   $$\left(f_{p1} = \frac{f_{SW}}{2} \right)$$

4. The poles and zeroes of the power stage are cancelled by the zero and pole of the compensator. Hence, the open loop gain only depends on the pole at the origin f_{p0} that forces a (−1) slope and on the static gain. In other words, the gain equates:

   $$\left((G(f))_{dB} = (G_0)_{dB} - 20 \cdot \log\left(\frac{f}{f_{p0}} \right) \right)$$

   To obtain the wish crossover frequency, we then need to choose (f_{p0}) so that:

   $$\left(0 = (G_0)_{dB} - 20 \cdot \log\left(\frac{f_c}{f_{p0}} \right) \right)$$

   Ultimately, this leads to the following equation giving f_{p0} as a function of f_c and G_0:

   $$\left(f_{p0} = f_c \cdot 10^{-\frac{(G_0)_{dB}}{20}} \right)$$

Please note that using this method, the phase margin asymptotically tends towards 90°, which must ensure a very stable operation. Now, if you want to improve the response to a load step and further filter the control signal for a minimized THD (Note 3), you can decrease the phase margin to, for instance, 75°. To do so, you can play with the high frequency pole following the procedure shown in [4]. Practically, this pole is placed at a lower frequency so that the phase shift it produces can alter the phase margin measured at:

$$f_{p1} = f_c \cdot \tan(\Phi_m)$$

Where Φ is the desired phase margin.

At which load and line voltage should we compensate our PFC stage?

As shown in section 1, there are two parameters that depend on the load and line conditions:

- The static gain (G_0) is proportional to line magnitude ($V_{in,RMS}$) and to the load equivalent resistance (R)
- The pole f_{RC} of the power stage is inversely dependent on R since:

$$\left(f_{RC} = \frac{3}{2\pi \cdot R \cdot C}\right)$$

In the compensation method that is proposed, we assume that:

- The pole f_{RC} is canceled by the compensator zero
- The pole at the origin by the compensator is set as a function of the static gain.

Let's assume that we design our compensator for full load conditions: $R = R_{min}$. The compensator zero (f_{z1}) is then computed for $R = R_{min}$. At this load, f_{z1} perfectly cancels the power stage pole (f_{RC}). At any other load, its frequency is too high to cancel f_{RC}. As a consequence, the loop gain will be attenuated as follows:

$$\Delta G_{dB} = 20 \cdot \log\left(\frac{f_{RC}}{f_{z1}}\right) = 20 \cdot \log\left(\frac{R}{R_{min}}\right) \quad \text{(eq. 12)}$$

On the other hand, we know that the static gain is increased as follows:

$$\left(\Delta G_0\right)_{dB} = 20 \cdot \log\left(\frac{K \cdot R \cdot V_{in,RMS}}{3 \cdot V_{out}{}^2}\right) - 20 \cdot \log\left(\frac{K \cdot R_{min} \cdot V_{in,RMS}}{3 \cdot V_{out}{}^2}\right) = 20 \cdot \log\left(\frac{R}{R_{min}}\right) \quad \text{(eq. 13)}$$

Finally the two gain variations cancel! Simply, we switch from Figure 5 to Figure 6.

A change in the load does not shift the crossover frequency. So, for instance, we can choose to make the computation at full load.

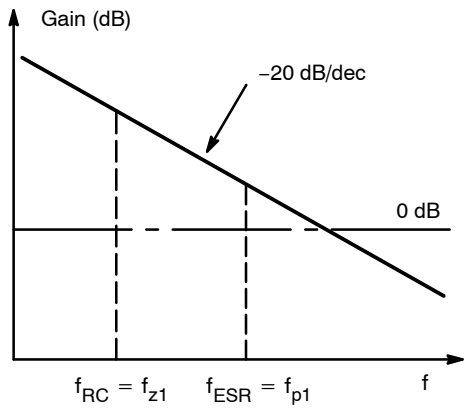


Figure 5.

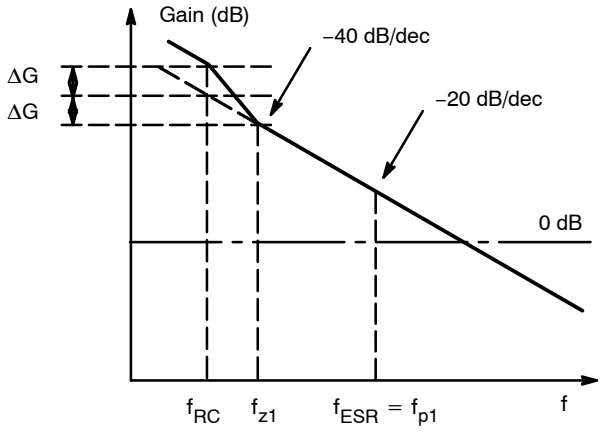


Figure 6.

As for the input voltage, it also changes the static gain but there is no change in the poles and zeroes position. So, the open−loop gain is (ΔG_0) shifted and the crossover frequency f_c is higher at high line than low line:

$$(f_c)_{HL} = \frac{(V_{in,RMS})_{HL}}{(V_{in,RMS})_{LL}} (f_c)_{LL} \quad \text{(eq. 14)}$$

Where:

- $(f_c)_{HL}$ is the high line crossover frequency.
- $(f_c)_{LL}$ is the low line crossover frequency.
- $(V_{in,RMS})_{LL}$ is the lowest line RMS voltage.
- $(V_{in,RMS})_{HL}$ is the highest line RMS voltage.

As the ratio is generally 3 between low and high line levels in a wide mains application, with the NCP1654, we can expect a ratio of 3 between the corresponding crossover frequencies:

$$(f_c)_{HL} = 3 \cdot (f_c)_{LL} \quad \text{(eq. 15)}$$

Finally, it seems reasonable to choose the crossover frequency to be targeted at high line and based on this selection, compute the compensation network for high line, full load.

Example

Let's illustrate the process in the following application:

- Universal Mains: $V_{in,RMS}$ varying from 90 to 265 V.
- Line Frequency: 50 Hz or 60 Hz
- Output Voltage Wished Level ($V_{out,nom}$): 390 V_{dc}
- Output Power: 300 W
- Output Capacitor: 180 μF / 450 V, ESR resistance: 500 mΩ
- Switching frequency: 65 kHz

The way of designing such a PFC stage is discussed in AND8322/D [3]. From it, we can deduce the following:

$$K = \frac{2\pi \cdot R_{CS} \cdot (R_{boU} + R_{boL}) \cdot V_{REF}}{\sqrt{2} \cdot R_M \cdot R_{boL} \cdot R_{SENSE}} = \frac{2\pi \cdot 3.6k \cdot 6682.2k \cdot 2.5}{\sqrt{2} \cdot 47k \cdot 82.5k \cdot 0.1} \cong 689\ A \quad \text{(eq. 16)}$$

At high line and full load (R = 500 Ω),

$$(G_0)_{dB} = 20 \cdot \log\left(\frac{K \cdot R \cdot (V_{in,RMS})_{HL}}{3 \cdot V_{out}^{\ 2}}\right) = 20 \cdot \log\left(\frac{689 \cdot 500 \cdot 265}{3 \cdot 390^{\ 2}}\right) = 46dB \quad \text{(eq. 17)}$$

Then, we can start the above presented process to close the loop:

1. Crossover Frequency at High Line: Let's choose it in the range of half the line frequency. As the specification indicates two line options (50 Hz or 60 Hz), let's use the lowest one: ($f_c = f_{line}/2 = 25$ Hz). We will then compute the compensation network with ($f_c = 25$ Hz) at high line.
2. Position the zero of your compensation at the frequency of the pole of the power stage: $f_{z1} = f_{RC}$ so that they cancel each other, at full load ($R = R_{min}$).
   Practically,
   $$f_{z1} = \frac{1}{2\pi \cdot R1 \cdot C1} = f_{RC} = \frac{3}{2\pi \cdot R_{min} \cdot C} \quad \text{(eq. 18)}$$
   Hence:
   $$R1 \cdot C1 = \frac{R_{min} \cdot C}{3} \rightarrow R1 = \frac{R_{min} \cdot C}{3 \cdot C1} \quad \text{(eq. 19)}$$
3. The frequency of the zero resulting from the bulk capacitor ESR is: $f_{ESR} = 1/(2\pi \cdot r_c \cdot C) = 1/(2\pi \cdot 500m \cdot 180\mu) \cong 1.8$ kHz, This frequency is far below the switching frequency so we simply have to place f_{p1} so that it cancels f_{ESR} without any clamp below ($f_{SW}/2$) consideration: $f_{p1} = 1/(2\pi \cdot R1 \cdot C2) = 1/(2\pi \cdot r_c \cdot C)$, where r_c is the ESR of the bulk capacitor.
   Then: $R1 \cdot C2 = r_c \cdot C \rightarrow C2 = ((r_c \cdot C)/(R1))$
4. The poles and zeroes of the power stage are cancelled by the zero and pole of the compensator. Hence, the open loop gain only depends on the pole at the origin f_{p0} that forces a (−1) slope and on the static gain. In other words, as previously explained, to obtain the wished crossover frequency, we need to choose (f_{p0}) so that G_0:
   $$\left(f_{p0} = f_c \cdot 10^{-\frac{(G_0)dB}{20}}\right)$$

Hence:

$$C1 = \frac{1}{2\pi \cdot f_c \cdot R_0} \cdot 10^{\frac{(G_0)dB}{20}} \quad \text{(eq. 20)}$$

Where as previously indicated:

$$R_0 = \frac{V_{out,nom}}{V_{REF} \cdot G_{EA}} = \frac{390}{2.5 \cdot 200\mu} \cong 780\ k\Omega \quad \text{(eq. 21)}$$

Finally in our application:

$$C1 = \frac{1}{2\pi \cdot f_c \cdot R_0} \cdot 10^{\frac{(G_0)dB}{20}} = \frac{1}{2\pi \cdot 25 \cdot 780k} \cdot 10^{\frac{46}{20}} = 1.6\ \mu F \quad \text{(eq. 22)}$$

Let's choose C1 = 1.5 μF. Equation 19 leads to:

$$R1 = \frac{R_{min} \cdot C}{3 \cdot C1} = \frac{500 \cdot 180\mu}{3 \cdot 1.5\mu} = 20\ k\Omega \quad \text{(eq. 23)}$$

Let's choose R1 = 20 kΩ:

$$C2 = \frac{r_c \cdot C}{R1} = \frac{500m \cdot 180\mu}{20k} = 4.5\ nF \quad \text{(eq. 24)}$$

Let's choose C2 = 4.7 nF:

With the computed C2, the phase margin is in the range of 90°. If you target a lower one for a faster recovery of the output voltage after a load step and a higher attenuation of the $V_{control}$ ripple for a reduced THD (Note 3), you can position the high frequency pole at a lower frequency level. Practically, the high frequency pole must meet the following equation:

$$f_{p1} = f_c \cdot \tan(\Phi_m) \quad \text{(eq. 25)}$$

And then:

$$C2 = \frac{1}{2\pi \cdot f_c \cdot R1 \cdot \tan(\Phi_m)} \quad \text{(eq. 26)}$$

For instance, if you target a 45° phase margin:

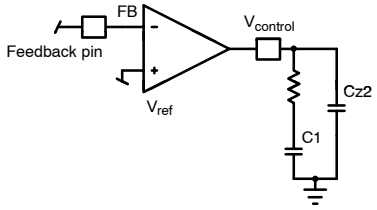
$$C2 = \frac{1}{2\pi \cdot f_c \cdot R1 \cdot \tan(45)} \cong 0.32\ \mu F \quad \text{(eq. 27)}$$

A 330 nF capacitor would then be a good choice.

3. The ac component of the control signal leads to a degradation of the Total Harmonic Distortion (THD).

Summary

The following table summarizes the main equations useful to compensate a NCP1654−driven PFC stage. Refer to Figure 7 for the meaning of the computed components.

Components	Formulae	Comments
NCP1654 CHARACTERISTICS		
Power delivered by the PFC stage	$P_{in,avg} = \frac{K \cdot (V_{control} - V_{control(min)}) \cdot V_{in,RMS}}{V_{out}}$	V_{REF} is the internal 2.5 V PWM reference, R_{CS} is the resistor that dictates the maximum coil current together with R_{SENSE} (current sense resistor), R_{boU} and R_{boL} are the upper and lower brownout resistors respectively, R_M is the resistor that sets the maximum power of the PFC stage. AND8322/D shows how to compute these elements.
Where:	$K = \frac{2\pi \cdot R_{CS} \cdot (R_{boU} + R_{boL}) \cdot V_{ref}}{\sqrt{2} \cdot R_M \cdot R_{boL} \cdot R_{SENSE}}$	
Error Amplifier Transconductance	$G_{EA} = 200\ \mu s$	
Internal Voltage reference for Regulation	$V_{REF} = 2.5\ V$	
POWER STAGE GAIN		
Static Gain at Full Load, High Line (dB)	$(G_0)_{dB} = 20 \cdot \log\left(\frac{K \cdot R_{min} \cdot \left(V_{in,RMS}\right)_{HL}}{3 \cdot {V_{out}}^2}\right)$	The static gain is line and load dependent. In PFCs that unlike the NCP1653/4, do not feature any feed−forward, G_0 even varies as a function of the square of the line RMS level. The static gain is calculated at full and high line as as necessary to design our compensation network.
Pole	$f_{RC} = \frac{3}{2\pi \cdot R \cdot C}$	Pole resulting from the bulk capacitor and the PFC load equivalent resistor.
Zero	$f_{ESR} = \frac{1}{2\pi \cdot r_c \cdot C}$	Zero produced by the series resistor (ESR) of the bulk capacitor.
COMPENSATION NETWORK		
Crossover Frequency at High Line	$(f_c)_{HL} = \frac{f_{line}}{2}$	The crossover frequency moves as a function of the line amplitude (see below).
Variation of f_c with respect to the line amplitude	$(f_c)_{HL} = \frac{(V_{in,RMS})_{HL}}{(V_{in,RMS})_{LL}}(f_c)_{LL}$	Subscript “HL” stands for “highest line”. Subscript “LL” stands for “lowest line”. In wide mains application, we have a ratio in the range of 3 between $(f_c)_{HL}$ and $(f_c)_{LL}$.
R0	$R_0 = \frac{V_{out,nom}}{V_{REF} \cdot G_{EA}}$	Equivalent resistor that sets the pole at the origin (f_{p0}) together with C1. $V_{out,nom}$ is the regulation level of the output voltage (390 V typically).
C1	$C1 = \frac{1}{2\pi \cdot f_c \cdot R_0} \cdot 10^{\frac{(G_0)dB}{20}}$	
R1	$R1 = \frac{R_{min} \cdot C}{3 \cdot C1}$	
C2	$C2_1 = \frac{r_c \cdot C}{R1}$ or $C2_2 = \frac{1}{2\pi \cdot f_c \cdot R1 \cdot \tan(\Phi_m)}$	$C2_1$ leads to 90° phase margin, $C2_2$ to a lower one (Φ_m) if wished for a better THD. $C2_2$ must be higher than $C2_1$.

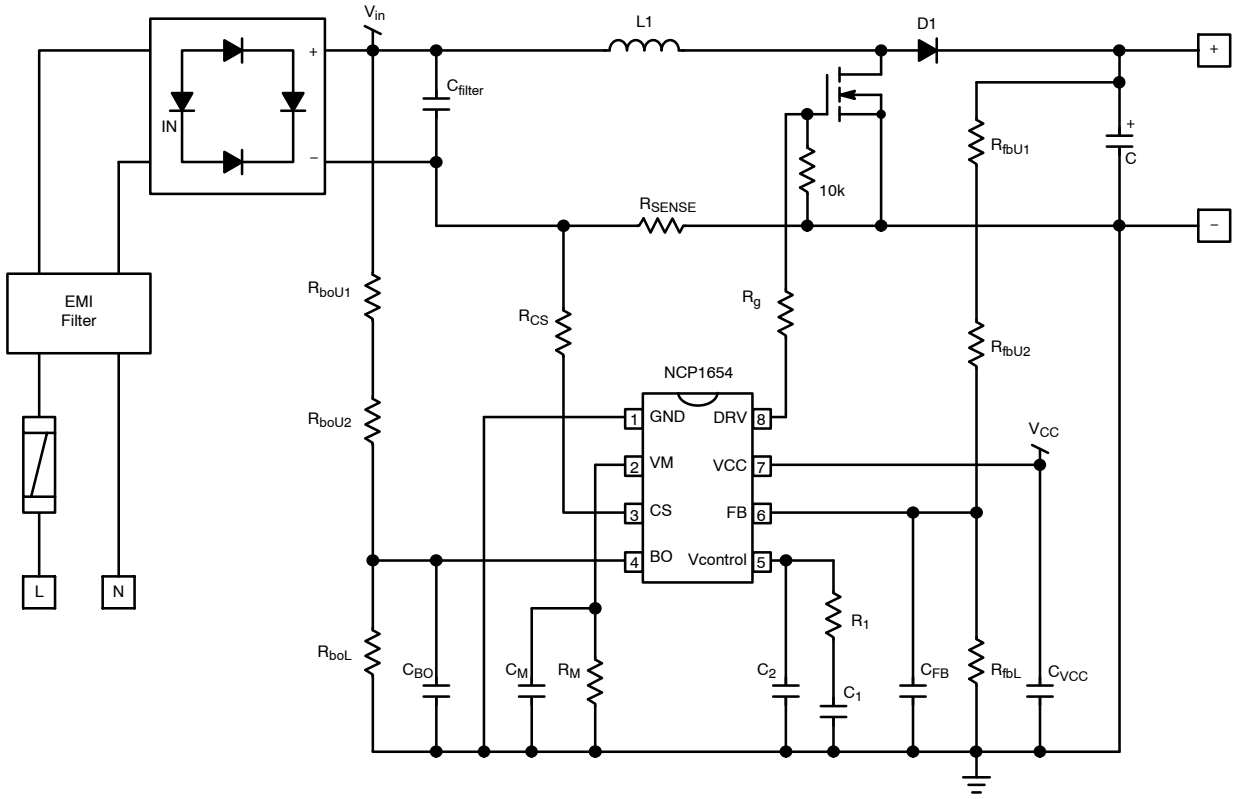


Figure 7. Generic Application Schematic
In this schematic, for the sake of a realistic representation, the brown−out and feedback upper resistors are split into two parts: ($R_{boU} = R_{boU1} + R_{boU2}$) and ($R_{fbU} = R_{fbU1} + R_{fbU2}$).

Conclusions

The paper presents a systematic approach to compensate your NCP1654 PFC stage. Such a process is useful to optimize your PFC stage particularly when you seek for the best trade−off between power factor quality and dynamic performance. Ultimately, it must ease and improve design of the whole power supply.

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