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AND8307/D

Characterization of ESD Clamping Performance

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APPLICATION NOTE

Introduction

The most commonly used standard for defining a typical electro−static discharge (ESD) event at the system level is IEC61000−4−2, which is distinguished by a waveform with a sub nanosecond rise time and high current levels (see Figure 1). The spec for this waveform calls out 4 levels of ESD magnitudes. Most designers are required to qualify their products to the highest level which is 8 kV contact discharge or 15 kV air discharge.

This test is a survival test designed for a system such as a cell phone or laptop computer. The test procedures for the spec require 10 pulses positive and 10 pulses negative at end user accessible points on the system and then determine if there has been an interruption (soft failure) or damage to the system (hard failure).

Table 1. IEC 61000−4−2 SPEC.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

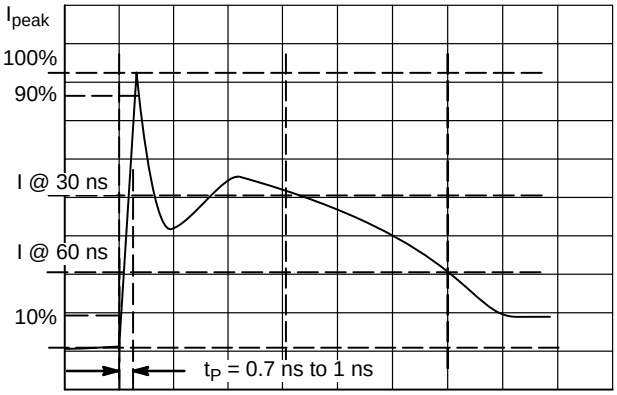

Figure 1. IEC61000−4−2 Spec

Testing ESD Voltage Clamping

ESD protection devices are an effective solution to protect sensitive circuit elements against these types of ESD surges. Most companies that make protection products, including ON Semiconductor, test their protection devices for survivability to the IEC 61000−4−2 current waveform. The ability of a protection device to survive an ESD stress does not guarantee that it will provide adequate protection to sensitive circuit elements, however. To do this the protection component must not only survive the ESD stress, but also maintain very low voltage across it during the ESD event to ensure that the circuit element it is protecting survives. Additional characterization is required to determine a protection device's voltage clamping capability. Examining the voltage waveform across the device during the time domain of an ESD event will give a designer valuable information as to what voltage the IC that is being protected will be exposed to. The following testing procedure outlines the steps ON Semiconductor utilizes to measure the voltage waveform over time of a protection device during an ESD event by obtaining an oscilloscope screenshot of the event.

Test Procedure to Obtain ESD Voltage Clamping Screenshot

1. Mount part on high frequency test board with SMA connector on back side − one terminal of protection part is connected to SMA center pin; other terminal connected to ground.
2. 50 Ω cable connects SMA connection on test board to oscilloscope.
   a. Set oscilloscope to 50 Ω input impedance to prevent reflections.
3. Attenuator used between cable and oscilloscope to protect the oscilloscope.
   a. Set oscilloscope external attenuator setting to match attenuator used to ensure correct voltage measurements.
4. Connect ground of ESD gun to ground of ESD test board by clipping it to SMA connection on back side of board. Connect tip of ESD gun to SMA center pin on ESD test board.
5. Discharge ESD gun in contact discharge mode at desired voltage.

The ESD diode is isolated between pins that are directly connected to the source of the ESD pulse and ground. The turn on resistance of the protection diode is much lower than the 50 Ω impedance of the cable so the majority of the current during the ESD event is directed through the protection device. The oscilloscope will then give an

accurate reading of the clamping waveform across the device over time during the event.

Figures 2 and 3 below illustrate the test setup described in the steps above.

An example of an ESD screenshot is shown in Figure 4. The desired output for an effective ESD protection device is to have a low overall voltage waveform during the entire duration of the ESD event. This screenshot technique becomes particularly useful when comparing two ESD protection devices for performance. In the past, this information was not readily available on datasheets but since IC's are becoming more sensitive to ESD ON Semiconductor recognizes the need for devices that clamp ESD to low voltages and now includes screenshots of the voltage clamping waveform on the datasheets for all ESD protection devices.

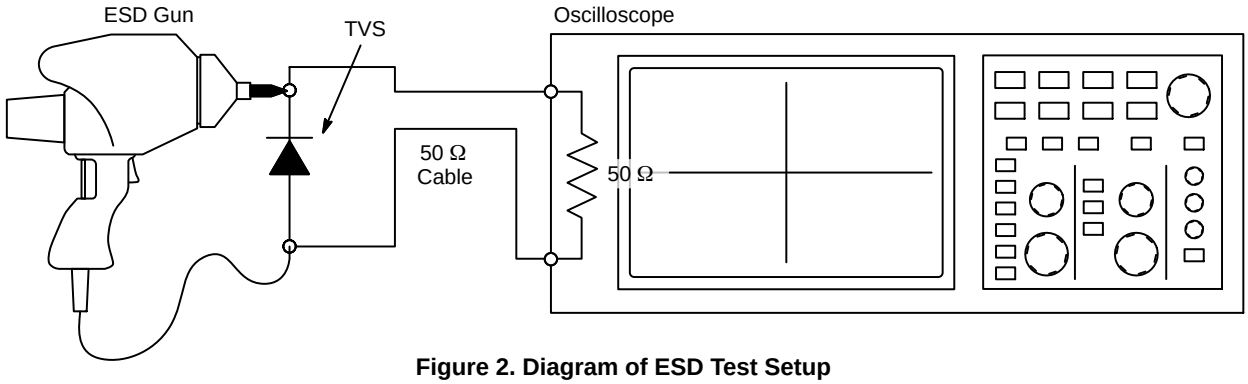

Figure 2. Diagram of ESD Test Setup

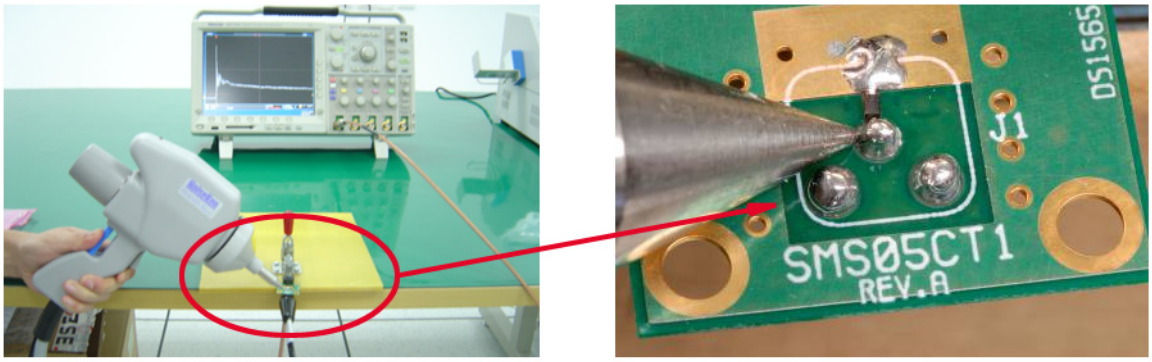

Figure 3. Picture of ESD Test Setup

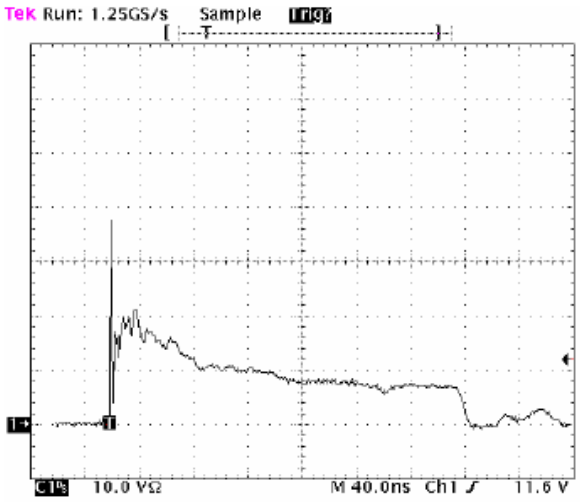

Figure 4. ESD Screenshot Example
(ON Semiconductor ESD9X5.0ST5G)

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