Improving Output Voltage Ripple of the NCP3063 Series of Switching Regulators by Applying a Simple Feedforward Technique

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The NCP3063 Switching Regulator is an improved version of the popular MC34063 switching regulators and is based on a very flexible hysteretic architecture that can be used to create step-down (buck), step-up (boost) and buck-boost voltage regulators. This device can support input and output voltages up to 40 V\(_{DC}\) which makes it attractive for a wide array of switching regulator applications, be it boosting a 5 V rail up to 24 V or stepping down a 12 V supply to 5 V or dealing with a wide input voltage from a Lead–Acid battery. The techniques discussed in this application note will assist the designer in optimizing their design to the specific \(V_{IN}\) and \(V_{OUT}\) requirements of their application and allowing them to improve output ripple performance when they do not require operating the DC–DC converter near the maximum duty cycle of the NCP3063.

The block diagram of the NCP3063 controller is shown in Figure 1.
The oscillator section consists of two current sources; one charging, the other discharging the timing capacitor $C_T$, between two fixed voltage levels. The levels are approximately 500 mV apart. The ratio between the charge current and the discharge current is set within the controller to be 1:6. This ratio creates a fixed duty cycle $D_{\text{MAX}}$ of 6/7 or 0.86. Typical operating waveforms, including the timing ramp $C_T$, are illustrated in Figure 2.

![Figure 2. Typical Operating Waveform](image)

This versatile controller can be configured for buck, boost, buck-boost and also inverting applications. For detailed information regarding controller operation refer to the NCP3063 data sheet. The essentials of the control method can be observed in the waveforms of Figure 2. The output voltage is fed back to the inverting input (Pin 5) of the comparator (Figure 1) via a resistor divider. If the output is above or below the setpoint, the comparator “gates” a series of clock cycles through the power switch. Control of the output voltage is achieved by varying the average number of “on cycles” to the number of “off cycles” in a given time interval.

The transfer functions (or gain) $V_{\text{OUT}}/V_{\text{IN}}$ for buck, boost and buck-boost operation, neglecting circuit losses, are given by the following equations:

- **Buck Transfer Function**
  \[
  G_{\text{BUCK}} = D \quad (\text{eq. 1})
  \]

- **Boost Transfer Function**
  \[
  G_{\text{BOOST}} = \frac{1}{(1 - D)} \quad (\text{eq. 2})
  \]

- **Buck-Boost Transfer Function**
  \[
  G_{\text{Buck-Boost}} = \frac{D}{(1 - D)} \quad (\text{eq. 3})
  \]

If the value $D_{\text{MAX}}$ equal to 0.86 is inserted into the above equations, the maximum gain available for each topology is determined.

- Maximum buck gain = 0.86
- Maximum boost gain = 7.14
- Maximum buck-boost gain = 6.14

The maximum gain values indicated above may be considerably more than a particular application requires. For example a 12 V to 5 V buck application requires a gain of 0.42 and a corresponding $D = 0.42$, a 12 V to 19 V boost application requires a gain of 1.58 resulting in a nominal $D = 0.37$, while a 12 V to 12 V buck-boost application requires unity gain and $D = 0.5$. Hence dependent on the application, the ratio of “on pulses” to “off pulses” can be very large or very small, to maintain output regulation against a given set point. In turn, this may result increased output ripple, requiring a large output capacitor. In extreme cases, audible noise generation is possible, if the pulse repetition rate is in the audio band.

The addition of a feedforward resistor can help to alleviate these issues. The ramp circuit is modified as illustrated in Figure 3 by the addition of an external current source $I_{\text{FF}}$ at the $C_T$ pin. This current source, in the simplest case, is created by adding a resistor between $V_{\text{IN}}$ and $C_T$.

![Figure 3.](image)
Adding an external current will reduce the time it takes to charge the CT capacitor between the ramp’s minimum and maximum thresholds. The design equations relating to the oscillator section are given below.

\[ T_{ON} = \frac{C_T \cdot V_{RAMP}}{\sum I_{CHARGE}} \]  \hspace{1cm} (eq. 4)

\[ T_{OFF} = \frac{C_T \cdot V_{RAMP}}{\sum I_{DISCHARGE}} \]  \hspace{1cm} (eq. 5)

\[ T_S = \left( T_{ON} + T_{OFF} \right) \]  \hspace{1cm} (eq. 6)

\[ D_{MOD} = \frac{T_{ON}}{T_{OFF}} \]  \hspace{1cm} (eq. 7)

\[ F_S = \frac{1}{T_S} \]  \hspace{1cm} (eq. 8)

Table 1 shows the corresponding reduction in duty cycle \( D_{MOD} \) as a normalized function of the charging and discharging currents flowing into the timing capacitor \( C_T \). The table also shows the change in normalized oscillator frequency.

Once an optimum duty cycle has been identified and \( I_{FF} \) selected, the value of \( C_T \) can be ratio metrically adjusted to set the design frequency. Once set, the frequency variation against duty cycle is small over a wide range of external charging currents.

**Table 1. VARIATION OF DUTY CYCLE \( D_{MOD} \) AND FREQUENCY \( F_{MOD} \) AS A FUNCTION OF NORMALIZED EXTERNAL CURRENT, CHARGING THE TIMING CAPACITOR \( C_T \).**

<table>
<thead>
<tr>
<th>External Charging Current</th>
<th>Internal Charging Current</th>
<th>Internal Discharging Current</th>
<th>Duty Cycle ( D_{MOD} )</th>
<th>Frequency ( F_{MOD} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>6</td>
<td>0.86</td>
<td>1.00</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
<td>0.71</td>
<td>1.43</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>4</td>
<td>0.66</td>
<td>1.71</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
<td>3</td>
<td>0.50</td>
<td>1.71</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
<td>2</td>
<td>0.29</td>
<td>1.43</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>1</td>
<td>0.14</td>
<td>0.86</td>
</tr>
</tbody>
</table>
Practical Example

Figure 4 is a schematic of a noninverting buck–boost topology. The input is a nominal 12 VIN while the output is regulated to 12 VOUT. Assuming no circuit losses, the transfer function or gain of this application is unity and the duty cycle determined from the buck boost transfer function is 0.5. Referring to Table 1, a 3:1 ratio for the external charging current to internal charging current would generate a modified duty DMOD of 0.5.

However, to accommodate conduction and switching losses in the power components, we will start by selecting a 2:1 ratio, providing a DMOD of 0.66 and modified gain (Equation 3) of 0.66/0.34 or 1.94.

The nominal charge and discharge currents for the NCP3063 are listed below:

- Charging Current is 260 μA @ 5 V VCC / 25°C and 280 μA @ 40 V VCC / 25°C.
- Discharging Current is 1550 μA @ 5 V VCC / 25°C and 1700 μA @ 40V VCC / 25°C.

The data above may be verified from measurements of the CT ramp illustrated in Figure 5 before inserting the feedforward resistor R3 in Figure 4.

Rearranging Equation 4, the charge current ICHARGE is given by the expression

\[ I_{\text{CHARGE}} = C_T \times \Delta V_{\text{RAMP}} / T_{\text{ON}} \]  

(eq. 9)
Substituting the measured values taken from the ramp waveform in Figure 5 into Equation 9,
\[
I_{\text{CHARGE}} = 1800 \ \text{pF} * 628 \ \text{mV} / 4.18 \ \mu\text{S} = 270 \ \mu\text{A}
\]
which corresponds to the data above.

For \(D_{\text{MOD}}\) of 0.66, we require an external current of 520 \(\mu\text{A}\). The average ramp voltage from Figure 5 is 0.9 V and \(V_{\text{IN}}\) is nominally 12 V, hence the value of the feedforward resistor \(R_3\) may be determined from the expression \((12 \text{ V} - 0.9 \text{ V})/520 \ \mu\text{A}\) or 21.3 k\(\Omega\). A preferred value of 20 k\(\Omega\) is selected; \(I_{\text{FF}}\) is then 555 \(\mu\text{A}\).

\[
\begin{align*}
\sum I_{\text{CHARGE}} &= 555 \ \mu\text{A} + 270 \ \mu\text{A} = 0.825 \ \text{mA} \\
\sum I_{\text{DISCHARGE}} &= 1550 \ \mu\text{A} - 555 \ \mu\text{A} = 0.995 \ \text{mA}
\end{align*}
\]

From Table 1, it is apparent that in order to maintain the same switching frequency \(F_S\) after an external current source is added in circuit, the value of the timing capacitor \(C_T\) has to be increased by a design factor 1.72 times. Here \(C_T\) was increased to 3.9 n\(\text{F}\).

\[
C_T \times \Delta V_{\text{RAMP}} = 3.9 \ \text{nF} \times 560 \ \text{mV} = 2.18 \times 10^{-9}
\]

Substituting the values above into Equations 4 and 5 gives:
\[
\begin{align*}
T_{\text{ON}} &= 2.64 \ \mu\text{s} \\
T_{\text{OFF}} &= 2.19 \ \mu\text{s} \\
T_S &= (T_{\text{ON}} + T_{\text{OFF}}) = 4.83 \ \mu\text{s} \\
D_{\text{MOD}} &= \frac{T_{\text{ON}}}{T_S} = 0.547 \\
F_S &= \frac{1}{T_S} = 207 \text{ kHz}
\end{align*}
\]

The modified ramp is captured in Figure 6.

Data measured from the ramp waveform in Figure 6 is given below and shows good correlation with the calculated results above.

\[
\begin{align*}
T_{\text{ON}} &= 2.68 \ \mu\text{s} \\
T_{\text{OFF}} &= 2.28 \ \mu\text{s} \\
T_S &= (T_{\text{ON}} + T_{\text{OFF}}) = 4.96 \ \mu\text{s} \\
D_{\text{MOD}} &= \frac{T_{\text{ON}}}{T_S} = 0.54 \\
F_S &= \frac{1}{T_S} = 202 \text{ kHz}
\end{align*}
\]

The output ripple across a 33 \(\mu\text{F}\) electrolytic and 20 \(\mu\text{F}\) MLCC capacitors in parallel is shown in Figure 7. The output voltage is regulated at 11.9 V. The ripple is 70 mV peak to peak with a repetition rate around 9 kHz.

The collector waveform of the NPN transistor Q2 and modified \(C_T\) ramp are illustrated in Figure 8. It is observed that energy is flowing from primary to secondary for many switching cycles to support the 100 mA output load. The converter was then operated without feedforward at the same switching frequency. The output capacitor bank and the load were identical. The output ripple is shown in Figure 9.
The collector waveform of the NPN transistor Q2 and D\text{MAX} ramp is shown in Figure 10. Here it is evident that the energy flow to support the same 100 mA output is drawn from the input in five switching cycles, during which time the voltage on the output capacitor C2 is increased by 1.2 V. C2 is discharged by the output load for several hundred microseconds before the gate oscillator in the NCP3063 restarts.

**Conclusion**

By summing an external current source into the C\text{T} pin of the NCP3063, it is possible to optimize the open loop gain of buck, boost or buck boost topologies for any given application. Reducing the controller’s maximum duty cycle of 0.86 to a lower value D\text{MOD} allows the power components to be designed for lower stress. Input capacitors, output capacitors, inductor, switches and diodes can all benefit from the D\text{MAX} reduction. The effect of output capacitor ripple was investigated in the particular case of a buck–boost topology. It is evident that a large reduction in output capacitor is possible when a single resistor feedforward function is implemented. This technique can also be applied to the MC33063/MC34063 but be aware that the ramp charge and discharge currents are different.