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## Using Critical Conduction Mode for High Power Factor Correction

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### APPLICATION NOTE

#### Introduction

Power Factor Correction (PFC) is very much a necessity for off-line switchmode power supplies requiring output powers of 75 watts or more. Boost converters using discontinuous mode and critical conduction mode design approaches to PFC have been mostly relegated to the low power end of the power spectrum because of the low cost and simplicity of the circuitry. It turns out that the critical conduction mode approach offers the same simplicity and low cost for power factor correctors in the kilowatt range and can additionally offer several performance advantages over the more conventional continuous conduction mode typically used in this power range.

#### Continuous Conduction Mode versus Critical Conduction Mode

Continuous conduction mode is typically chosen for high power PFC designs because it offers the lowest peak to average current ratio for the converter throughput power, and it operates at a fixed switching frequency. The low peak to average current ratio minimizes the power mosfet peak current and output (bulk) capacitor ripple current requirements. Referring to the typical PFC boost pre-converter in Figure 1, the inductance value of the choke and the switching frequency are chosen such that the dc component of current in the choke never goes to zero during any part of the switching cycle for most of the upper end of the PFC load range.

Despite the advantage of the lower peak to average current ratio in the continuous mode PFC boost converter, there are several significant disadvantages associated with this conversion mode:

1. The “hard” reverse recovery of the output diode when the mosfet switch turns on and the generation of high frequency EMI harmonic products is probably the most significant disadvantage. Keep in mind that forward current will normally be flowing through the diode when the mosfet turns on due to the continuous mode of operation. For high power designs the output diode must be of the ultra-fast, soft-recovery type. Otherwise additional circuitry composed of tapped chokes, saturable inductors, or resonant snubbing networks are required to soften the reverse current transient of the diode and the switching mosfet turn-on.
2. The control algorithm to assure maximum power factor and minimum harmonic distortion over the full AC input range and output load range is very complex and requires significant external circuitry in most cases to provide the bias and sense levels required by the most commonly used continuous mode control chip. In most high power continuous mode PFC designs significant circuit and layout “tweaking” may be necessary before reliable operation and low conducted EMI emissions are assured.

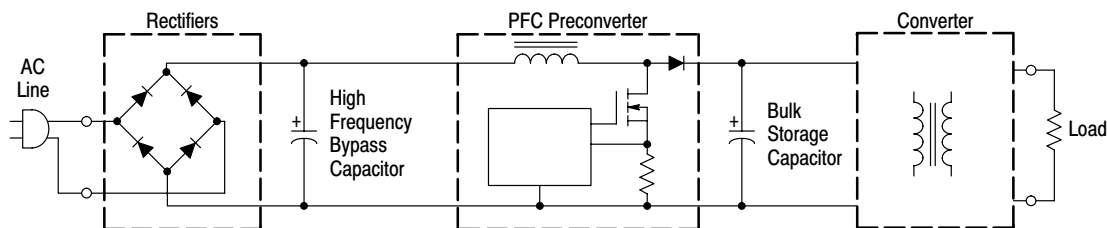
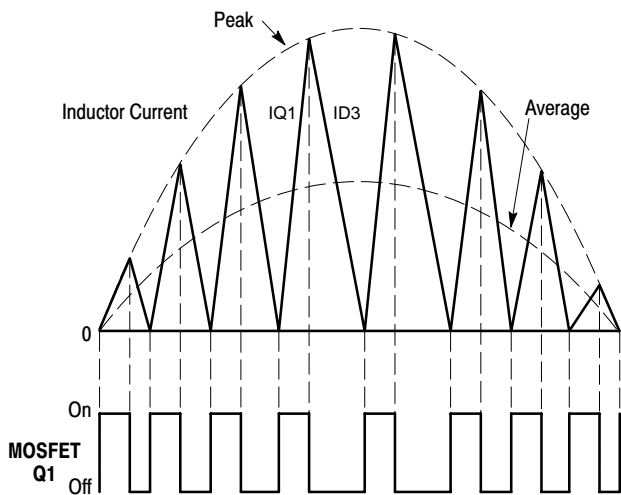


Figure 1. Active Power Factor Correction Preconverter

In critical conduction mode operation, sometimes referred to as boundary mode or transition mode operation, the inductor current is allowed to completely go to zero before the next switching cycle of the mosfet is initiated. Figure 2 illustrates the inductor current waveform with the mains current envelope superimposed to show their relationship. In order for the critical conduction mode technique to work properly, a means of sensing when the inductor current has reached zero is imperative. This is done most effectively by a small auxiliary sense winding on the boost choke that indicates when the flyback voltage across the winding has dropped to less than a volt or so. Sensing zero current by this indirect method is much more noise immune than sensing the current directly. A consequence of having to sense for the zero current point prior to mosfet turn-on disallows fixed frequency operation in this mode. In fact the frequency will typically vary over a 5:1 range from the midpoint in the AC sinewave to the zero crossing point. Changes in the output load and/or the nominal line operating point will also cause shifts in the median operating frequency.



**Figure 2. Inductor Current and MOSFET Gate Voltage Waveforms**

The major disadvantage of critical conduction mode operation is the high peak currents in the mosfet and output diode. It turns out that a careful analysis of the rms ripple current in the output capacitor shows that it is only about 1.3 times that of an equivalent continuous mode PFC stage due to the triangular waveshape of the current and its associated rms value. By using a high speed, higher current density

IGBT for the boost switch, the peak currents and their impact become less significant and the following advantages of this design approach can be realized:

1. The output diode essentially self-commutates off because the current is zero in the device before the IGBT turns on. In many cases a conventional fast recovery diode can be used for the boost output rectifier and heatsinking may not be necessary because all diode losses are due to forward conduction.
2. The IGBT (or mosfet) switch sees zero current switching at turn-on so heating due to switching losses and EMI are generated only when the power switch turns off. It should also be noted that the switching frequency is lowest when the input line peaks are maximum and hence the power switch currents are at their maximum. Maximum switching frequency and minimum switch current occurs around the zero crossing point of the AC line envelope.
3. The average EMI is further reduced by the constantly shifting or “dithering” effect of the variable frequency operation of the PFC.
4. The control algorithm for achieving high power factor and low harmonic distortion using this mode is extremely simple and can be accomplished with ON Semiconductor’s MC33262 eight pin control chip and a minimum of external components.
5. The required inductance for the boost choke is approximately one fourth of that typically required for continuous mode chokes. This means fewer turns and less expensive chokes in most cases. It can be shown that for lowest harmonic distortion, a choke with a linear B/H response characteristic (i.e. constant inductance) is desirable for critical conduction mode operation. This requires the use of a gapped ferrite core which would typically be a larger structure due to the maximum flux limitations of ferrite than would be the powdered iron or Molypermalloy (MPP) magnetic structures commonly used for continuous mode PFCs. It has been found experimentally, however, that if a more compact choke design is necessary, low loss powdered iron or MPP materials can be used effectively for critical conduction mode as long as the inductance drop caused by the dc bias is no more than about 25% maximum.

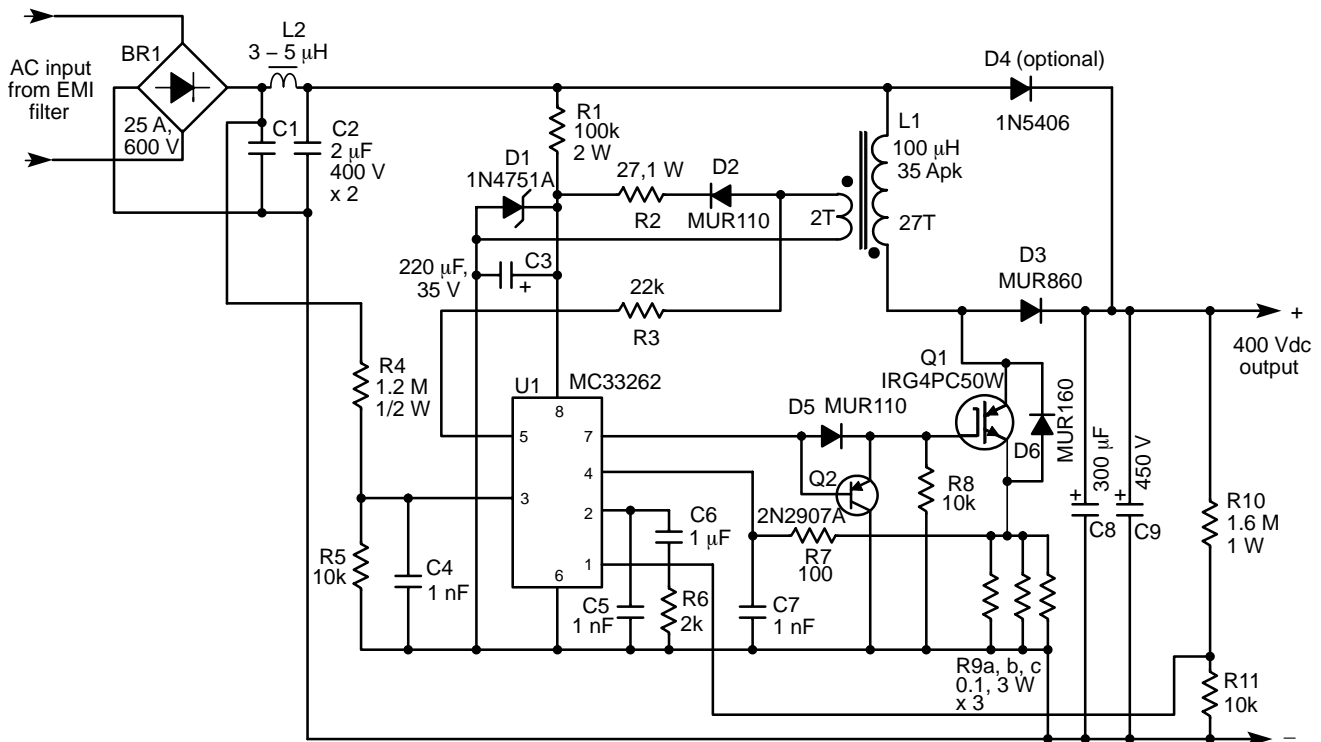
**One Kilowatt Power Factor Corrector**

Figure 3 shows a 1.0 kilowatt, universal input power factor corrector implemented with the ON Semiconductor MC33262 critical conduction mode control chip and a single IGBT. The internal circuit architecture of the chip is shown in Figure 4. Referring to these figures the basic PFC circuit operation is as follows: Input signals to the control chip from the dc output voltage (Pin 1) and the full-wave rectified line voltage (Pin 3) are presented as inputs to a single quadrant, analog voltage multiplier. The output of the multiplier is just a reproduction of the rectified line voltage in which the amplitude is modulated by the PFC dc output voltage so as to achieve output regulation. The multiplier output signal becomes the reference for the current sense comparator. The non-inverting input to this comparator sees the peak IGBT current profile that is developed across current sense resistor R9. The current sense comparator output is now a pulse width and pulse rate modulated signal that eventually drives the gate of the IGBT after some additional logic level signal processing. Note that the next critical level of signal processing is in the R/S latch where the zero current sense detector circuit allows the IGBT to be turned on for the next switching cycle only after the choke current has reached zero. The zero current point is detected indirectly by looking for a complete collapse of the choke flyback voltage via

Pin 5. The end result of this logical process is that the peak current being switched by the IGBT through the choke must track the low frequency sine envelope of the rectified line voltage (see Figure 2). Because of the triangular current waveform produced by the critical conduction control algorithm, it turns out that the average choke current over a line half-cycle is also a sine wave. The end result is that the input line current is forced to be sinusoidal and in phase with the line voltage.

In order for harmonic distortion to be minimal the bandwidth of the voltage control loop must be less than the line frequency. Capacitor C6 sets this point to about 16 Hz. If the bandwidth were wider, the error amplifier would attempt to regulate off the 120 Hz ripple component on output bulk capacitors C8 and C9. This would cause the input current waveshape to start looking like a trapezoidal wave instead of a sine wave. The power factor would still be high but the harmonic distortion would become unacceptable.

For those interested in a detailed mathematical description of power factor corrector circuits operating in critical conduction mode, please see the ON Semiconductor Application Note AND8123/D by Joel Turchi. (see references)



**Figure 3. 1.0 kW Power Factor Controller with MC33262 Controller**

# AND8179/D

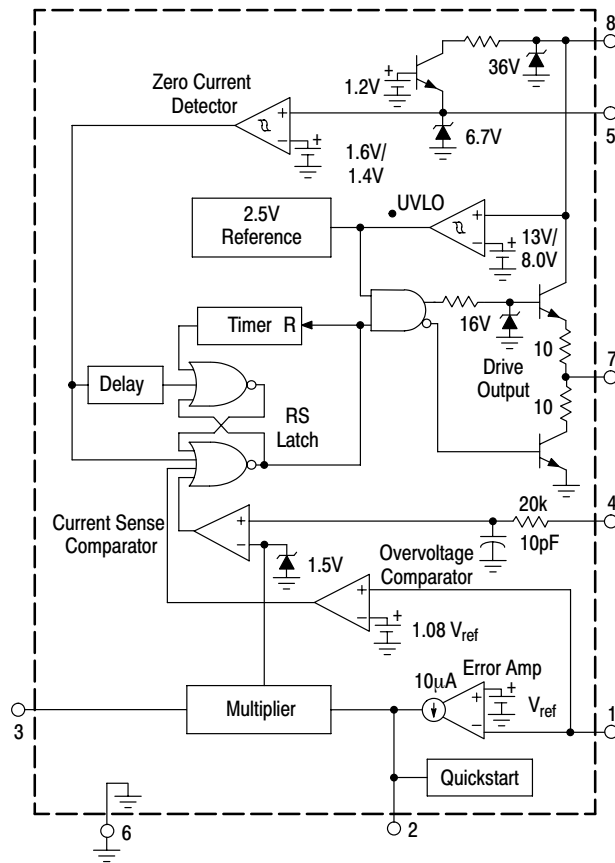


Figure 4. 80 W Power Factor Controller

### Circuit Comments and Performance

The circuit of Figure 3 was constructed and tested with both a resistive load and a 1.0 kW switchmode power supply which was connected to a variable load. The tests using the

“downstream” power supply as a load was done to check for possible switching circuit noise interactions and the stability of the PFC driving a typical “real world” load. The performance data is tabulated below.

Table 1.


Power Out	Vin	Vout	PF	Efficiency	THD (Current)
100 W	120 Vac	396 Vac	0.98	92%	4.0%
100 W	235 Vac	396 Vac	0.96	93%	10.1%
450 W	120 Vac	396 Vac	0.99	96%	2.9%
450 W	235 Vac	396 Vac	0.98	97%	4.0%
1.0 kW	120 Vac	396 Vac	0.99	94%	3.2%
1.0 kW	235 Vac	396 Vac	0.98	96%	5.1%

The following information is from additional data taken during the testing of the 1.0 kW PFC:

1. Heatsinking was required on Q1 and D3 and a small amount of forced air (35 cfm fan) was blown across the breadboard when operated at maximum output power. Thermal losses from L1 were minimal.
2. The inductor L1 was wound on a E55 ferrite core set (Phillips/Ferroxcube E55/28/21-3C90) with 27 turns of 10 strands (twisted) of #26HN magnet wire over approximately 3 layers. The auxiliary winding for the control chip Vcc and zero current sensing was 2 turns of #24 insulated wire spiral wound on top of the main winding and over the width of the main coil. The core was gapped 2 mm in each leg. The main winding inductance was approximately 100  $\mu$ H.
3. Zener diode D1 along with resistor R2 were added to make sure the control chip's operating Vcc did not exceed 30 volts. For power applications of this level a dedicated Vcc supply is recommended, however, this simple approach works satisfactorily.
4. Ultrafast diode D6 was added for reverse transient protection of Q1 because the IGBT does not have an intrinsic body diode like a mosfet does.
5. D4 is an optional 5 amp, 600 volt low frequency diode that prevents resonant voltage ring-up on bulk capacitors C8 and C9 when the AC input is initially applied to the PFC. If the circuit uses appropriate resistive inrush limiting, this diode may not be necessary but is still recommended.
6. The combination of D5 and Q2 form a "speed-off" circuit for the IGBT and dramatically lowers the device's turn-off switching losses.
7. L2 is optional and is comprised of a few turns of #14 wire around a small powered iron toroidal core to give an inductance of about 3 to 5  $\mu$ H. This forms a pi network with polypropylene input capacitors C1 and C2 to help reduce differential mode conducted EMI.
8. Although paralleled current sense resistors R9a through R9c will result in a few watts of dissipation with full power out at low mains input, it is not recommended that a current sense transformer be used as a substitute because of noise effects and propagation delays in sensing the current peaks.
9. It was found that for reliable PFC starting under all output load and universal input conditions, C3 needed to be at least 180  $\mu$ F. If a dedicated Vcc source is used this is not an issue.
10. The optimum values for C4 and C7 will depend on the circuit layout and the resultant common mode noise that exists in the circuit as a whole. C7 will be 1 nF or less for most applications while C4 will be optimum between 1 nF and 10 nF.
11. Keep in mind that an EMI filter will be required before the input rectifier to meet agency requirements for conducted EMI. Common mode EMI in the megahertz range will typically be lower than that produced by an equivalent continuous mode PFC circuit. Lower frequency differential mode EMI components may be higher but should fall below the lower specified agency limit if designed properly.
12. High value resistors R4 and R10 should probably be broken down into series elements adding up to the required resistance. They are shown on the schematic as single resistors for simplicity.

### References:

1. AND8123/D. "Power Factor Controller Stages Operating in Critical Conduction Mode." [www.onsemi.com](http://www.onsemi.com)
2. MC33260/D. "GreenLine™ Compact Power Factor Controller: Innovative Circuit for Cost Effective Solutions." [www.onsemi.com](http://www.onsemi.com)
3. MC34262/D. "Power Factor Controllers." [www.onsemi.com](http://www.onsemi.com)

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