AND8132/D

Performance Improvements to the NCP1012 Evaluation Board

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APPLICATION NOTE

This application note uses the standard NCP1012 evaluation board, referenced in the NCP1010–1014 data sheet. The board includes only the core components needed to demonstrate the operation of the NCP101x; the application note describes modifications to the basic circuit to reduce standby power consumption, increase efficiency, and reduce EMI.

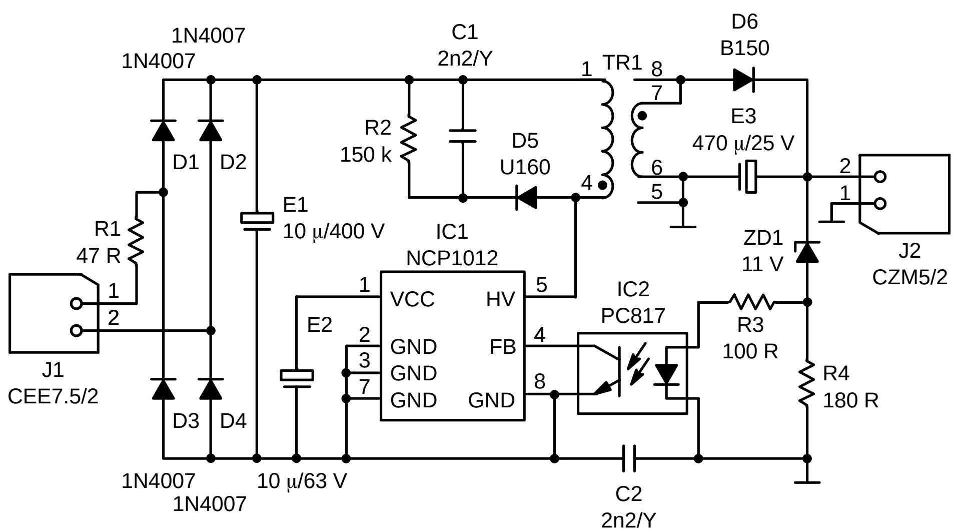

Figure 1. Schematic Diagram of the Demo Board

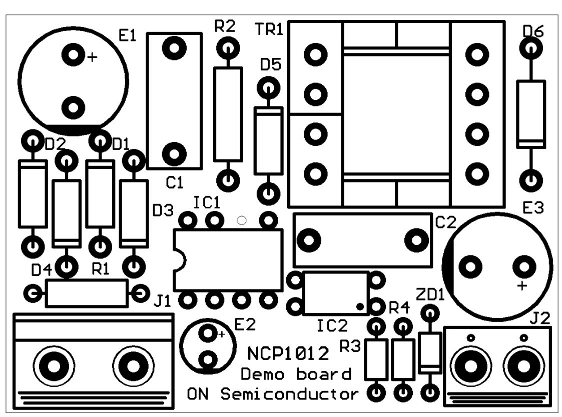

Figure 2. PCB Component Placement

The evaluation board demonstrates the NCP1012 in a 7.0 W SMPS with the universal input voltage range (85 VAC−265 VAC) and an output of 12 V. The schematic of the SMPS is shown in Figure 1, and the component placement in Figure 2. The tested performance of the unmodified board is shown below:

Item	Test 1	Test 2
Vin DC (V)	125	325
Iin DC (mA)	66	25.1
Pin (W)	8.25	8.15
Vout DC (V)	11.99	12.1
Iout DC (mA)	520	520
Pout (W)	6.24	6.29
Efficiency (%)	75.6	77.1
Standby (mW)	638.3	695.6

Feedback Stability: The regulation was tested for stability over the full input voltage range (85 VAC−265 VAC) with a load of 550 mA. No instability was found.

Standby Consumption

Standby power consumption is one of the most important parameters for an SMPS under low− or no−load conditions. In the demo board the main sources of standby power consumption are the NCP1012 Vcc supply, the drain clamp circuit, the feedback loop operating current and various transformer losses. Of these, only the feedback loop operating current and drain clamp circuit can easily be modified.

The **feedback loop operating current** must be calculated properly to achieve good DC voltage stability, adequate dynamic response and acceptable noise immunity. For the simplest case – zener type feedback − a typical operating current is 4.0−6.0 mA. This method is used in the demo board, resulting in 695 mW of standby consumption at 325 VDC. By reducing the operating current of the loop, the standby consumption is reduced, but with negative effects on the noise immunity and accuracy. For example, when bias resistor R4 is removed, the operating current is as low as 335 μA and standby consumption is reduced to 314 mW. In this case circuit operation is still in the non−burst mode, so although the voltage stability is not as good there is still low AC ripple at the output.

A more complicated, but more accurate, solution is based on the TLV431 shunt regulator. This regulator operates correctly at an operating current as low as 100 μA. When used for this design, at no load, due to the high gain, it operates in burst mode. In this mode the complete design has standby consumption as low as 100 mW, but the output voltage is unstable, with noise and AC ripple, as shown in Figure 4.

Output voltage waveforms for both feedback solutions:

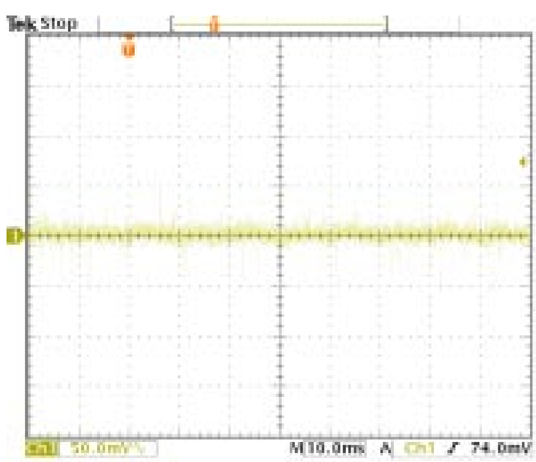

Figure 3. Zener Feedback

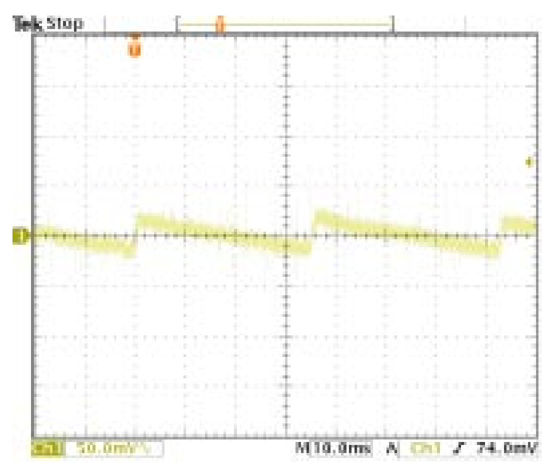

Figure 4. TLV431 Feedback

There are various ways to design the drain clamp circuit. The RDC clamp, used in the evaluation board, is the cheapest and most widely used. This clamp dissipates the peak energy from the transformer and part of the transformed energy. The peak energy need to be dissipated, but the transformed energy not. In case of the demo board this clamp is used. With R4 connected the consumption at 325 V DC input voltage is 695 mW. When R4 is removed, the consumption is reduced to 314 mW.

Another approach is to use a TVS (transient voltage suppressor) clamp. Recommended parts include ON's P6KE200A or SA170A, or the SMD versions of both − P6SMB200AT3 and 1SMB170AT3 respectively. This clamp consists of a high voltage zener diode, or a TVS with an ultrafast rectifier diode in series. The zener clamp voltage is usually set to around 200 V. Using this clamp, the power consumption is significantly reduced. With R4 connected, the consumption is 526 mW at 300 V DC input voltage versus 306 mW with R4 disconnected. The active clamp allows greater reduction of standby power, but is more expensive than the simple RDC clamp.

This TVS clamp solution has positive results not only on the standby consumption, but also on the efficiency both under normal operation and light load conditions. At 100 mA output current and 325 V DC input voltage, the input power drops from 2.94 W with the RDC clamp to 2.83 W with the TVS clamp. For higher output powers the benefit is not so significant.

If the demo board design is intended for production, improvements in EMI performance are needed. For example, an EMI filter is not necessary for the basic function of the SMPS, but it is mandatory for a real−world design. Figure 5 shows the EMI performance for the basic demo board before any modification; conducted emissions at the input are well above the maximum allowed by EN50081−1.

When a 47 nF suppression capacitor X2 is added at the input, the magnitude of the EMI is dramatically reduced. The result is shown in Figure 6. This solution may be usable if X2 is increased to 100 nF or more.

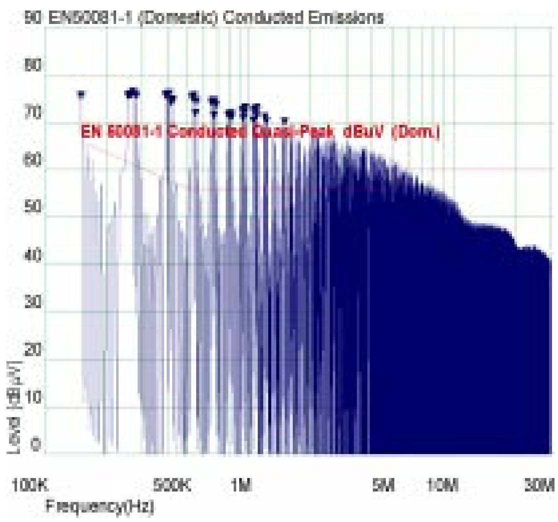

Figure 5. No EMI Filter

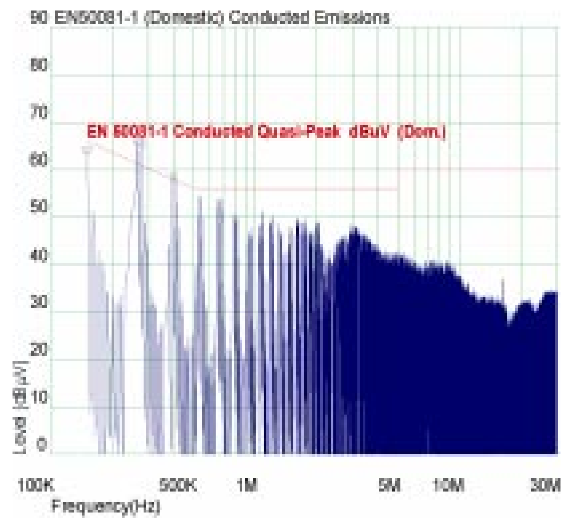

Figure 6. X2 47 n Capacitor at Input

Further improvement results from adding an LC filter L1 and E2 between the rectifier bridge and the bulk capacitor E1, as shown in Figure 7.

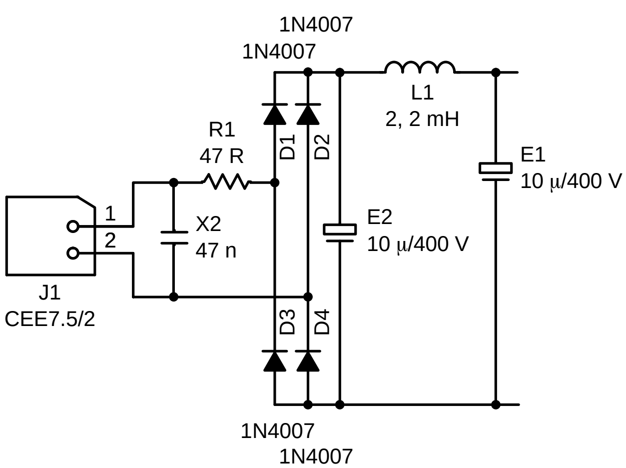

Figure 7. Complete EMI Filter

With L1 and E2, EMI radiation is reduced by more than 20 dBµV. This design is acceptable for production if good PCB layout guidelines are followed. Figure 8 shows the improvement in conducted emissions as a result of adding capacitor X2 and coil L1 only; Figure 9 shows the result of implementing the complete EMI filter.

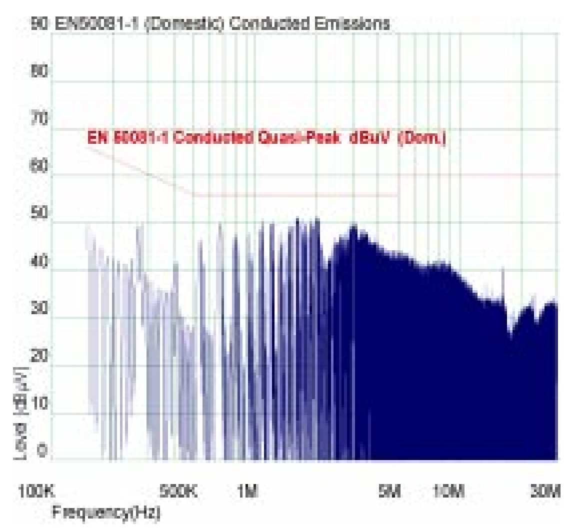

Figure 8. Coil + X2 Capacitor

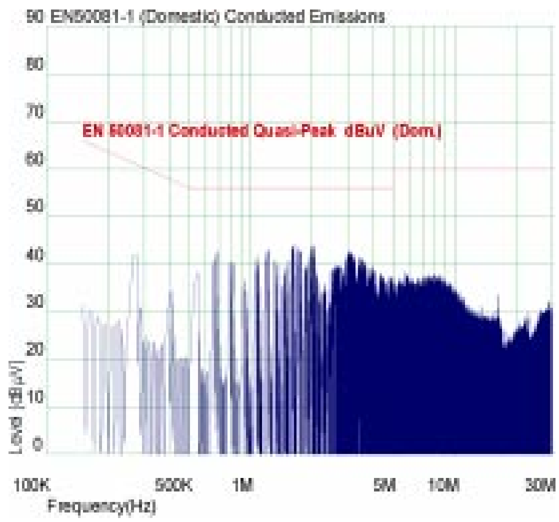

Figure 9. Complete EMI Filter

Bills of material used for the standard and TVS versions of the demo board:

Standard Version

Part	Value	Package	Manuf.
MMM			
C1	2n2/Y2	R41	Arcotronics
C2	2n2/Y2	R41	Arcotronics
D1	**1N4007**	**DO−41**	**ON Semiconductor**
D2	**1N4007**	**DO−41**	**ON Semiconductor**
D3	**1N4007**	**DO−41**	**ON Semiconductor**
D4	**1N4007**	**DO−41**	**ON Semiconductor**
D5	**MUR160**	**59−04**	**ON Semiconductor**
D6	**MBR150**	**59−04**	**ON Semiconductor**
E1	10 μ/400 V	NHG	Panasonic
E2	10 μ/63 V	KMG	Nippon
E3	470 μ/25 V	KMF	Nippon
IC1	**NCP1012**	**DIP 7**	**ON Semiconductor**
IC2	PC817	DIP 4	Sharp
J1	CEE7.5/2	CEE7,5/2	Various
J2	CZM5/2	CZM5/2	Various
R1	47 R	RM10	Vishay
R2	150 k	RM12,5	Vishay
R3	100 R	RM6,35	Vishay
R4	180 R	RM6,35	Vishay
TR1	TR−NCP1012	EF16 Hor.	P&V Elektronic
ZD1	**1N5241B**	**DO−204AH**	**ON Semiconductor**

TVS Version

Part	Value	Package	Manuf.
MMM			
C1	NU		
C2	2n2/Y2	R41	Arcotronics
D1	**1N4007**	**DO−41**	**ON Semiconductor**
D2	**1N4007**	**DO−41**	**ON Semiconductor**
D3	**1N4007**	**DO−41**	**ON Semiconductor**
D4	**1N4007**	**DO−41**	**ON Semiconductor**
D5	**MUR160**	**59−04**	**ON Semiconductor**
D6	**MBR150**	**59−04**	**ON Semiconductor**
E1	10 μ/400 V	NHG	Panasonic
E2	10 μ/63 V	KMG	Nippon
E3	470 μ/25 V	KMF	Nippon
IC1	**NCP1012**	**DIP 7**	**ON Semiconductor**
IC2	PC817	DIP 4	Sharp
J1	CEE7.5/2	CEE7,5/2	Various
J2	CZM5/2	CZM5/2	Various
R1	47 R	RM10	Vishay
R2	**P6KE200A**	**SURMETIC 40**	**ON Semiconductor**
R3	100 R	RM6,35	Vishay
R4	180 R	RM6,35	Vishay
TR1	TR−NCP1012	EF16 Hor.	P&V Elektronic
ZD1	**1N5241B**	**DO−204AH**	**ON Semiconductor**

Notes

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