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Power Factor Correction Stages Operating in Critical Conduction Mode

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APPLICATION NOTE

This paper proposes a detailed and mathematical analysis of the operation of a critical conduction mode Power factor Corrector (PFC), with the goal of easing the PFC stage dimensioning. After some words on the PFC specification and a brief presentation of the main critical conduction schemes, this application note gives the equations necessary for computing the magnitude of the currents and voltages that are critical in the choice of the power components.

Introduction

The IEC1000−3−2 specification, usually named Power Factor Correction (PFC) standard, has been issued with the goal of minimizing the Total Harmonic Distortion (THD) of the current that is drawn from the mains. In practice, the legislation requests the current to be nearly sinusoidal and in phase with the AC line voltage.

Active solutions are the most effective means to meet the legislation. A PFC pre-regulator is inserted between the input bridge and the bulk capacitor. This intermediate stage is designed to output a constant voltage while drawing a sinusoidal current from the line. In practice, the step-up (or boost) configuration is adopted, as this type of converter is easy to implement. One can just notice that this topology requires the output to be higher than the input voltage. That is why the output regulation level is generally set to around 400 V in universal mains conditions.

BASICS OF THE CRITICAL CONDUCTION MODE

Critical conduction mode (or border line conduction mode) operation is the most popular solution for low power applications. Characterized by a variable frequency control scheme in which the inductor current ramps to twice the desired average value, ramps down to zero, then immediately ramps positive again (refer to Figures 2 and 4), this control method has the following advantages:

- *Simple Control Scheme:* The Application Requires Few External Components
- *Ease of Stabilization:* The Boost Keeps the First Order Converter and There is No Need for Ramp Compensation
- *Zero Current Turn On:* One Major Benefit of Critical Conduction Mode is the MOSFET Turn On when the Diode Current Reaches Zero. Therefore the MOSFET Switch On is Lossless and Soft and there is No Need for a Low trr Diode

On the other hand, the critical conduction mode has some disadvantages:

- Large Peak Currents that Result in High dI/dt and rms Currents Conducted throughout the PFC Stage
- Large Switching Frequency Variations as Detailed in the Paper

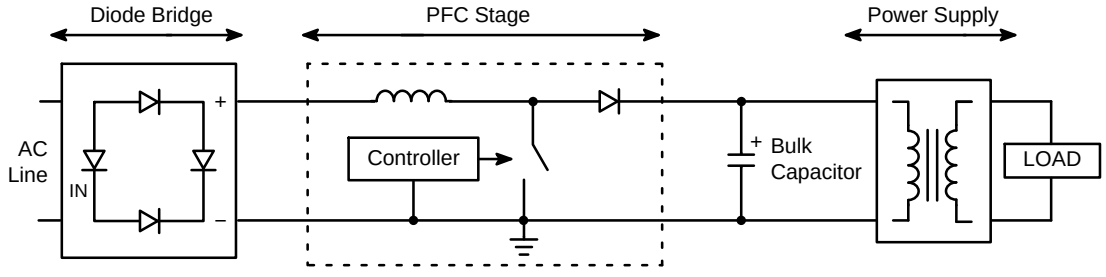

Figure 1. Power Factor Corrected Power Converter

PFC boost pre-converters typically require a coil, a diode and a Power Switch. This stage also needs a Power Factor Correction controller that is a circuit specially designed to drive PFC pre-regulators. ON Semiconductor has developed three controllers (MC33262, MC33368 and MC33260) that operate in critical mode and the NCP1650 for continuous mode applications.

One generally devotes critical conduction mode to power factor control circuits below 300 W.

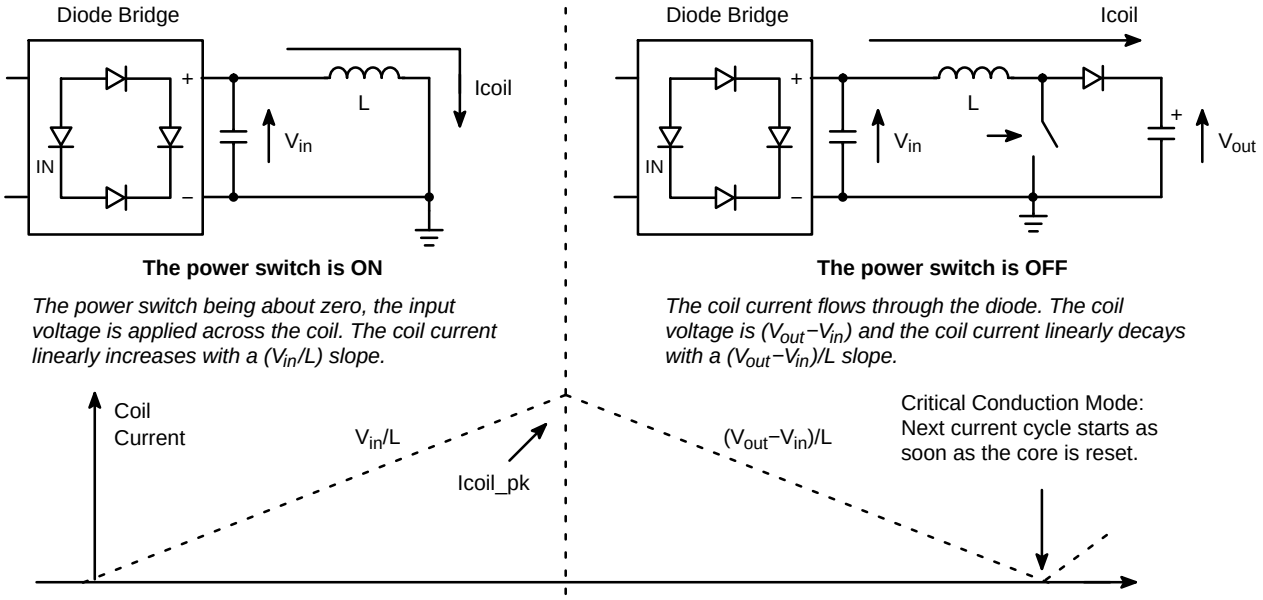

Figure 2. Switching Sequences of the PFC Stage

In critical discontinuous mode, a boost converter presents two phases (refer to Figure 2):

- The on-time during which the power switch is on. The inductor current grows up linearly according to a slope (V_{in}/L) where V_{in} is the instantaneous input voltage and L the inductor value.
- The off time during which the power switch is off. The inductor current decreases linearly according to the slope (V_{out}−V_{in})/L where V_{out} is the output voltage. This sequence terminates when the current equals zero.

Consequently, a triangular current flows through the coil. The PFC stage adjusts the amplitude of these triangles so that in average, the coil current is a (rectified) sinusoid (refer to Figure 4). The EMI filter (helped by the 100 nF to 1.0 μF input capacitor generally placed across the diodes bridge output), performs the filtering function.

The more popular scheme to control the triangles magnitude and shape the current, forces the inductor peak current to follow a sinusoidal envelope. Figure 3 diagrammatically portrays its operation mode that could be summarized as follows:

- The diode bridge output being slightly filtered, the input voltage (V_{in}) is a rectified sinusoid. One pin of the PFC controller receives a portion of V_{in}. The voltage of this terminal is the shaping information necessary to build the current envelope.
- An error amplifier evaluates the power need in response to the error it senses between the actual and wished levels of the output voltage. The error amplifier bandwidth is set low so that the error amplifier output reacts very slowly and can be considered as a constant within an AC line period.
- The controller multiplies the shaping information by the error amplifier output voltage. The resulting product is the desired envelope that as wished, is sinusoidal, in phase with the AC line and whose amplitude depends on the amount of power to be delivered.
- The controller monitors the power switch current. When this current exceeds the envelope level, the PWM latch is reset to turn off the power switch.
- Some circuitry detects the core reset to set the PWM latch and initialize a new MOSFET conduction phase as soon as the coil current has reached zero.

Consequently, when the power switch is ON, the current ramps up from zero up to the envelope level. At that moment, the power switch turns off and the current ramps down to zero (refer to Figures 2 and 4). For simplicity of the drawing, Figure 4 only shows 8 “current triangles”. Actually, their frequency is very high compared to the AC line one. The input filtering capacitor and the EMI filter averages the “triangles” of the coil current, to give:

$$< Icoil >_T = \frac{Icoil\_pk}{2} \qquad \text{(eq. 1)}$$

where $<Icoil>_T$ is the average of one current triangle (period T) and Icoil_pk is the peak current of this triangle.

As Icoil_pk is forced to follow a sinusoidal envelop ($k*V_{in}$), where k is a constant modulated by the error amplifier, $<Icoil>_T$ is also sinusoidal:

$$\left(< Icoil >_T = \frac{k * Vin}{2} = \frac{k * \sqrt{2} * Vac * \sin(\omega t)}{2} \right) \qquad \text{(eq. 2)}$$

As a result, this scheme makes the AC line current sinusoidal.

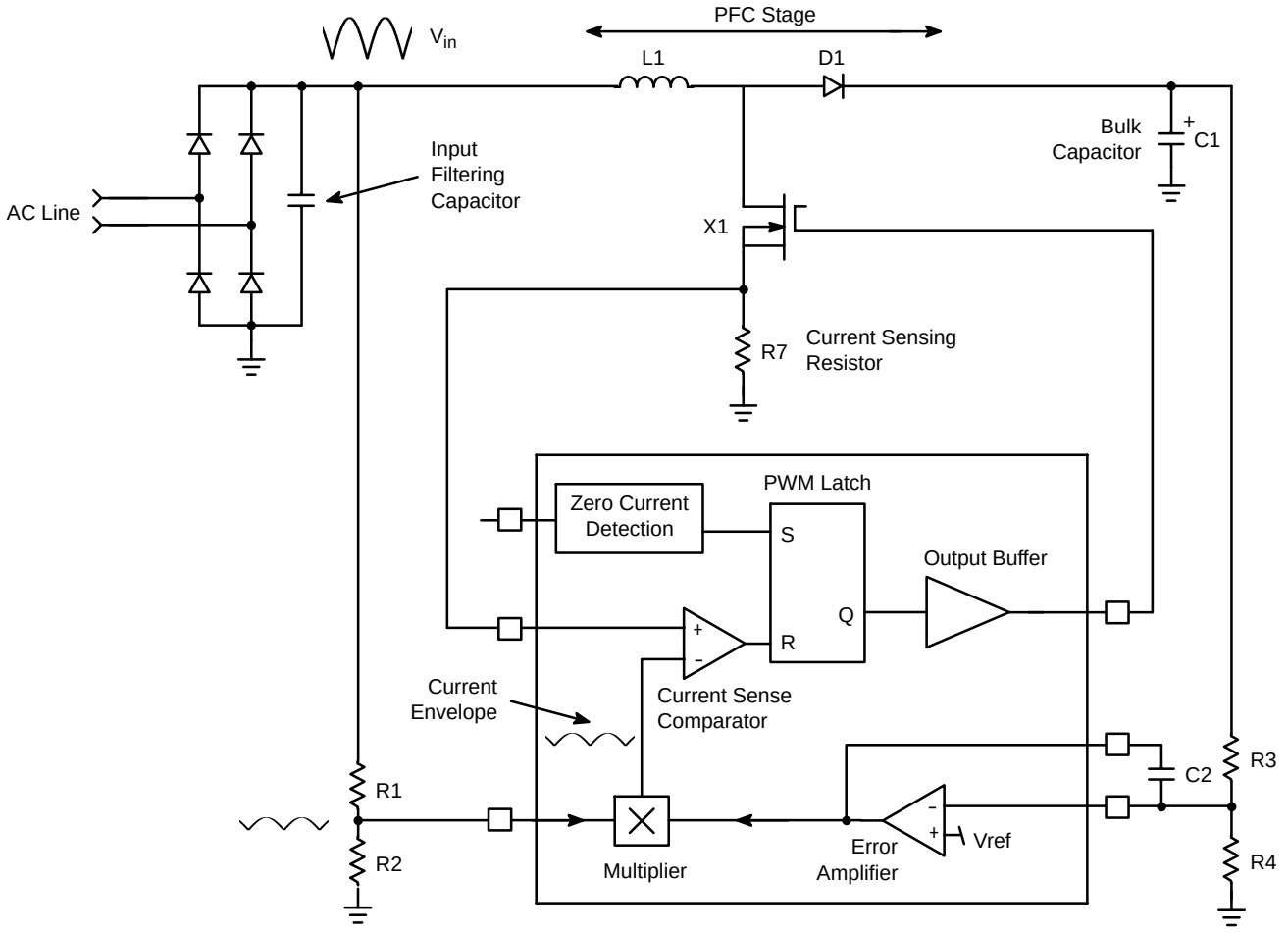

Figure 3. Switching Sequences of the PFC Stage

The controller monitors the input and output voltages and using this information and a multiplier, builds a sinusoidal envelope. When the sensed current exceeds the envelope level, the Current Sense Comparator resets the PWM latch and the power switch turns off. Once the core has reset, a dedicated block sets the PWM latch and a new MOSFET conduction time starts.

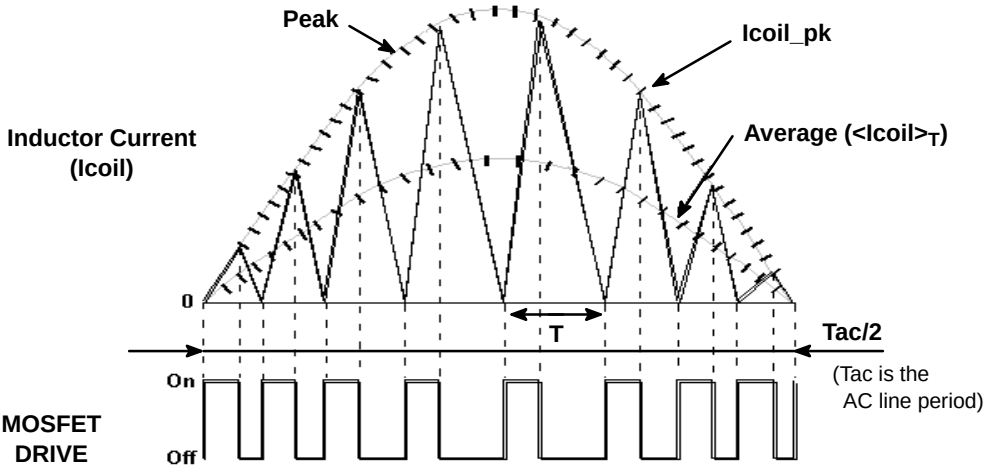

Figure 4. Coil Current

During the power switch conduction time, the current ramps up from zero up to the envelope level. At that moment, the power switch turns off and the current ramps down to zero. For simplicity of the drawing, only 8 “current triangles” are shown. Actually, their frequency is very high compared to the AC line one.

One can note that a simple calculation would show that the on-time is constant over the sinusoid: $ton = 2 * L * \frac{< Pin >}{Vac^2}$ and that the switching frequency modulation is brought by the off-time that equals:

$$toff = 2 * \sqrt{2} * L * \frac{< Pin >}{Vac * (Vout - \sqrt{2} * Vac * \sin(\omega t))} * \sin(\omega t) = ton * \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout - \sqrt{2} * Vac * \sin(\omega t)} \quad \text{(eq. 3)}$$

That is why the MC33260 developed by ON Semiconductor does not incorporate a multiplier inputting a portion of the rectified AC line to shape the coil current. Instead, this part forces a constant on-time to achieve in a simplest manner, the power factor correction.

MAIN EQUATIONS

Switching Frequency

As already stated, the coil current consists of two phases:

- The power switch conduction time (ton). During this time, the input voltage applies across the coil and the current increases linearly through the coil with a (V_{in}/L) slope:

$$Icoil(t) = \frac{Vin}{L} * t \quad \text{(eq. 4)}$$

This phase ends when the conduction time (ton) is complete that is when the coil current has reached its peak value (Icoil_pk). Thus:

$$Icoil\_pk = \frac{Vin}{L} * ton \quad \text{(eq. 5)}$$

The conduction time is then given by:

$$ton = \frac{L * Icoil\_pk}{Vin} \quad \text{(eq. 6)}$$

- The power switch off time (toff). During this second phase, the coil current flows through the output diode and feeds the output capacitor and the load. The diode voltage being considered as null when on, the voltage across the coil becomes negative and equal to (V_{in}−V_{out}). The coil current decreases then linearly with the slope ((V_{out}−V_{in})/L) from (Icoil_pk) to zero, as follows:

$$Icoil(t) = Icoil\_pk - \left(\frac{Vout - Vin}{L} * t\right) \quad \text{(eq. 7)}$$

This phase ends when Icoil reaches zero, then the off−time is given by the following equation:

$$toff = \frac{L * Icoil\_pk}{Vout - Vin} \quad \text{(eq. 8)}$$

The total current cycle (and then the switching period, T) is the sum of ton and toff. Thus:

$$T = ton + toff = L * Icoil\_pk * \frac{Vout}{Vin * (Vout - Vin)} \quad \text{(eq. 9)}$$

As shown in the next paragraph (equation 17), the coil peak current can be expressed as a function of the input power and the AC line rms voltage as follows:

$$Icoil\_pk = 2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t) \quad \text{(eq. 10)}$$

Where ω is the AC line angular frequency. Replacing Icoil_pk by this expression in equation (9) leads to:

$$T = 2 * \sqrt{2} * \frac{L * < Pin >}{Vac} * \sin(\omega t) * \frac{Vout}{\sqrt{2} * Vac * \sin(\omega t) * (Vout - Vin)} \quad \text{(eq. 11)}$$

This equation simplifies:

$$T = \frac{2 * L * < Pin > * Vout}{Vac^2 * (Vout - Vin)} \quad \text{(eq. 12)}$$

The switching frequency is the inverse of the switching period. Consequently:

$$\mathbf{f = \frac{Vac^2}{2 * L * < Pin >} \left(1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout}\right)} \quad \text{(eq. 13)}$$

This equation shows that the switching frequency consists of:

- One term $\left(\frac{Vac^2}{2 * L * < Pin >}\right)$ that only varies versus the working point (load and AC line rms voltage).
- A modulation factor $\left(1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout}\right)$ that makes the switching frequency vary within the AC line sinusoid.

The following figure illustrates the switching frequency variations versus the AC line amplitude, the power and within the sinusoid.

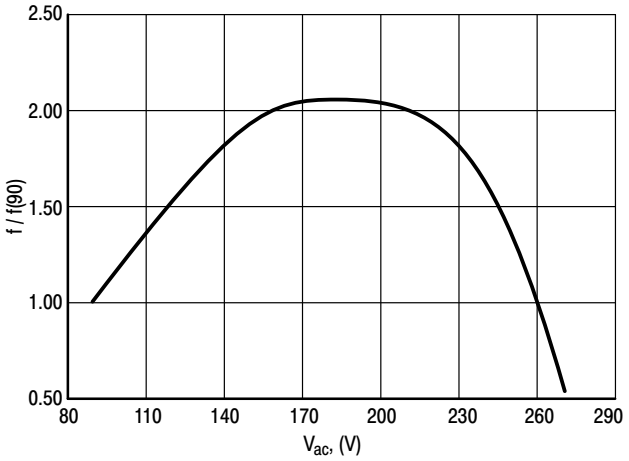

Figure 5. Switching Frequency Over the AC Line RMS Voltage (at the Sinusoid top)

The figure represents the switching frequency variations versus the line rms voltage, in a normalized form where f(90) = 1. The plot drawn for V_{out} = 400 V, shows large variations (200% at Vac = 180 V, 60% at Vac = 270 V). The shape of the curve tends to flatten if V_{out} is higher. However, the minimum of the switching frequency is always obtained at one of the AC line extremes (VacLL or VacHL where VacLL and VacHL are respectively, the lowest and highest Vac levels).

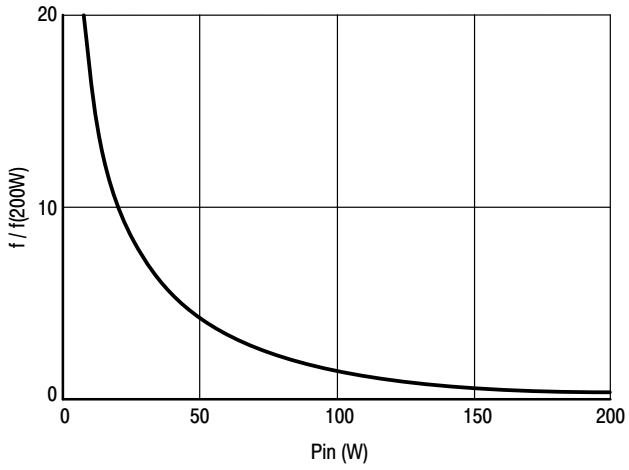

Figure 6. Switching Frequency vs. the Input Power (at the Sinusoid top)

This plot sketches the switching frequency variations versus the input power in a normalized form where f(200 W) = 1. The switching frequency is multiplied by 20 when the power is 10 W. In practice, the PFC stage propagation delays clamp the switching frequency that could theoretically exceed several megaHertz in very light load conditions. The MC33260 minimum off-time limits the no load frequency to around 400 kHz.

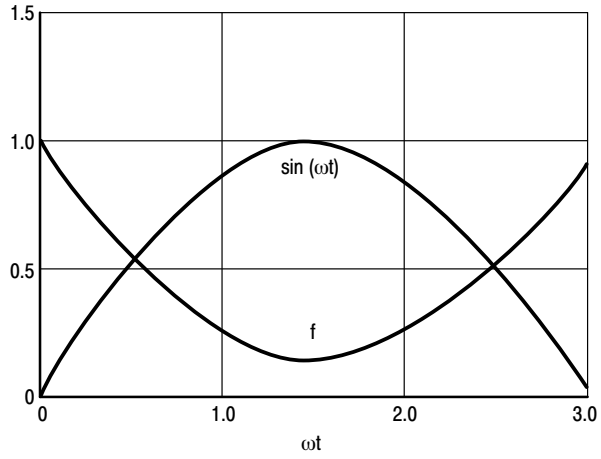

Figure 7. Switching Frequency Over the AC Line Sinusoid @ 230 Vac

This plot gives the switching variations over the AC line sinusoid at Vac = 230 V and V_{out} = 400 V, in a normalized form where f is taken equal to 1 at the AC line zero crossing. The switching frequency is approximately divided by 5 at the top of the sinusoid.

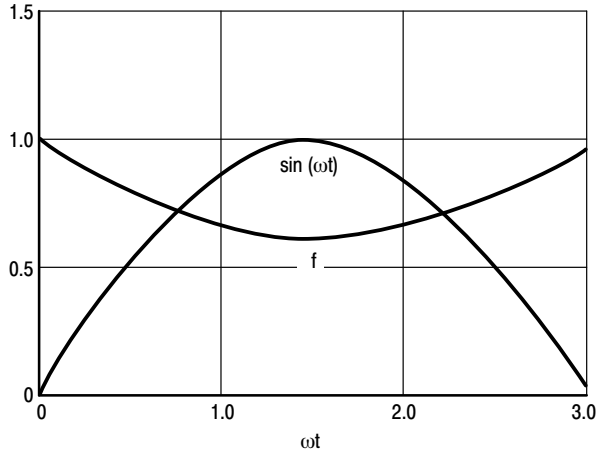

Figure 8. Switching Frequency Over the AC Line Sinusoid @ 90 Vac

This plot shows the same characteristic but for Vac = 90 V. Similarly to what was observed in Figure 5 (f versus Vac), the higher the difference between the output and input voltages, the flatter the switching frequency shape.

Finally, the switching frequency dramatically varies within the AC line and versus the power. This is probably the major inconvenience of the critical conduction mode operation. This behavior often makes tougher the EMI

filtering. It also can increase the risk of generating interference that disturb the systems powered by the PFC stage (for instance, it may produce some visible noise on the screen of a monitor).

In addition, the variations of the frequency and the high values it can reach (up to 500 kHz) practically prevent the use of effective tools to damp EMI and reduce noise like snubbing networks that would generate too high losses.

One can also note that the frequency increases when the power diminishes and when the input voltage increases. In light load conditions, the switching period can become as low as 2.0 μs (500 kHz). All the propagation delays within the control circuitry or the power switch reaction times are no more negligible, what generally distorts the current shape. The power factor is then degraded.

The switching frequency variation is a major limitation of the system that should be reserved to application where the load does not vary drastically.

COIL PEAK AND RMS CURRENTS

Coil Peak Current

As the PFC stage makes the AC line current sinusoidal and in phase with the AC line voltage, one can write:

$$\text{Iin}(t) = \sqrt{2} * \text{Iac} * \sin(\omega t) \qquad \text{(eq. 14)}$$

where Iin(t) is the instantaneous AC line current and Iac its rms value.

Provided that the AC line current results from the averaging of the coil current, one can deduct the following equation:

$$\text{Iin}(t) = < \text{Icoil} >_T = \frac{\text{Icoil\_pk}}{2} \qquad \text{(eq. 15)}$$

where $<\text{Icoil}>_T$ is the average of the considered coil current triangle over the switching period T and Icoil_pk is the corresponding peak.

Thus, the peak value of the coil current triangles follows a sinusoidal envelope and equals:

$$\text{Icoil\_pk} = 2 * \sqrt{2} * \text{Iac} * \sin(\omega t) \qquad \text{(eq. 16)}$$

Since the PFC stage forces the power factor close to 1, one can use the well known relationship linking the average input power to the AC line rms current and rms voltage ($< \text{Pin} > = \text{Vac} * \text{Iac}$) and the precedent equation leads to:

$$\text{Icoil\_pk} = 2 * \sqrt{2} * \frac{< \text{Pin} >}{\text{Vac}} * \sin(\omega t) \qquad \text{(eq. 17)}$$

The coil current peak is maximum at the top of the sinusoid where $\sin(\varpi t) = 1$. This maximum value, (Icoil_pk)H, is then:

$$(\text{Icoil\_pk})\text{H} = 2 * \sqrt{2} * \frac{< \text{Pin} >}{\text{Vac}} \qquad \text{(eq. 18)}$$

From this equation, one can easily deduct that the peak coil current is maximum when the required power is maximum and the AC line at its minimum voltage:

$$\textbf{Icoil\_max} = \mathbf{2} * \sqrt{\mathbf{2}} * \frac{< \textbf{Pin} > \textbf{max}}{\textbf{VacLL}} \qquad \text{(eq. 19)}$$

where <Pin>max is the maximum input power of the application and VacLL the lowest level of the AC line voltage.

Coil RMS Current

The rms value of a current is the magnitude that squared, gives the dissipation produced by this current within a 1.0 Ω resistor. One must then compute the rms coil current by:

- First calculating the “rms current” within a switching period in such a way that once squared, it would give the power dissipated in a 1.0 Ω resistor during the considered switching period.
- Then the switching period being small compared to the input voltage cycle, regarding the obtained expression as the instantaneous square of the coil current and averaging it over the rectified sinusoid cycle, to have the squared coil rms current.

This method will be used in this section. As above explained, the current flowing through the coil is:

- ($I_M(t) = \text{Vin} * t/L = \text{Icoil\_pk} * t/\text{ton}$) during the MOSFET on−time, when $0 < t < \text{ton}$.
- ($I_D(t) = \text{Icoil\_pk} - [(\text{Vout} - \text{Vin}) * t/L] = \text{Icoil\_pk} * (T - t)/(T - \text{ton})$) during the diode conduction time, that is, when $\text{ton} < t < T$.

Therefore, the rms value of any coil current triangle over the corresponding switching period T, is given by the following equation:

$$< (\text{Icoil})\text{rms} >_T = \sqrt{\frac{1}{T} * \left(\int_0^{\text{ton}} \left[\frac{\text{Icoil\_pk} * t}{\text{ton}} \right]^2 * dt + \int_{\text{ton}}^{T} \left[\text{Icoil\_pk} * \frac{T - t}{T - \text{ton}} \right]^2 * dt \right)} \qquad \text{(eq. 20)}$$

Solving the integrals, it becomes:

$$< (\text{Icoil})\text{rms} >_T = \sqrt{\frac{1}{T} * \left(\left[\frac{\text{Icoil\_pk}^2}{\text{ton}^2} * \frac{\text{ton}^3}{3} \right] + \left[\frac{-(T - \text{ton})}{3 * \text{Icoil\_pk}} * \left(\left[\text{Icoil\_pk} * \frac{T - T}{T - \text{ton}} \right]^3 - \left[\text{Icoil\_pk} * \frac{T - \text{ton}}{T - \text{ton}} \right]^3 \right) \right] \right)} \qquad \text{(eq. 21)}$$

The precedent simplifies as follows:

$$< (Icoil)rms >_T = \sqrt{\frac{1}{T} * \left(\frac{Icoil\_pk^2 * ton}{3} + \left[\frac{-(T - ton)}{3 * Icoil\_pk} * (-Icoil\_pk^3) \right] \right)} \quad \text{(eq. 22)}$$

Rearrangement of the terms leads to:

$$< (Icoil)rms >_T = I_{coil\_pk} * \sqrt{\frac{1}{T} * \left(\frac{ton}{3} + \frac{T - ton}{3} \right)} \quad \text{(eq. 23)}$$

Calculating the term under the root square sign, the following expression is obtained:

$$< (Icoil)rms >_T = \frac{Icoil\_pk}{\sqrt{3}} \quad \text{(eq. 24)}$$

Replacing the coil peak current by its expression as a function of the average input power and the AC line rms voltage (equation 17), one can write the following equation:

$$< (Icoil)rms >_T = 2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sin(\omega t) \quad \text{(eq. 25)}$$

This equation gives the equivalent rms current of the coil over one switching period, that is, at a given V_{in}. As already stated, multiplying the square of it by the coil resistance, gives the resistive losses at this given V_{in}. Now to have the rms current over the rectified AC line period, one must not integrate $<(Icoil)rms>_T$ but the square of it, as we would have proceeded to deduct the average resistive losses from the dissipation over one switching period. However, one must not forget to extract the root square of the result to obtain the rms value.

As the consequence, the coil rms current is:

$$(Icoil)rms = \sqrt{\frac{2}{Tac} * \int_0^{Tac/2} < (I_{coil})rms >_T^2 * dt} \quad \text{(eq. 26)}$$

where $Tac = 2*\pi/\omega$ is the AC line period (20 ms in Europe, 16.66 ms in USA). The PFC stage being fed by the rectified AC line voltage, it operates at twice the AC line frequency. That is why, one integrates over half the AC line period (Tac/2).

Substitution of equation (25) into the precedent equation leads to:

$$(Icoil)rms = \sqrt{\frac{2}{Tac} * \int_0^{Tac/2} \left[2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sin(\omega t) \right]^2 * dt} \quad \text{(eq. 27)}$$

This equation shows that the coil rms current is the rms value of: $2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sin(\omega t)$, that is, the rms value of a sinusoidal current whose magnitude is $(2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac})$. The rms value of such a sinusoidal current is well known (the amplitude divided by $\sqrt{2}$).

Therefore:

$$\mathbf{Icoil(rms)} = \frac{\mathbf{2}}{\sqrt{\mathbf{3}}} * \frac{\mathbf{< Pin >}}{\mathbf{Vac}} \quad \text{(eq. 28)}$$

Switching Losses

The switching losses are difficult to determine with accuracy. They depend of the MOSFET type and in particular of the gate charge, of the controller driver capability and obviously of the switching frequency that varies dramatically in a critical conduction mode operation. However, one can make a rough estimation if one assumes the following:

- The output voltage is considered as a constant. The output voltage ripple being generally less than 5% the nominal voltage, this assumption seems reasonable.
- The switching times (δt and t_{FR}, as defined in Figure 9), are considered as constant over the sinusoid.

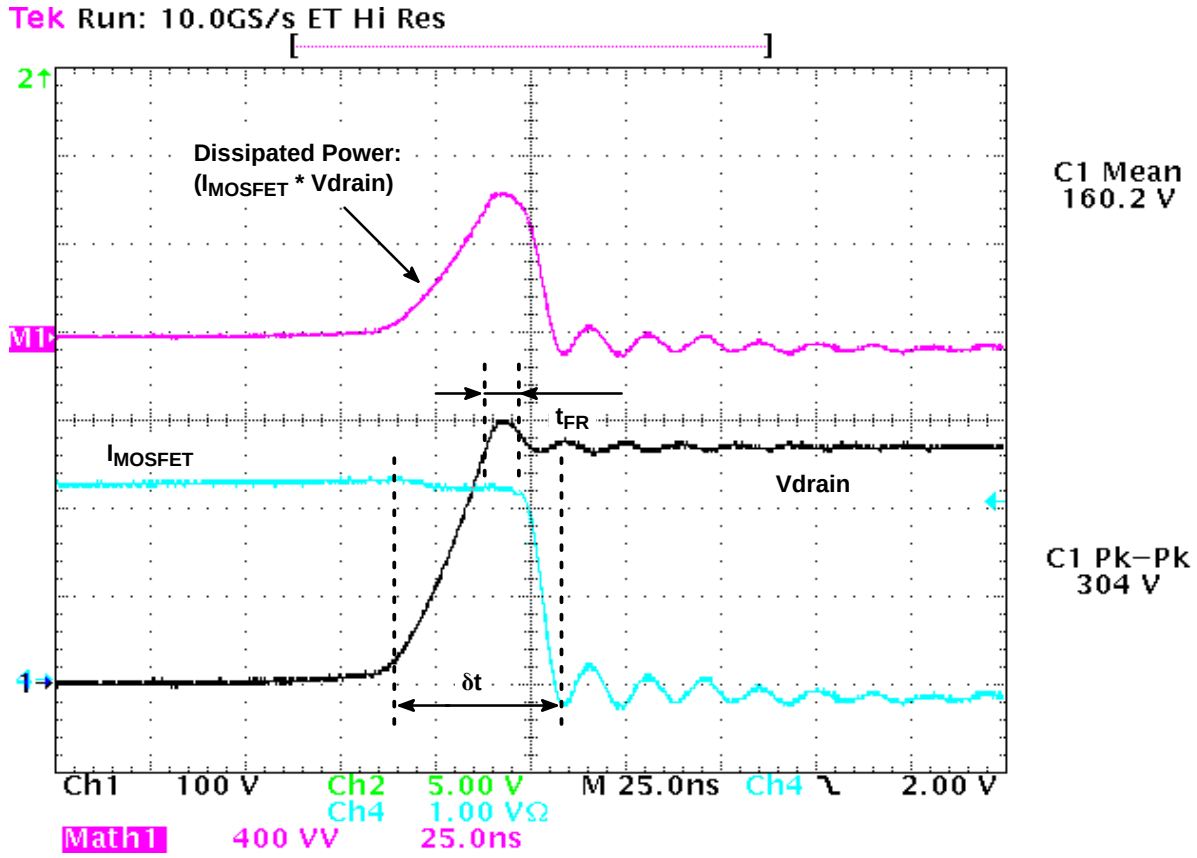

Figure 9. Turn Off Waveforms

Figure 9 represents a turn off sequence. One can observe three phases:

- During approximately the second half of the gate voltage Miller plateau, the drain−source voltage increases linearly till it reaches the output voltage.
- During a short time that is part of the diode forward recovery time, the MOSFET faces both maximum voltage and current.
- The gate voltage drops (from the Miller plateau) below the gate threshold and the drain current ramps down to zero.

"δt" of Figure 9 represents the total time of the three phases, "t_{FR}" the second phase duration.

Therefore, one can write:

$$psw = \left(\frac{Vout * Icoil\_pk}{2} * \frac{\delta t - t_{FR}}{T}\right) + \left(Vout * Icoil\_pk * \frac{t_{FR}}{T}\right) \quad \text{(eq. 29)}$$

where: δt and t_{FR} are the switching times portrayed by Figure 9 and T is the switching period.

Equation (9) gives an expression linking the coil peak current and the switching period of the considered current cycle (triangle): $T = \frac{L * Icoil\_pk}{Vin} * \frac{Vout}{Vout - Vin}$.

Substitution of equation (9) into the equation (29) leads to:

$$psw = \frac{Vin * (Vout - Vin) * (\delta t + t_{FR})}{2 * L} \quad \text{(eq. 30)}$$

This equation shows that the switching losses over a switching period depend of the instantaneous input voltage, the difference between the instantaneous output and input voltages, the switching time and the coil value. Let's calculate the average losses (<psw>) by integrating psw over half the AC line period:

$$< psw > = \frac{2}{Tac} * \int_0^{Tac/2} \frac{Vin * (Vout - Vin) * (\delta t + t_{FR})}{2 * L} * dt \quad \text{(eq. 31)}$$

Rearranging the terms, one obtains:

$$< psw > = \frac{\delta t + t_{FR}}{2 * L} * \left\{\left(\frac{2}{Tac} * \int_0^{Tac/2} Vin * Vout * dt\right) - \left(\frac{2}{Tac} * \int_0^{Tac/2} Vin^2 * dt\right)\right\} \quad \text{(eq. 32)}$$

V_{out} being considered as a constant, one can easily solve this equation if one remembers that the input voltage average value is $(2 * \sqrt{2} * Vac/\pi)$ and that $(Vac^2 = \frac{2}{Tac} * \int_0^{Tac/2} Vin^2 * dt)$. Applying this, it becomes:

$$< psw > = \frac{\delta t + t_{FR}}{2 * L} * \left(\frac{2 * \sqrt{2} * Vac * Vout}{\pi} - Vac^2 \right) \quad \text{(eq. 33)}$$

Or in a simpler manner:

$$< psw > = \frac{2 * (\delta t + t_{FR}) * Vac^2}{\pi * L} * \left(\frac{Vout}{\sqrt{2} * Vac} - \frac{\pi}{4} \right) \quad \text{(eq. 34)}$$

The coil inductance (L) plays an important role: the losses are inversely proportional to this value. It is simply because the switching frequency is also inversely proportional to L.

This equation also shows that the switching losses are independent of the power level. One could have easily predict this result by simply noting that the switching frequency increased when power diminished.

Equation (34) also shows that the lower the ratio (V_{out}/Vac), the smaller the MOSFET switching losses. That is because the “Follower Boost” mode that reduces the difference between the output and input voltages, lowers the switching frequency. In other words, this technique enables the use of a smaller coil for the same switching frequency range and the same switching losses.

For instance, the MC33260 features the “Follower Boost” operation where the pre-converter output voltage stabilizes at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage [1].

How to extract δt and t_{FR}?

- The best is to measure them.
- One can approximate δt as the time necessary to extract the gate charge Q3 of the MOSFET (refer to Figure 10). Q3 being not always specified, instead, one can take the sum of Q1 with half the Miller plateau gate charge (Q2/2). Knowing the drive capability of the circuit, one can deduct the turn off time ($\delta t = Q3/I_{drive}$ or $\delta t = [Q1 + (Q2/2)]/I_{drive}$).
- In a first approach, t_{FR} can be taken equal to the diode forward recovery time.

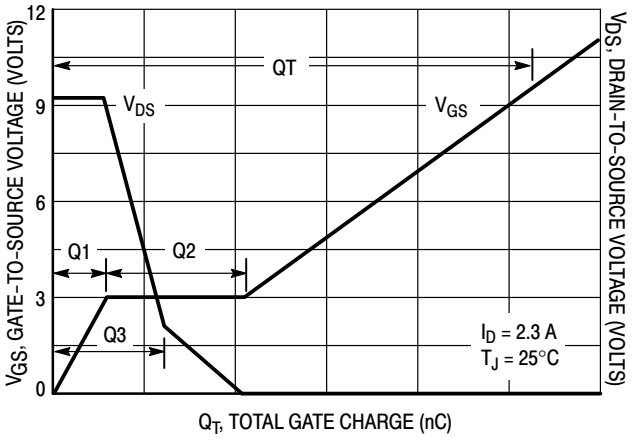

Figure 10. Typical Total Gate Charge Specification of a MOSFET

One must note that the calculation does not take into account:

- The energy consumed by the controller to drive the MOSFET (Qcc*Vcc*f), where Qcc is the MOSFET gate charge necessary to charge the gate voltage to Vcc, Vcc the driver supply voltage and f the switching frequency.
- The energy dissipated because of the parasitic capacitors of the PFC stage. Each turn on produces an abrupt voltage change across the parasitic capacitors of the MOSFET drain−source, the diode and the coil. This results in some extra dissipation across the MOSFET ($1/2*C_{parasitic}*\Delta V^2*f$), where $C_{parasitic}$ is the considered parasitic capacitor and ΔV the voltage change across it.

[1] Refer to MC33260 data sheet for more details at www.onsemi.com

However, equation (34) should give a sufficient first approach approximation in most applications where the two listed sources of losses play a minor role. Nevertheless, the losses produced by the parasitic capacitors may become significant in light load conditions where the switching frequency gets high. As always, bench validation is key.

Power MOSFET Conduction Losses

As portrayed by Figure 4, the coil current is formed by high frequency triangles. The input capacitor together with the input RFI filter integrates the coil current ripple so that the resulting AC line current is sinusoidal.

During the on-time, the current rises linearly through the power switch as follows:

$$Icoil(t) = \frac{Vin}{L} * t \quad \text{(eq. 35)}$$

where V_{in} is the input voltage $(Vin = \sqrt{2} * Vac * \sin(\omega t))$, L is the coil inductance and t is the time.

During the rest of the switching period, the power switch is off. The conduction losses resulting from the power dissipated by Icoil during the on-time, one can calculate the power during the switching period T as follows:

$$p_T = \frac{1}{T} * \int_0^{ton} Ron * Icoil(t)^2 * dt = \frac{1}{T} * \int_0^{ton} Ron * \left(\frac{Vin}{L} * t\right)^2 * dt \quad \text{(eq. 36)}$$

where Ron is the MOSFET on-time drain source resistor, ton is the on-time.

Solving the integral, equation (36) simplifies as follows:

$$p_T = \frac{Ron}{T} * \left(\frac{Vin}{L}\right)^2 * \int_0^{ton} t^2 * dt = \frac{1}{3} * Ron * \left(\frac{Vin}{L}\right)^2 * \frac{ton^3}{T} \quad \text{(eq. 37)}$$

As the coil current reaches its peak value at the end of the on-time, $Icoil\_pk = Vin * ton/L$ and the precedent equation can be rewritten as follows:

$$p_T = \frac{1}{3} * Ron * Icoil\_pk^2 * \frac{ton}{T} \quad \text{(eq. 38)}$$

One can recognize the traditional equation permitting to calculate the MOSFET conduction losses in a boost or a flyback ($\frac{1}{3} * Ron * Ipk^2 * d$, where Ipk is the peak current and d, the MOSFET duty cycle).

One can calculate the duty cycle (d = ton/T) by:

- Either noting that the off-time (toff) can be expressed as a function of ton (refer to equation 3) and substituting this equation into (T = ton + Toff),
- Or considering that the critical conduction mode being at the border of the continuous conduction mode (CCM), the expression giving the duty-cycle in a CCM boost converter applies.

Both methods lead to the same following result:

$$d = \frac{ton}{T} = 1 - \frac{Vin}{Vout} \quad \text{(eq. 39)}$$

Substitution of equation (39) into equation (38) leads to:

$$p_T = \frac{1}{3} * Ron * Icoil\_pk^2 * \left(1 - \frac{Vin}{Vout}\right) \quad \text{(eq. 40)}$$

One can note that the coil peak current (Icoil_pk) that follows a sinusoidal envelop, can be written as follows: $Icoil\_pk = 2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)$ (refer to equation 17).

Replacing V_{in} and Icoil_pk by their sinusoidal expression, respectively ($\sqrt{2} * Vac * \sin(\omega t)$) and ($2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)$), equation (40) becomes:

$$p_T = \frac{1}{3} * Ron * \left(2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)\right)^2 * \left(1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout}\right) \quad \text{(eq. 41)}$$

That is in a more compact form:

$$p_T = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \left[\sin^2(\omega t) - \left(\frac{\sqrt{2} * Vac}{Vout} * \sin^3(\omega t)\right)\right] \quad \text{(eq. 42)}$$

Equation (42) gives the conduction losses at a given V_{in} voltage. This equation must be integrated over the rectified AC line sinusoid to obtain the average losses:

$$< p > Tac = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \frac{2}{Tac} * \int_0^{Tac/2} \left[\sin^2(\omega t) - \left(\frac{\sqrt{2} * Vac}{Vout} * \sin^3(\omega t)\right)\right] * dt \quad \text{(eq. 43)}$$

If the average value of $\sin^2(\omega t)$ is well known (0.5), the calculation of $<\sin^3(\omega t)>$ requires few trigonometry remembers:

- $\sin^2(\alpha) = \frac{1 - \cos(2\alpha)}{2}$
- $\sin(\alpha) * \cos(\beta) = \frac{\sin(\alpha + \beta) + \sin(\alpha - \beta)}{2}$

Combining the two precedent formulas, one can obtain:

$$\sin^3(\omega t) = \frac{3 * \sin(\omega t)}{4} - \frac{\sin(3\omega t)}{4} \quad \text{(eq. 44)}$$

Substitution of equation 44) into equation (43) leads:

$$< p > Tac = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \frac{2}{Tac} * \int_0^{Tac/2} \left[\sin(\omega t)^2 - \left(\frac{3 * \sqrt{2} * Vac}{4 * Vout} * \sin(\omega t)\right) + \left(\frac{\sqrt{2} * Vac}{4 * Vout} * \sin(3\omega t)\right)\right] * dt \quad \text{(eq. 45)}$$

Solving the integral, it becomes:

$$< p > Tac = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \left[\frac{1}{2} - \left(\frac{3 * \sqrt{2} * Vac}{4 * Vout} * \frac{2}{\pi}\right) + \left(\frac{\sqrt{2} * Vac}{4 * Vout} * \frac{2}{3\pi}\right)\right] \quad \text{(eq. 46)}$$

Equation (46) simplifies as follows:

$$< p > Tac = \frac{4}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \left[1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right)\right] \quad \text{(eq. 47)}$$

This formula shows that the higher the ratio (Vac/V_{out}), the smaller the MOSFET conduction losses. That is why the "Follower Boost" mode that reduces the difference between the output and input voltages, enables to reduce the MOSFET size.

For instance, the MC33260 features the "Follower Boost" operation where the pre-converter output voltage stabilizes at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage[2].

By the way, one can deduct from this equation the rms current ((I_M)rms) flowing through the power switch knowing that $< p > Tac = Ron * (I_M)^2 rms$:

$$(I_M)rms = \frac{2}{\sqrt{3}} * \frac{< Pin >}{Vac} * \sqrt{1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right)} \quad \text{(eq. 48)}$$

Dissipation within the Current Sense Resistor

PFC controllers monitor the power switch current either to perform the shaping function or simply to prevent it from being excessive. That is why a resistor is traditionally placed between the MOSFET source and ground to sense the power switch current.

[2] Refer to MC33260 data sheet for more details at www.onsemi.com

The MC33260 monitors the whole coil current by monitoring the voltage across a resistor inserted between ground and the diodes bridge (negative sensing – refer to Figure 15). The circuit utilizes the current information for both the overcurrent protection and the core reset detection (also named zero current detection). This technique brings two major benefits:

- No need for an auxiliary winding to detect the core reset. A simple coil is sufficient in the PFC stage.
- The MC33260 detects the in-rush currents that may flow at start-up or during some overload conditions and prevents the power switch from turning on in that stressful condition. The PFC stage is significantly safer.

Some increase of the power dissipated by the current sense resistor is the counter part since the whole current is sensed while circuits like the MC33262 only monitor the power switch current.

Dissipation of the Current Sense Resistor in MC33262 Like Circuits

Since the same current flows through the current sense resistor and the power switch, the calculation is rather easy. One must just square the rms value of the power switch current (I_M)rms calculated in the previous section and multiply the result by the current sense resistance.

Doing this, one obtains:

$$< pRs > 262 = \frac{4}{3} * Rs * \left(\frac{< Pin >}{Vac}\right)^2 * \left[1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right)\right] \quad \text{(eq. 49)}$$

where $<pRs>_{262}$ is the power dissipated by the current sense resistor Rs.

Dissipation of the Current Sense Resistor in MC33260 Like Circuits

In this case, the current sense resistor Rs derives the whole coil current. Consequently, the product of Rs by the square of the rms coil current gives the dissipation of the current sense resistor:

$$< pRs > 260 = Rs * (Icoil(rms))^2 \quad \text{(eq. 50)}$$

where Icoil(rms) is the coil rms current that as expressed by equation (28), equals: $Icoil(rms) = \frac{2}{\sqrt{3}} * \frac{< Pin >}{Vac}$.

Consequently:

$$< pRs > 260 = \frac{4 * Rs}{3} * \left(\frac{< Pin >}{Vac}\right)^2 \quad \text{(eq. 51)}$$

Comparison of the Losses Amount in the Two Cases

Let's calculate the ratios: $< pRs > 262 / < pRs > 260$. One obtains:

$$< pRs > 262 / < pRs > 260 = 1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right) \quad \text{(eq. 52)}$$

If one considers that (8/3 π) approximately equals 0.85, the precedent equation simplifies:

$$< \mathbf{pRs} > \mathbf{262} \; / \; < \mathbf{pRs} > \mathbf{260} \approx \mathbf{1} - \frac{\mathbf{0.85 * Vm}}{\mathbf{Vout}} \quad \text{(eq. 53)}$$

where Vm is the AC line amplitude.

Average and RMS Current through the Diode

The diode average current can be easily computed if one notes that it is the sum of the load and output capacitor currents:

$$Id = I_{load} + I_{Cout} \quad \text{(eq. 54)}$$

Then, in average:

$$< Id > = < I_{load} + I_{Cout} > = < I_{load} > + < I_{Cout} > \quad \text{(eq. 55)}$$

At the equilibrium, the average current of the output capacitor must be 0 (otherwise the capacitor voltage will be infinite). Thus:

$$< \mathbf{Id} > = < \mathbf{I_{load}} > = \frac{\mathbf{Pout}}{\mathbf{Vout}} \quad \text{(eq. 56)}$$

The rms diode current is more difficult to calculate. Similarly to the computation of the rms coil current for instance, it is necessary to first compute the squared rms current at the switching period level and then to integrate the obtained result over the AC line sinusoid.

As portrayed by Figure 4, the coil discharges during the off time. More specifically, the current decays linearly through the diode from its peak value (Icoil_pk) down to zero that is reached at the end of the off-time. Taking the beginning of the off-time as the time origin, one can then write:

$$Icoil(t) = Icoil\_pk * \frac{toff - t}{toff} \quad \text{(eq. 57)}$$

Similarly to the calculation done to compute the coil rms current, one can calculate the “diode rms current over one switching period”:

$$Id(rms)^2_T = \frac{1}{T} * \int_0^{toff} \left[Icoil\_pk * \frac{toff - t}{toff} \right]^2 * dt \quad \text{(eq. 58)}$$

Solving the integral, one obtains the expression of the “rms diode current over one switching period”:

$$Id(rms)_T = \sqrt{\frac{toff}{3 * T}} * Icoil\_pk \quad \text{(eq. 59)}$$

Substitution of equation (17) that expresses Icoil_pk, into the precedent equation leads to:

$$Id(rms)_T = 2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sqrt{\frac{toff}{T}} * \sin(\omega t) \quad \text{(eq. 60)}$$

In addition, one can easily show that toff and T are linked by the following equation:

$$toff = T * \frac{Vin}{Vout} = T * \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \quad \text{(eq. 61)}$$

Consequently, equation (60) can be changed into:

$$Id(rms)_T = \frac{2 * \sqrt{2 * \sqrt{2}}}{\sqrt{3}} * \frac{< Pin >}{\sqrt{Vac * Vout}} * \left(\sqrt{\sin(\omega t)} \right)^3 \quad \text{(eq. 62)}$$

This equation gives the equivalent rms current of the diode over one switching period, that is, at a given V_{in}. As already stated in the Coil Peak and RMS Currents section, the square of this expression must be integrated over a rectified sinusoid period to obtain the square of the diode rms current.

Therefore:

$$Id(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} \frac{8 * \sqrt{2}}{3} * \frac{< Pin >^2}{Vac * Vout} * \sin^3(\omega t) * dt \quad \text{(eq. 63)}$$

Similarly to the Power MOSFET Conduction Losses section, the integration of ($\sin^3(\omega t)$) requires some preliminary trigonometric manipulations:

$$\begin{cases} \sin^3(\omega t) = \sin(\omega t) * \sin^2(\omega t) = \sin(\omega t) * \left(\frac{1 - \cos(2\omega t)}{2} \right) = \frac{1}{2} * \sin(\omega t) - \frac{1}{2} * \sin(\omega t) * \cos(2\omega t) \\ \text{And :} \\ \sin(\omega t) * \cos(2\omega t) = \frac{1}{2} * (\sin(-\omega t) + \sin(4\omega t)) \\ \text{Then :} \\ \sin^3(\omega t) = \frac{3}{4} * \sin(\omega t) - \frac{1}{4} * \sin(3\omega t) \end{cases}$$

Consequently, equation (63) can change into:

$$Id(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} \frac{8 * \sqrt{2}}{3} * \frac{Pin^2}{Vac * Vout} * \left[\frac{3 * \sin(\omega t)}{4} - \frac{\sin(3\omega t)}{4} \right] * dt \quad \text{(eq. 64)}$$

One can now solve the integral and write:

$$Id(rms)^2 = \frac{16 * \sqrt{2}}{3 * Tac} * \frac{< Pin >^2}{Vac * Vout} * \left(\frac{3 * (\cos(\omega 0) - \cos(\omega Tac/2))}{4\omega} + \frac{\cos(3\omega Tac/2) - \cos(3\omega 0)}{12\omega} \right) \quad \text{(eq. 65)}$$

As ($\varpi * Tac = 2\pi$), we have:

$$Id(rms)^2 = \frac{16 * \sqrt{2}}{3} * \frac{Pin^2}{Vac * Vout} * \left(\frac{3 * (1 - \cos(\pi))}{4\omega * Tac} + \frac{\cos(\pi) - 1}{12\omega * Tac} \right) \quad \text{(eq. 66)}$$

One can simplify the equation replacing the cosine elements by their value:

$$Id(rms)^2 = \frac{16 * \sqrt{2}}{3} * \frac{< Pin >^2}{Vac * Vout} * \left(\frac{6}{8 * \pi} - \frac{1}{12 * \pi} \right) \quad \text{(eq. 67)}$$

The square of the diode rms current simplifies as follows:

$$Id(rms)^2 = \frac{32 * \sqrt{2}}{9 * \pi} * \frac{< Pin >^2}{Vac * Vout} \quad \text{(eq. 68)}$$

Finally, the diode rms current is given by:

$$\mathbf{Id(rms) = \frac{4}{3} * \frac{\sqrt{2 * \sqrt{2}}}{\pi} * \frac{< Pin >}{\sqrt{Vac * Vout}}} \quad \text{(eq. 69)}$$

Output Capacitor RMS Current

As shown by Figure 11, the capacitor current results from the difference between the diode current (I1) and the current absorbed by the load (I2):

$$Ic(t) = I1(t) - I2(t) \quad \text{(eq. 70)}$$

Thus, the capacitor rms current over the rectified AC line period, is the rms value of the difference between I1 and I2 during this period. As a consequence:

$$Ic(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} (I1 - I2)^2 * dt \quad \text{(eq. 71)}$$

Rearranging $(I1-I2)^2$ leads to:

$$Ic(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} [I1^2 + I2^2 - (2 * I1 * I2)] * dt \quad \text{(eq. 72)}$$

Thus:

$$Ic(rms)^2 = I1(rms)^2 + I2(rms)^2 - \frac{4}{Tac} * \int_0^{Tac/2} I1 * I2 * dt \quad \text{(eq. 73)}$$

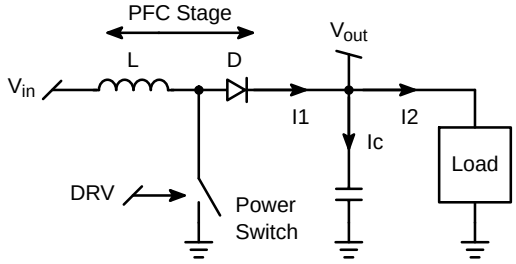

Figure 11. Output Capacitor Current

One knows the first term $(I1(rms)^2)$. This is the diode rms current calculated in the previous section. The second and third terms are dependent of the load. One cannot compute them without knowing the characteristic of this load.

Anyway, the second term $(I2(rms)^2)$ is generally easy to calculate once the load is known. Typically, this is the rms current absorbed by a downstream converter. On the other hand, the third term is more difficult to determine as it depends on the relative occurrence of the I1 and I2 currents. As the PFC stage and the load (generally a switching mode power supply) are not synchronized, this term even seems impossible to predict. One can simply note that this term tends to decrease the capacitor rms current and consequently, one can deduct that:

$$Ic(rms) \leq \sqrt{I1(rms)^2 + I2(rms)^2} \quad \text{(eq. 74)}$$

Substitution of equation (69) that gives the diode rms current into the precedent equation leads to:

$$\mathbf{Ic(rms) \leq \sqrt{\frac{32 * \sqrt{2} * < Pin >^2}{9 * \pi * Vac * Vout} + I2(rms)^2}} \quad \text{(eq. 75)}$$

where I2(rms) is the load rms current.

If the load is resistive, $I2 = V_{out}/R$ where R is the load resistance and equation (73) changes into:

$$Ic(rms)^2 = I1(rms)^2 + \left(\frac{Vout}{R} \right)^2 - \frac{4}{Tac} * \int_0^{Tac/2} I1 * \frac{Vout}{R} * dt \quad \text{(eq. 76)}$$

Thus, the capacitor squared rms current is:

$$Ic(rms)^2 = Id(rms)^2 + \left(\frac{Vout}{R} \right)^2 \frac{2 * Vout}{R} * < Id > \quad \text{(eq. 77)}$$

$$Ic(rms)^2 = \frac{32 * \sqrt{2}}{9 * \pi} * \frac{< Pin >^2}{Vac * Vout} + \left(\frac{Vout}{R} \right)^2 - \left(\frac{2 * Vout}{R} * \frac{Pout}{Vout} \right) \quad \text{(eq. 78)}$$

As $Pout = V_{out}^2/R$, the precedent equation simplifies as follows:

$$\mathbf{Ic(rms) = \sqrt{\left[\frac{32 * \sqrt{2}}{9 * \pi} * \frac{< Pin >^2}{Vac * Vout} \right] - \left(\frac{Vout}{R} \right)^2}} \quad \text{(eq. 79)}$$

You may find a more friendly expression in the literature: $Ic(rms) = \frac{I2}{\sqrt{2}}$, where I2 is the load current. This equation is an approximate formula that does not take into account the switching frequency ripple of the diode current. Only the low frequency current that generates the low frequency ripple of the bulk capacitor (refer to the next section) is considered (this expression can easily be found by using equation (90) and computing $Ibulk = Cbulk * dVout/dt$).

Equation (79) takes into account both high and low frequency ripples.

Output Voltage Ripple

The output voltage (or bulk capacitor voltage) exhibits two ripples.

The first one is traditional to Switch Mode Power Supplies. This ripple results from the way the output is fed by current pulses at the switching frequency pace. As bulk capacitors exhibit a parasitic series resistor (ESR – refer to Figure 12), they cannot fully filter this pulsed energy source.

More specifically:

- During the on-time, the PFC MOSFET conducts and no energy is provided to the output. The bulk capacitor feeds the load with the current it needs. The current together with the ESR resistor of the bulk capacitor form a negative voltage –(ESR*I2), where I2 is the instantaneous load current,
- During the off-time, the diode derives the coil current towards the output and the current across the ESR becomes ESR*(Id−I2), where Id is the instantaneous diode current.

This explanation assumes that the energy that is fed by the PFC stage perfectly matches the energy drawn by the load over each switching period so that one can consider that the capacitive part of the bulk has a constant voltage and that only the ESR creates some ripple.

In fact, there is an additional low frequency ripple which is inherent to the Power Factor Correction. The input current and voltage being sinusoidal, the power fed by the PFC stage has a squared sinusoid shape. On the other hand, the load generally draws a constant power. As a consequence, the PFC pre-converter delivers an amount of power that matches the load demand in average only. The output capacitor compensates the lack (excess) of input power by supplying (storing) the part of energy necessary for the instantaneous matching. Figures 13 and 14 sketch this behavior.

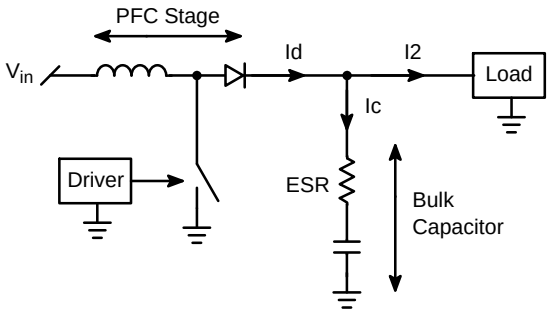

Figure 12. ESR of the Output Capacitor

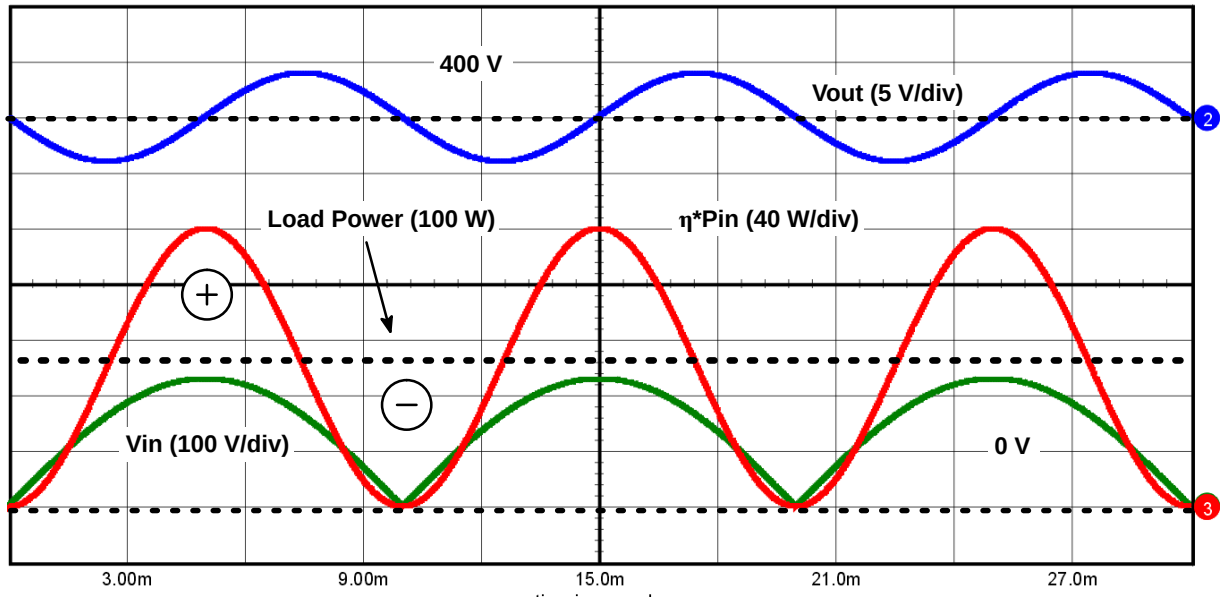

Figure 13. Output Voltage Ripple

The dashed black line represents the power that is absorbed by the load. The PFC stage delivers a power that has a squared sinusoid shape. As long as this power is lower than the load demand, the bulk capacitor compensates by supplying part of the energy it stores. Consequently the output voltage decreases. When the power fed by the PFC pre-converter exceeds the load consumption, the bulk capacitor recharges. The peak of the PFC power is twice the load demand.

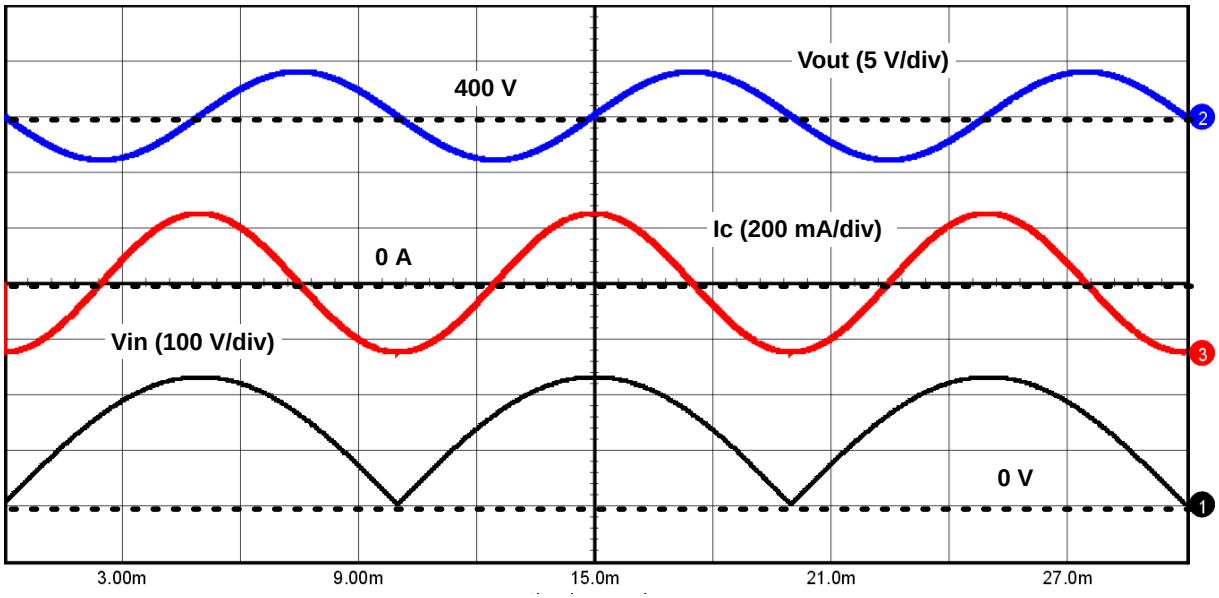

Figure 14. Output Voltage Ripple

The output voltage equals its average value when the input voltage is minimum and maximum. The output voltage is lower than its average value during the rising phase of the input voltage and higher during the input voltage decay. Similarly to the input power and voltage, the frequency of the capacitor current (represented in the case of a resistive load) is twice the AC line one.

In this calculation, one does not consider the switching ripple that is generally small compared to the low frequency ripple. In addition, the switching ripple depends on the load current shape that cannot be predicted in a general manner.

As already discussed, the average coil current over a switching period is:

$$Iin = \frac{\sqrt{2} * < Pin >}{Vac} * \sin(\omega t) \qquad \text{(eq. 80)}$$

The instantaneous input power (averaged over the switching period) is the product of the input voltage ($\sqrt{2} * Vac * \sin(\varpi t)$) by Iin. Consequently:

$$Pin = 2 * < Pin > * \sin^2(\omega t) \qquad \text{(eq. 81)}$$

In average over the switching period, the bulk capacitor receives a charge current ($\eta * Pin/Vout$), where η is the PFC stage efficiency, and supplies the averaged load current $< I2 > = \eta * < Pin > / Vout$. Applying the famous "capacitor formula" $I = C * dV/dt$, it becomes:

$$\eta * \frac{Pin}{Vout} - < I2 > = Cbulk * \frac{dVout}{dt} \qquad \text{(eq. 82)}$$

Substitution of equation (81) into equation (82) leads to:

$$\frac{dVout}{dt} = \frac{1}{Cbulk} * \left(\frac{2 * \eta * < Pin > * \sin^2(\omega t)}{Vout} - \frac{\eta * < Pin >}{Vout} \right) \qquad \text{(eq. 83)}$$

Rearranging the terms of this equation, one can obtain:

$$Vout * \frac{dVout}{dt} = \frac{\eta * < Pin >}{Cbulk} * \left[2 * \sin^2(\omega t) - 1 \right] \qquad \text{(eq. 84)}$$

Noting that $\frac{d(Vout^2)}{dt} = 2 * Vout * \frac{dVout}{dt}$ and that $\cos(2\omega t) = 1 - 2 * \sin^2(\omega t)$, one can deduct the square of the output voltage from the precedent equation:

$$Vout^2 - < Vout >^2 = \frac{-\eta * < Pin >}{Cbulk * \omega} * \sin(2\omega t) \qquad \text{(eq. 85)}$$

where $<V_{out}>$ is the average output voltage.

Dividing the terms of the precedent equations by the square of the average output voltage, it becomes:

$$\left(\frac{Vout}{< Vout >} \right)^2 = 1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2} \qquad \text{(eq. 86)}$$

Thus:

$$\frac{< Vout > + \delta Vout}{< Vout >} = \sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} \qquad \text{(eq. 87)}$$

Where δV_{out} is the instantaneous output voltage ripple.

Equation (87) can be rearranged as follows:

$$\delta Vout = < Vout > * \left(\sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} - 1 \right) \quad \text{(eq. 88)}$$

One can simplify this equation considering that the output voltage ripple is small compared to the average output voltage (fortunately, it is generally true). This leads to say that the term $\left(\sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} - 1 \right)$ is nearly zero or in other words, that $\left(\frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2} \right)$ is small compared to 1. Thus, one can write that:

$$\sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} \approx 1 - \frac{1}{2} * \frac{\eta < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2} \quad \text{(eq. 89)}$$

Substitution of equation (88) into equation (89), leads to the simplified ripple expression that one can generally find in the literature:

$$\delta Vout = \frac{-\eta * < Pin > * \sin(2\omega t)}{2 * Cbulk * \omega * < Vout >} \quad \text{(eq. 90)}$$

The maximum ripple is obtained when ($\sin(2\varpi t) = -1$) and minimum when ($\sin(2\omega t) = 1$). Thus, the peak-to-peak ripple that is the difference of these two values is:

$$\mathbf{(\delta Vout)pk-pk} = \frac{\boldsymbol{\eta * < Pin >}}{\mathbf{Cbulk * \omega * < Vout >}} \quad \text{(eq. 91)}$$

And:

$$\mathbf{Vout} = < \mathbf{Vout} > - \frac{\mathbf{(\delta Vout)pk-pk}}{\mathbf{2}} * \mathbf{\sin(2\omega t)} \quad \text{(eq. 92)}$$

CONCLUSION

Compared to traditional switch mode power supplies, one faces an additional difficulty when trying to predict the currents and voltages within a PFC stage: the sinusoid modulation. This is particularly true in critical conduction mode where the switching ripple cannot be neglected. As proposed in this paper, one can overcome this difficulty by:

- First calculating their value within a switching period,
- Then the switching period being considered as very small compared to the AC line cycle, integrating the result over the sinusoid period.

The proposed theoretical analysis helps predict the stress faced by the main elements of the PFC stages: coil, MOSFET, diode and bulk capacitor, with the goal of easing the selection of the power components and therefore, the PFC implementation. Nevertheless, as always, it cannot replace the bench work and the reliability tests necessary to ensure the application proper operation.

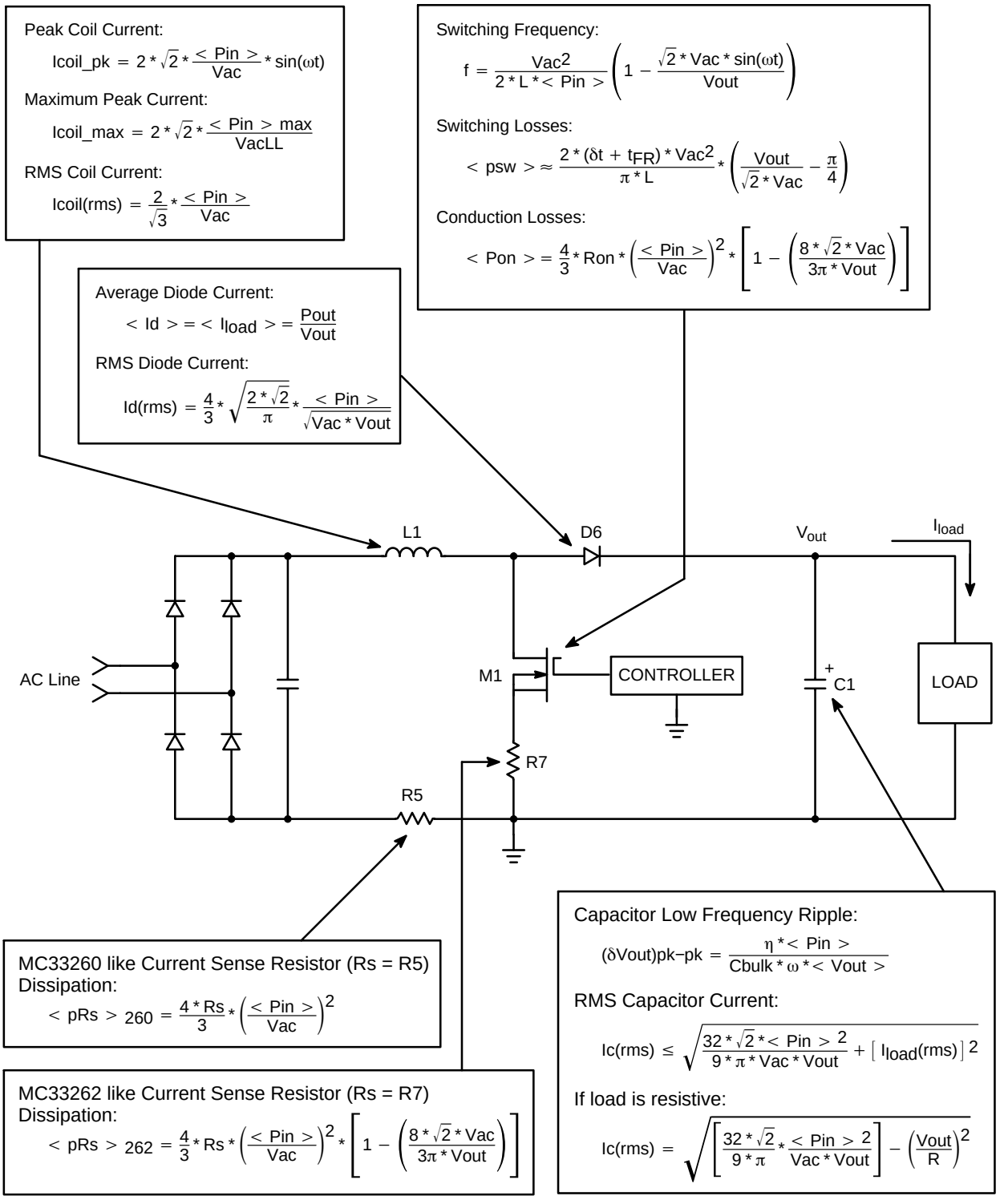

Figure 15. Summary

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